Timeline

t = 0ns → Digital Input

t = 0-2ns → FSM Controller (IDLE → Decode → Prepare → MVM)

t = 2-4ns → DAC Array (Digital → Analog Conversion)

t = 4ns → Wordline Distribution (16 Voltage)

t = 4-14ns → Crossbar Core (Matrix_vector Multiplication)

t = 14ns → Bitline Current Collection (16 Current)

t = 14-19ns → TIA Array (Current → Voltage Conversion)

t = 19-24ns → ADC Array (Voltage → Digital Conversion)

t = 24-27ns → VPU Processing (Vector processing pipeline)

t = 27-28.5ns → System Output (FIFO → DMA → Interface)

t = 28.5 ns → output

Crossbar Array

16*16