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A low power and high linearity UWB low noise amplifier (LNA) for 3.1–10.6 GHz wireless applications in 0.13 μm CMOS process

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ABSTRACT

In this paper, a low power ultra-wideband (UWB) CMOS LNA was designed exploiting source inductive degeneration technique operating in the frequency range of 3.1–10.6 GHz. In order to achieve low noise figure and high linearity simultaneously, a modified three-stage UWB LNA with inter-stage inductors was proposed. Forward Body-Biased (FBB) technique was used to reduce threshold voltage and power consumption at the first and third stages. The second stage is a push–pull topology exploiting the complementary characteristics of NMOS and PMOS transistors to enhance the linearity performance. The proposed LNA was simulated in standard 0.13 μm CMOS process. A gain of 19.5 ± 1.5 dB within the entire band was exhibited. The simulated noise figure (NF) was 1–3.9 dB within the bandwidth. A maximum simulated third-order input intercept point (IIP3) of 4.56 dBm while consuming 4.1 mW from a 0.6 power supply was achieved. The simulated input return loss (S_{11}) was less than −5 dB from 4.9 to 12.1 GHz. The output return loss (S_{22}) was below −10.6 dB and S_{12} was better than −70.6 dB.

1. Introduction

Since the Federal Communication Commission (FCC) has allocated 7500 MHz bandwidth for UWB application in the unlicensed frequency range of 3.1–10.6 GHz, the related technologies have attracted much attention from both industry and academia [1]. This technology has become more popular for broadband wireless communication research due to its characteristics of high data rates, low power transmission, robustness for multi-path fading and low power dissipation [2]. LNA is the first stage of any communication receiver, and its main function is to overcome the noise problem for subsequent stages providing enough gain to make the signal easier to process [3]. LNA design involves tradeoffs among many of figures of merits, such as gain, noise, power dissipation, input matching, stability, and linearity [4]. Such an amplifier must feature wide-band input matching to a 50 Ω antenna, flat gain over the entire bandwidth, good linearity, minimum possible noise figure, and low power consumption [5]. The increasing demands on portable wireless devices have motivated the development of CMOS Radio Frequency Integrated Circuits (RFICs), these portable devices require low power dissipation to maximize Buttery lifetime [6]. Integrating large amount of circuits for sure requires low power consumption design techniques; therefore wide attention has been paid to the low power fully integrated LNA designs [7]. However, due to inductive loss, the input filtering structure choice can greatly affect the noise figure performance at higher frequencies, gain flatness in band [8]. Instead of using conventional second or third-order Chebyshev filtering structures, a high pass filter is designed to reduce the number of inductors, die area, cost, and noise performance. Several CMOS LNAs have been successfully demonstrated in UWB technology as reported in [1,8,9].

We proposed a three-stage LNA to solve the noise figure and linearity problems, simultaneously. The designed UWB LNA is based on the cascode topology as the first stage to achieve good trade-offs among noise figure, input return loss, and gain. A Complementary Push–Pull (CPP) topology is used to improve the linearity of the proposed LNA as the second stage. A simple Common Source (CS) with shunt peaking technique is designed as the third stage to enhance the gain in the frequency range.

This paper is organized as follows. In Section 2, input impedance matching network will be described. FBB and linearization techniques will be presented in Section 3. In Section 4, we explain the gain and noise analysis of the designed circuit. The proposed circuit and design considerations are presented in Section 5. In Section 6, the simulation results and a comparison with other published works are presented. Section 7 summarizes and concludes this work.

2. Input impedance matching network

The wideband input impedance matching is one of the most critical design tasks in UWB circuits [8]. To deliver the maximum

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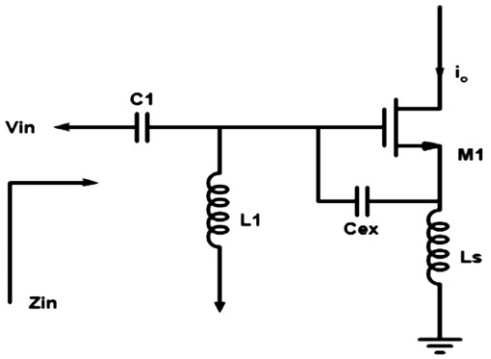

Fig. 1. Input impedance matching network.

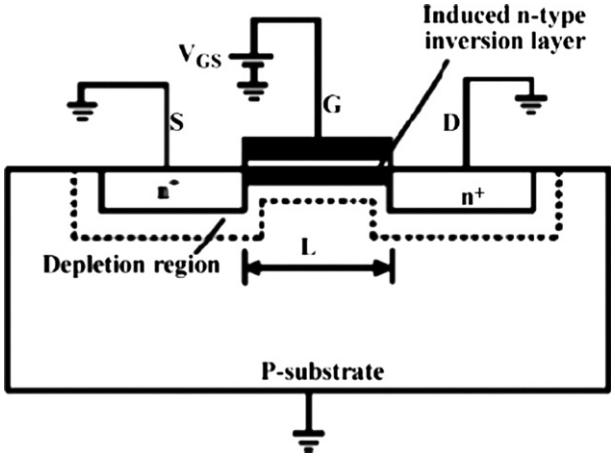

Fig. 2. Vertical cross-section of an n-MOS with positive gate voltage applied [14].

power from the antenna to the LNA, matching to the impedance of antenna, e.g., 50 Ω is required at the input port of the LNA. For wideband application, this impedance matching should be obtained over a wide frequency range at the input port of the LNA and is usually a major challenge considering the noise and power consumption requirements. To overcome the deleterious effect of real resistors on the NF of LNAs, designers suggest the use of inductively degenerated LNA to generate the required input impedance. This topology produces a real resistor, with this advantage that it does not have the thermal noise of a resistor; therefore, the noise figure of the LNA can be reduced. The inductively degenerated common-source technique is widely used in narrow band designs [10]. However, in this paper a high pass filtering structure with source inductive degeneration is chosen at the input port of the LNA to achieve wideband impedance matching.

The LC filtering structure performs two tasks: (i) filtering network function to obtain the desired lower-end cut-off characteristic; (ii) to achieve low input return loss coefficient within the desired band. The cut-off frequency of high pass LC filter is chosen close to lower-end cut-off frequency for suppressing signals outside the whole band.

The combination of M_1 input parasitic capacitance (C_{gs}), external capacitance (C_{ex}), source degeneration inductor (L_s) and input LC filter form a multisection LC ladder filtering structure that can achieve a wideband input matching characteristic of 50 Ω. The input impedance which can be seen from the input port of the LNA is shown in Fig. 1 and expressed as follows:

$$Z_{in}(s)=\frac{1}{sC_1}+sL_1\|\left(sL_s+\frac{1}{sC_t}+R_{eq}\right)\quad\text{and}\quad C_t=C_{gs}+C_{ex} \tag{1}$$

where C_1 and L_1 are the high pass filter capacitance and inductor, respectively and $R_{eq}=g_{m1}L_s/C_t$.

3. Bias condition and linearity analysis

3.1. FBB technique analysis

A long-channel improvement mode n-MOSFET, where source, body and drain terminals are connected to ground is shown in Fig. 2. Consider an external voltage is connected to the gate terminal, which is initially zero. As V_{GS} becomes more positive, the holes in the P-substrate are repelled from the gate area, leaving negative ions behind so as to mirror the charge on the gate. In other words, a depletion region is created. Under this condition, no current flows because no charge carries are available. As V_{GS} increases, so do the width of the depletion region and the potential at the oxide–silicon interface. When the interface potential reaches a sufficiently positive value, electrons flow from the source to the interface and eventually to the drain. Thus a channel of charge carriers is formed under the gate-oxide between source and drain, and the transistor is turned on. We also say the interface is inverted. The value of V_{GS} for which this occurs is called threshold voltage, V_{th} [11].

The biggest problem with a low voltage design is the limitation of the V_{th}, since it is not expected to decrease much below what is available today [12].

FBB technique is introduced to solve this limitation problem and further reduce V_{th}. The threshold voltage of MOSFET equation is well-known as

$$V_{th}=V_{th0}+\gamma(\sqrt{2\phi_F-V_{BS}}-\sqrt{2\phi_F}) \tag{2}$$

where V_{th0} is the value of V_{th} with $V_{BS}=0$, γ is the bulk threshold parameter and φ_F is the strong inversion surface potential of the NMOS. According to the above equation, increasing the V_{BS} can reduce the V_{th}, which can reduce the power supply and power consumption. The junction between body and source is reversed-biased or zero-biased mode. If bulk voltage becomes positive than the source voltage, V_{BS} becomes positive; therefore, the threshold voltage can be reduced. The V_{BS} should be set as high as possible, but there is a limit to the amount of the V_{BS}, which can be applied due to CMOS latch up. The lower limit for the V_{th} is set by the amount of off-state or leakage current (due to standby power considerations in static circuits including the latch up) [3].

Fig. 3 shows the latch up current versus forward bias voltage. The latch up current is relatively low when forward biased source-substrate is below 0.4 V [13].

3.2. Linearity analysis

The main source of nonlinearity in a LNA is the nonlinear trans-conductance g_m due to nonlinear I_{ds}–V_{gs} relation [15]. The transfer function of a short-channel transistor can be expressed as follows [16]:

$$i_{ds}=K\frac{x^2}{1+\theta x} \tag{3}$$

$$x=2\eta\phi_t\,Ln\left(1+\exp\left(\frac{V_{gs}-V_{th}}{2\eta\phi_t}\right)\right) \tag{4}$$

V_{gs} is the gate-source voltage, i_{ds} is the drain-source current, φ_t is the thermal voltage KT/q, $K=0.5\,\mu_o C_{ox}W/L$, and θ is the normal field mobility degradation factor. η is the rate of exponential increase of drain current with gate-source voltage in sub-threshold region and the size of the moderate inversion region. Taylor series expansion of voltage–current characteristic can be

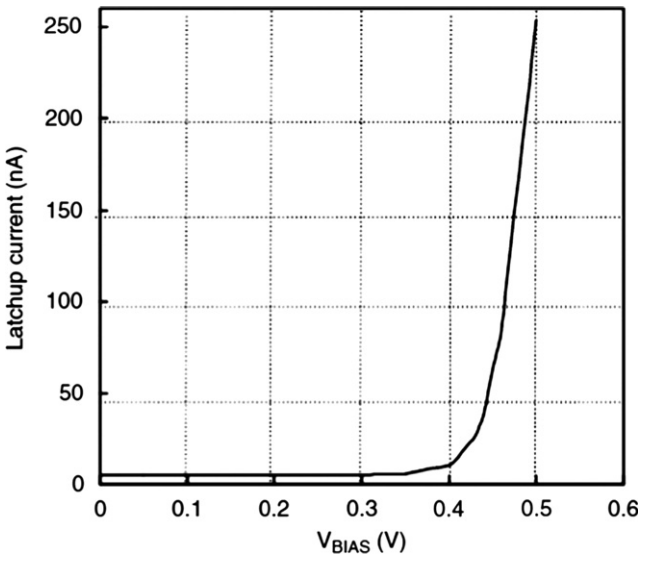

Fig. 3. Latch up current relation to source-substrate forward-biased voltage [13].

described as follows:

$$i_{ds} = g_{m1}v_{gs} + g_{m2}v_{gs}^2 + g_{m3}v_{gs}^3 + \dots \quad (5)$$

where g_{m1} is the main trans-conductance of the MOSFET, g_{m2} is the second-order nonlinear coefficient obtained by the second-order derivative of the DC transfer characteristic, and g_{m3} is the third-order nonlinear coefficient obtained by the third-order derivative of the DC transfer characteristic. The coefficients of the above equation can be given by [17]

$$g_{m1} = \frac{\partial I_D}{\partial V_{gs}} \quad (6)$$

$$g_{m2} = \frac{1}{2}\frac{\partial^2 I_D}{\partial V_{gs}^2} = \frac{1}{2}\frac{\partial g_{m1}(V_{gs})}{\partial V_{gs}} \quad (7)$$

$$g_{m3} = \frac{1}{6}\frac{\partial^3 I_D}{\partial V_{gs}^3} = \frac{1}{3}\frac{\partial g_{m2}(V_{gs})}{\partial V_{gs}} \quad (8)$$

Fig. 4 shows a CPP topology which is chosen to improve the linearity of CMOS LNA. According to the above equations, the transfer functions of the PMOS and NMOS transistors are described as follows:

$$i_p = -g_{m1p}v_{gs} + g_{m2p}v_{gs}^2 - g_{m3p}v_{gs}^3 + \dots \quad (9)$$

$$i_n = g_{m1n}v_{gs} + g_{m2n}v_{gs}^2 + g_{m3n}v_{gs}^3 + \dots \quad (10)$$

As can be seen in Fig. 4

$$i_{out} = i_n - i_p = (g_{m1n} + g_{m1p})v_{gs} + (g_{m2n} - g_{m2p})v_{gs}^2 + (g_{m3n} + g_{m3p})v_{gs}^3 \quad (11)$$

More attention has been given to the third-order nonlinear term, which is the main contribution of nonlinearity. The third-order IP3 products exist at four frequencies: $(2f_1 - f_2)$; $(2f_2 - f_1)$; $(2f_1 + f_2)$; and $(2f_2 + f_1)$. The last two terms are located at a high frequency and are out of the frequency range and can be neglected. The two first terms are located in the band of interest. Fig. 5 shows the simulated drain current and its derivatives with respect to V_{GS} for NMOS and PMOS transistors operating in the strong inversion region. The third-order nonlinear coefficient of NMOS and PMOS transistors are shown in Fig. 6. As can be seen from it, gate bias voltages and sizes of the transistors are chosen such to align the positive peak of the PMOS transistor with the negative peak of the NMOS one, resulting in the g_{m3} will be close to zero.

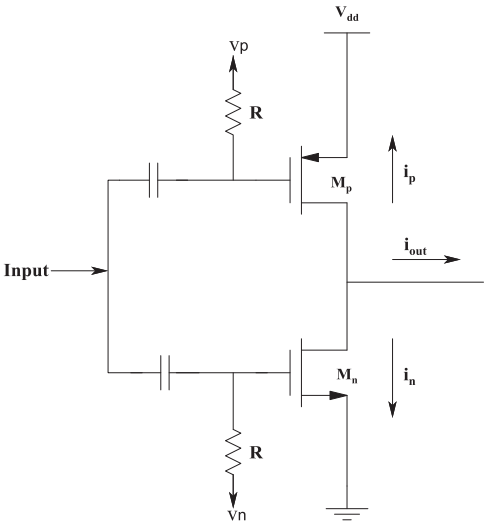

Fig. 4. Complementary push–pull topology.

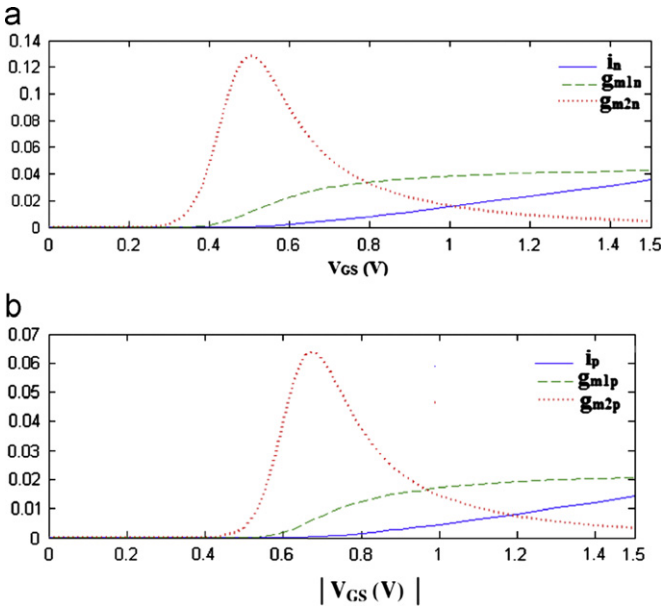

Fig. 5. (a) Simulated i_n, g_{m1n} and g_{m2n} for NMOS and (b) simulated i_p, g_{m1p} and g_{m2p} for PMOS.

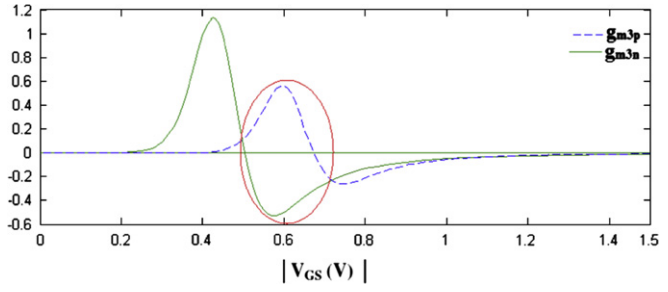

Fig. 6. Simulated third-order nonlinear coefficients for NMOS and PMOS transistors.

The IIP3 of a nonlinear device is as follows [18]:

$$\mathrm{IIP3} = \sqrt{\frac{4}{3}\left|\frac{g_{m1}}{g_{m3}}\right|} \quad (12)$$

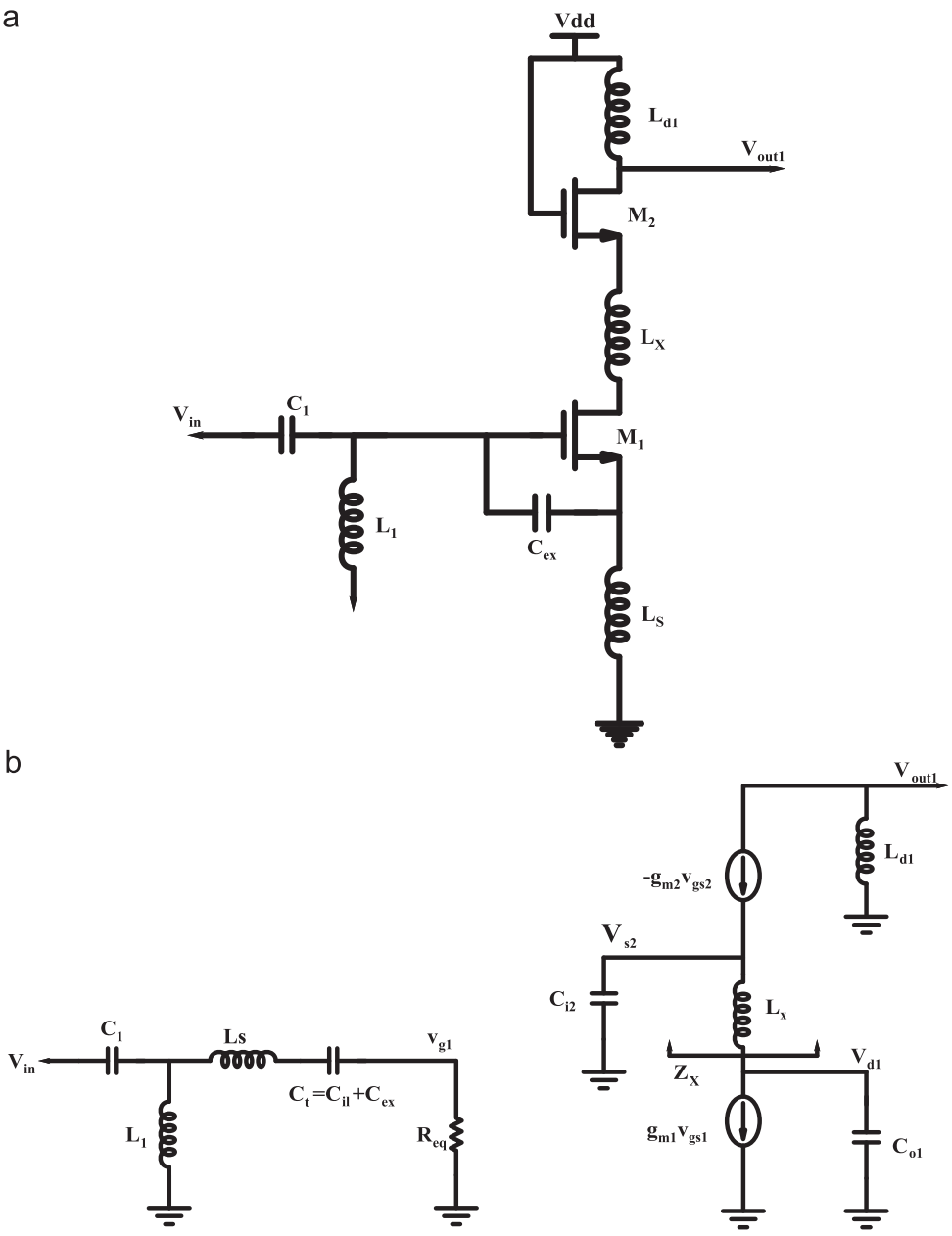

Fig. 7. (a) Schematic of cascode topology with series and shunt peaking inductors and (b) small signal model of a cascode topology for gain calculation.

By using CPP configuration and choosing appropriate gate voltages and sizes of transistors, IIP3 of the LNA can be improved. With a simple analysis, the proposed technique can boost g_{m1} (see Fig. 5) and reduce g_{m3} (see Fig. 6). Therefore, CPP technique can highly improve the LNA linear performance in the frequency range.

4. Gain and noise analysis

4.1. First stage gain analysis

Fig. 7(a) shows the circuit of cascode topology with series peaking inductor (L_x). Fig. 7(b) shows the small signal model at high frequencies that is suitable for calculating the total voltage gain as follows:.

$$\frac{V_{out1}}{V_{g1}} = \frac{V_{s2}}{V_{g1}}\frac{V_{d2}}{V_{s2}} \tag{13}$$

where $V_{d2} = -g_{m2}V_{gs2}L_{d1}s$ and V_{s2}/V_{g1} is calculated by multiplying the V_{s2}/V_{d1} and V_{d1}/V_{g1} which is expressed as follows:

$$\frac{V_{d2}}{V_{s2}} = \frac{-g_{m2}V_{gs2}L_{d1}S}{V_{s2}} \tag{14}$$

$$\frac{V_{s2}}{V_{d1}} = \frac{1}{S^2L_xC_{i2} + SL_xg_{m2} + 1} \tag{15}$$

$$\frac{V_{d1}}{V_{g1}} = -g_{m1}\left(Z_x \| \frac{1}{SC_{o1}}\right) \tag{16}$$

where Z_x is the impedance that can be seen from the drain of CS in cascode topology (shown in Fig. 7(b)) and approximately can be given as

$$Z_x \approx SL_x + \frac{1/g_{m2}}{1 + S(C_{i2}/g_{m2})} \tag{17}$$

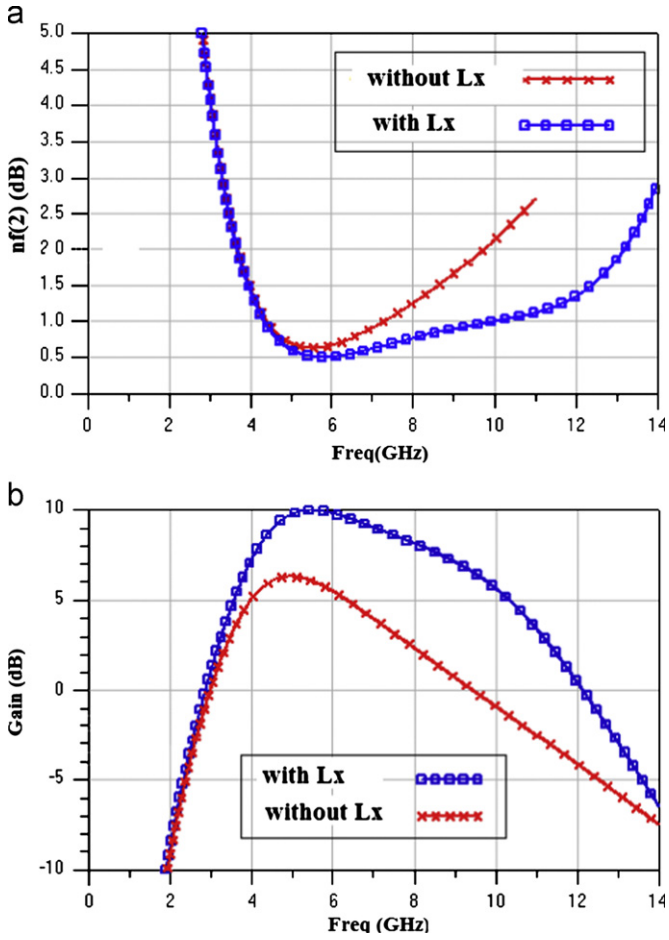

Fig. 8. (a) Effect of L_x on the first stage noise figure and (b) effect of L_x on the first stage gain.

The total voltage gain G_F of the first stage is given as follows:

$$G_F = \frac{V_{out1}}{V_{g1}} = -g_{m1}\frac{1}{1+sZ_xC_{o1}}\frac{1}{1+S(C_{i2}/g_{m2})} \tag{18}$$

As can be seen from (18), first stage voltage gain has a pole at $f_0=g_{m2}/2\pi C_{i2}$. Due to L_x, Z_x has inductive behavior and resonate with C_{o1} (shown in Fig. 7(b)) at high frequencies, resulting a peaking in gain frequency response. Fig. 8 shows cascode gain and noise figure with and without L_x versus frequency. Without L_x, G_F has a gain roll-off in the middle of frequency range. By inserting L_x, the gain roll-off disappears in the frequency range. Thus, the value of L_x is chosen to minimize the gain roll-off and increase the first stage gain, in order to reduce the noise of cascode topology in the band of interest.

4.2. Noise analysis

4.2.1. Sources of noise

The generic small signal model of a cascode topology with noise sources is shown in Fig. 9. Four sources of noise have been considered: the thermal noise of source resistance ($i_{n,Rs}$), thermal noise of the channel current ($i_{n,d}$), the gate-induced current noise ($i_{n,g}$), and the thermal noise of the output resistance ($i_{n,out}$). The Power Spectral Densities (PSDs) of $\overline{i^2_{n,Rs}}$ and $\overline{i^2_{n,Rout}}$ are as follows:

$$\overline{i^2_{n,\ Rs}} = 4KT\frac{1}{R_s}\Delta f \tag{19}$$

$$\overline{i^2_{n,\ Rout}} = 4KT\frac{1}{R_{out}}\Delta f \tag{20}$$

where T is the absolute temperature in Kelvin, Δf is the noise bandwidth in Hertz and K is the Boltzmann constant.

The PSDs of channel current thermal and gate-induced noises are given by [19,20]

$$\overline{i^2_{n,d}} = 4KT\gamma g_{d0}\Delta f \tag{21}$$

$$\overline{i^2_{n,g}} = 4KT\delta g_g\Delta f \tag{22}$$

where g_g is the equivalent shunt gate conductance, which is given by [19]

$$g_g = \frac{(\omega\ C_{gs})^2}{5g_{d0}} \tag{23}$$

where g_{d0} is the drain conductance for zero drain-source voltage and γ is a technology-dependent parameter and has a value of around 2/3 for long-channel devices in saturation region (in short channel devices γ is larger and its value is between 2 and 3) [21]. δ is the gate noise coefficient and is also a technology-dependent parameter. Its value is 4/3 for long channel devices and is augmented by a factor of 2 in short channel devices.

4.2.2. Output noise of the first stage

The input impedance of the cascode topology using inductively degenerated technique has been expressed by Eq. (1). The input impedance should be equal to the source impedance, R_s, and it can be expressed as

$$Z_{in} = g_m\frac{L_s}{C_t} = R_s = 50 \tag{24}$$

The quality factor of input circuit is then

$$Q = \frac{1}{(R_s+g_m(L_s/C_t))\omega_0C_t} = \frac{1}{2R_s\omega_0C_t} \tag{25}$$

where ω_0 is the resonance frequency of input matching network.

The output noise ($i_{n,out}$) of four noise sources (shown in Fig. 9) at ω_0 is as follows:

$$i_{n,\ out,\ Rs} = \frac{g_m}{j2\omega_0C_t}i_{n,\ Rs} \tag{26}$$

$$i_{n,\ out,\ Rout} = i_{n,\ Rout} \tag{27}$$

$$i_{n,out,d} = \frac{1}{2}i_{n,d} \tag{28}$$

$$i_{n,out,g} = \frac{g_m}{j\omega_0C_t}\frac{jR_s\omega_0C_t-1}{j2R_s\omega_0C_t}i_{n,g} \tag{29}$$

Now the correlation coefficient between $i_{n,g}$ and $i_{n,d}$ is given by [22,23]

$$c = \frac{i_{n,g}.i^*_{n,d}}{\sqrt{\overline{i^2_{n,g}}.\ \overline{i^2_{n,d}}}} \tag{30}$$

For a long channel device, $c=-0.395j$, and its magnitude decreases as the channel length scales down [19].

The PSD of output current due to $i_{n,g}$ and $i_{n,d}$ can be calculated as

$$\begin{aligned}\overline{i^2_{n,\ out,g+d}} &= \overline{(Hi_{n,g}+Ki_{n,d})(Hi_{n,g}+Ki_{n,d})^*}\\ &= |H|^2\overline{i^2_{n,g}}+|K|^2\overline{i^2_{n,d}}+HK^*\overline{i_{n,g}.i^*_{n,d}}+H^*K\overline{i^*_{n,g}.i_{n,d}}\end{aligned} \tag{31}$$

where, K and H are the transfer function of (28) and (29), respectively. The last two terms are output noise due to correlation and can be re-expressed by using (28)–(30) as follows:

$$\begin{aligned}\overline{i^2_{n,\ out,c}} &= (jcHK^*-jcH^*K)\sqrt{\overline{i^2_{n,g}}.\ \overline{i^2_{n,d}}}\\ &= \frac{g_m.c}{2\omega_0C_t}\sqrt{\overline{i^2_{n,g}}.\ \overline{i^2_{n,d}}}\end{aligned} \tag{32}$$

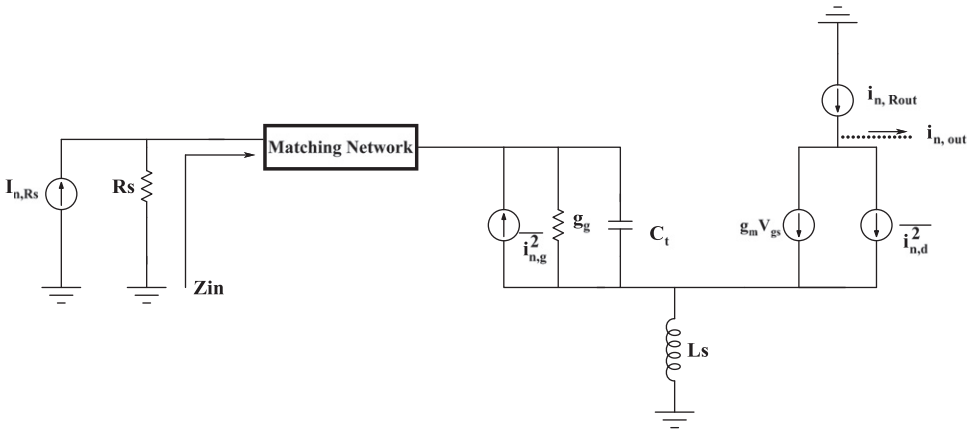

Fig. 9. Small signal model of a cascode topology with inductively degenerated and noise sources.

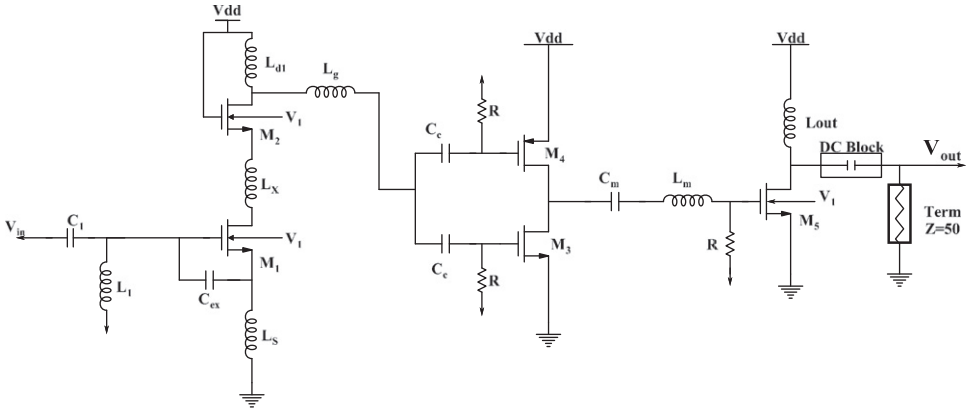

Fig. 10. Proposed CMOS LNA circuit, (buffer is not shown).

By using (25), the total noise factor of cascode topology at ω_0 is calculated as follows:

$$F_{first\ stage} = \frac{\overline{i^2_{n,out,Rs}} + \overline{i^2_{n,out,d}} + \overline{i^2_{n,out,g}} + \overline{i^2_{n,out,Rout}} + \overline{i^2_{n,out,c}}}{\overline{i^2_{n,out,Rs}}} \tag{33}$$

After simplification of the above equation, it can be re-expressed as follows:

$$F_{first\ stage} = 1 + \frac{g_{g1}(Q^2+1/4)P^2\ \ (g_m^2/g_{dn}) + \gamma_1(g_{dn}/4) + \sqrt{(\gamma_1 g_{g1}/4)}\, cPg_m + 1/R_{out}}{R_s Q^2 g_m^2} \tag{34}$$

$$P = \frac{C_{gs}}{C_t} \tag{35}$$

$$g_{dn} = \gamma g_{d0} \tag{36}$$

The long-channel values for g_{g1} and γ_1 are 8/45 and 1, respectively. Parameter P always is less than unity, because C_t always is greater than C_{gs} due to an additional capacitance (C_{ex}).

According to Friis equation, the total noise factor of the designed CMOS LNA is as follows:

$$F_{total} = F_{first\ stage} + \frac{F_{subsequent} - 1}{G_F} \tag{37}$$

where, $F_{first\ stage}$ is the noise factor of the cascode topology, $F_{subsequent}$ is the noise factor of the subsequent stages of LNA, and G_F is calculated in Eq. 18. Therefore, due to high G_F, the dominant noise source of the LNA is the first stage noise. For this reason, NF is minimized at the first stage by using source inductive degeneration and inserting L_x. According to Eq. 34, it can be seen that by increasing g_m, F (or NF in dB) of the first stage can be improved.

5. Design considerations

In a receiver path, as the signal propagates from the antenna to digital back-ends, different blocks may introduce noise to the signal. The overall NF of the receiver depends on the NF of each block as well as the gain of preceding stages. Intuitively, larger signals are less susceptible to noise, and this is why the large gain of one stage makes the noise of the following stage less important.

Consequently the two major requirements for the LNA performance are low noise figure and high gain. The main contribution of the noise of an LNA is the first stage noise; therefore, a cascode topology with peaking techniques (series and shunt techniques) are chosen as the first stage to achieve high gain and low noise figure. The proposed LNA is shown in Fig. 10. A series peaking inductor (L_x) is inserted between M_1 and M_2 to resonate with output parasitic capacitors of CS (M_1) and input capacitors of common gate (M_2) in the desired frequency range, in order to compensate the plausible gain roll-off of the cascode and reduce the first stage NF.

L_{d1} is chosen as the shunt peaking inductor to resonate with the total output parasitic capacitors of M_2 at the vicinity of 3.1 GHz to boost the first stage gain. To reduce the losses of the input impedance matching network, a high pass filtering structure is chosen and an external capacitor (C_{ex}=0.11 PF) is placed in

parallel with the gate-source capacitor of the input transistor to add a flexibility to the noise performance of the transistor. The series peaking inductor (L_g) is placed between first and second stages to improve the gain roll-off of cascode topology at the middle of the frequency range. The coupling capacitors (C_c and C_m) at high frequencies are ideally shorted and allow the RF signal transmits from the first stage to the second stage.

At the second stage a CPP structure and multiple gate configurations are used to improve the IIP3 of the CMOS LNA. The complementary characteristic of NMOS and PMOS transistors is used to enhance the linearity of the proposed UWB LNA circuit [24]. L_m is connected between the CPP topology and CS configuration to resonate with the output parasitic capacitors of M_3 and M_4 and input parasitic capacitors of M_5 to extend the bandwidth and compensate the LNA gain roll-off at the high frequencies. At the third stage a CS topology is chosen to improve the total gain of the LNA and L_{out} is designed to resonate with the total output capacitors of M_5 at the vicinity of the 10.6 GHz to compensate the gain roll-off of M_3 and M_4. However, supplying cascode topology typically requires a high voltage to bias both stages, subsequently increasing power consumption [25]. To solve the high power supply of cascode type, a FBB technique has been chosen to reduce the V_{th} and power consumption of the cascode topology.

6. Simulation results and discussions

The designed circuit of Fig. 10 is simulated with Agilent Advanced Design System (ADS) tools in 0.13 μm CMOS process. M_1, M_2, M_3, M_4, and M_5 sizes are set to $W_1=220$ μm, $W_2=220$ μm, $W_3=126$ μm, $W_4=130$ μm, and $W_5=50$ μm, respectively. For input impedance matching network, the high pass filter inductors L_1 and L_S are set to 1 nH and 0.512 nH, respectively.

Inter-stage inductors, L_g and L_m are set to 1.3 nH and 1.4 nH. L_{d1} and L_{out} are set to 3.1 nH, 1.57 nH, respectively. Using a low-voltage supply of 0.6 V, the proposed LNA power consumption is 4.1 mW (without buffer). This latter is low for a CMOS LNA in wireless applications. Fig. 11 shows the effect of L_g and L_m on the gain frequency response of the designed amplifier. Therefore, the results show the important role of these inductors in enhancing the gain and bandwidth of the proposed circuit at high frequencies. Output return loss (S_{22}) is less than -10.6 dB which are illustrated in Fig. 12. Gain response of the LNA (without buffer gain) and input return loss (S_{11}) are shown in Fig. 13. Maximum gain is 21 dB in band of interest and S_{11} is better than -5 dB from 4.9 to 12.1 GHz.

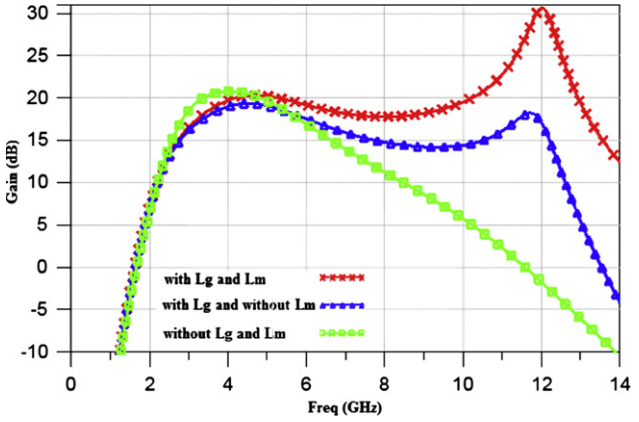

Fig. 11. Effect of L_g and L_m on the gain response of the LNA.

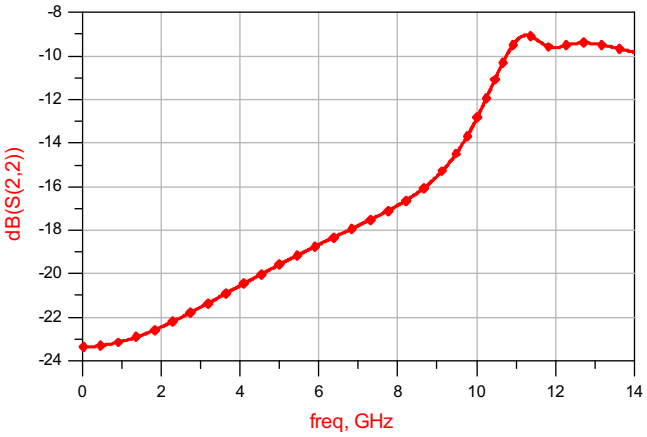

Fig. 12. S_{22} of the proposed circuit.

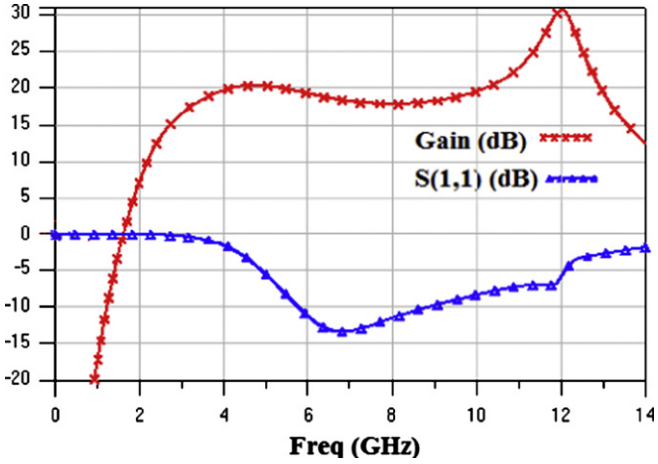

Fig. 13. Gain response and S_{11} of the CMOS LNA.

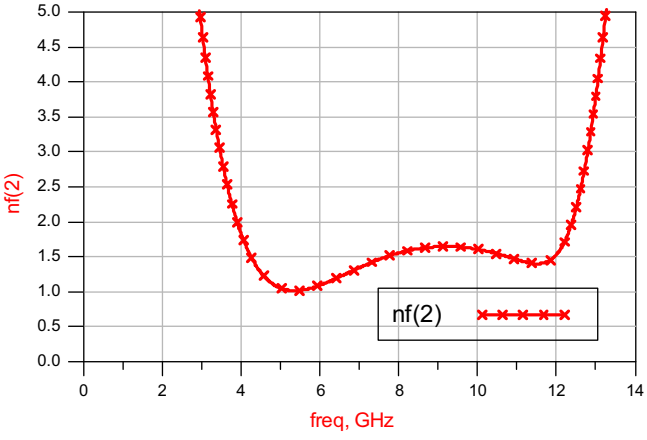

Fig. 14. Noise figure characteristic of the CMOS LNA.

Fig. 14 clearly shows that the designed LNA achieves a noise characteristic below than of 1.7 dB from 4 to 10.6 GHz which is a good candidate for wideband low noise application.

The two tone test was performed for intermodulation distortion with 1 MHz spacing for IIP3 simulation with ADS tools. Fig. 15(a) shows the simulated IIP3. The simulated third-order input intercept point of the designed LNA is shown versus different frequencies in Fig. 15(b).

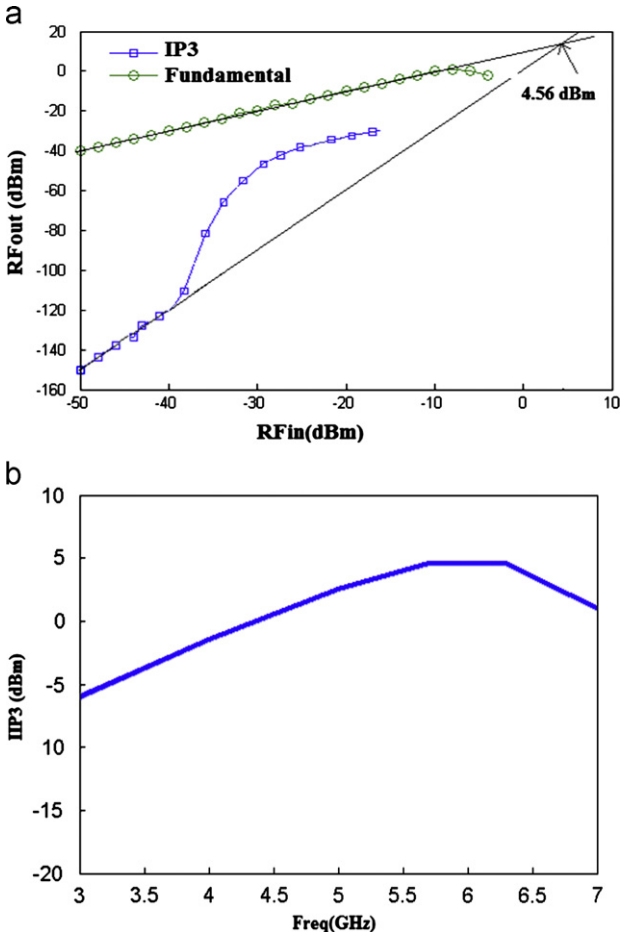

Fig. 15. (a) Simulated IIP3 of the proposed circuit and (b) simulated IIP3 versus different frequencies.

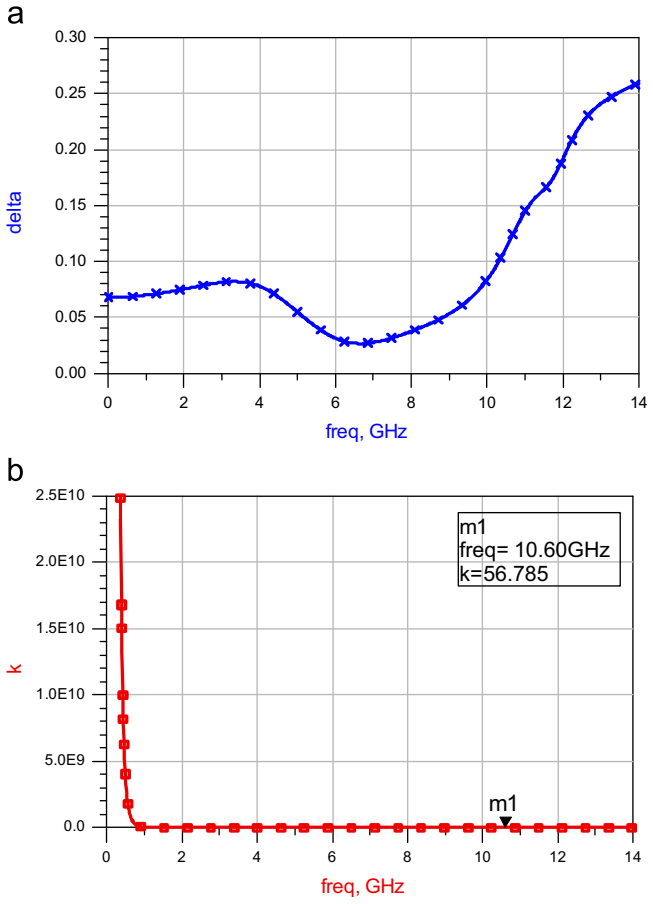

Fig. 16. Unconditional stable and stability factor *K*.

The stability of a LNA is the important requirement. The stability factor (K) is a popular measure of circuit stability [26]. If $K>1$ and $|\Delta|<1$, the amplifier is unconditionally stable meaning the LNA will be stable under any load condition. The value of K and $|\Delta|$ are obtained as follows [27]:

$$K=\frac{1-|S11|^2+|S22|^2+|S11\times S22-S12\times S21|^2}{2|S12\times S21|}>1 \quad (38)$$

$$|\Delta|=|S11\times S22-S12\times S21|<1 \quad (39)$$

The K factor and $|\Delta|$ of the designed LNA are shown in Fig. 16. Table 1 gives the characteristics of the proposed UWB CMOS LNA compared to the recently published works.

Table 1
Comparison of the simulated results of the designed CMOS LNA and recently published works.

Ref.	[4][a]	[7]	[9]	[23]	[25]	This work
Tech (μm)	0.25	0.18	0.18	0.18	0.18	0.13
BW (GHz)	2.1	5.5	3.1–10.6	2.4	3.1–10.6	3.1–10.6
Power(mW)	25	1.98	33.2	2.7	33.66	4.1
S_{21} (dB)	16.4	20.5	16 ± 0.8	11.2	11.7 ± 0.4	19.5 ± 1.5
S_{22} (dB)	−18.8	−21.3	<-13	–	<-9.5	<-10.6
S_{12} (dB)	−33.4	<-48	–	<-60	–	<-70.6
NF (dB)	2.77	1.8–2.6	3.1-5.7	2.15–2.7	5.8–6.7	1–3.9
IIP3 (dBm)	7.45	−6.2	–	−6.5	–	4.56

[a] Differential.

7. Conclusion

A three-stage CMOS low noise amplifier (LNA) was proposed using a cascode topology for its high gain and low noise figure at the first stage. At the second stage a complementary push–pull topology was used to enhance the linearity performance. A simple common source topology was used to increase the total gain of the proposed LNA as the third stage. Forward Body-Biased technique was chosen to reduce the threshold voltage, power supply and as well power consumption of the LNA.

A high pass filtering structure with source inductive degeneration technique was employed to reduce the number of inductors; therefore, reduces the die area and the noise figure of the designed circuit. The proposed UWB CMOS LNA is a good candidate for UWB wireless applications due to its low voltage and low power consumption.

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References

[1] Yi-Jing Lin, S.H. Hsu, Jun-De Jin, C.Y. Chan, A 3.1–10.6 GHz ultra-wideband CMOS low noise amplifier with current-reused technique, IEEE Microw. Wireless Components Lett. 17 (3) (2007).

[2] H.L. Kao, K.C. Chang, Very low-power CMOS LNA for UWB wireless receivers using current-reused topology, Science-direct 2007 Elsevier Ltd, Solid-State Electrochem. 52 (2008) 86–90.

[3] Gh.R. Karimi, S. Babaei Sedaghat, Ultra low voltage, ultra low power low noise amplifier for 2 GHz applications, Int. J. Electron. Commun. 66 (2012) 18–22.

[4] Li En-ling, Song Lin-hong, Yang Dang-qiang, Xue Ying, C.H.U. Meng, Design of 2.1 GHz CMOS low noise amplifier, J. China Univ. Post Telecommun. 13 (1) (2006) 71–74.

[5] Andrea Bevilacqual, M. Niknejad, An Ultra-wideband CMOS LNA for 3.1–10.6 GHz wireless receivers, ISSCC 2004/session 21/rf potpourri/21.3.

[6] Dake Wu, Ru Huang, Waisum Wong, Yangyuan Wang, A 0.4 V low noise amplifier using Forward Body Bias technology for 5 GHz application, IEEE Microw. Wireless Components Lett. 17 (7) (2007) 543–545.

[7] S. Toofan, A.R. Rahmati, A. Abrishamifar, G. Roientan Lahiji, Low power and high gain current reuse LNA with modified input matching and inter-stage inductors, Microelectron. J. 39 (2008) 1534–1537.

[8] Abdelhalim Slimane, M. Trabelsi, M.T. Belaroussi, A 0.9 V, 7 mW UWB LNA 3.1–10.6 GHz wireless applications in 0.18 μm CMOS technology, Microelectron. J. 42 (2011) 1263–1268.

[9] Y. Lu, K.S. Yeo, A. Cabuc, J. Ma, M. Do, Z. Lu, A novel CMOS low-noise amplifier design for 3.1–10.6 GHz ultra-wideband wireless receivers,, IEEE Trans. Circuits Syst. I: Regular Papers 53 (2006) 1683–1692.

[10] Yang Yi, Gao Zhang, Yang Liqiong, Huang Lingyi, Hu Weiwu, Design and analysis of a UWB low-noise amplifier in the 0.18 μm CMOS process, J. Semicond. 30 (1) (2009) 015001–015005.

[11] R. Behzad, Design of Analog CMOS Integrated Circuits, McGraw-Hill, New York, 2001.

[12] A. Srivastava, D. Govindarajan, A fast ALU design in CMOS for low voltage operation, J. VLSI Des. 14 (2002) 315–327.

[13] A. Srivastava, C. Zhang, An adaptive body-bias generator for low voltage CMOS VLSI circuits, Int. J. Distributed Sensor Networks 4 (2008) 213–222.

[14] Gh.R. Karimi, E. Nazari, An ultra low votage amplifier design using forward body bias folded cascade topology for 5 GHz application, in: Proceedings of the 5th IEEE Conference of ICIEA, 2010, pp. 1838–1842.

[15] A.I. Galal, R. Pokhrael, H. Kanaya, K. Yoshida, High linearity technique for ultra-wideband low noise amplifier in 0.13 μm CMOS technology, Int. J. Electron. Commun. 66 (2012) 12–17.

[16] M.T. Terrovitis, R.G. Meyer, Intermodulation distortion in current-commutating CMOS mixers, IEEE J. Solid-State Circuits 35 (2000) 1461–1473.

[17] Vladimir Aparin, Gary Brown, E. Larson. Linearization of CMOS LNA's via optimum gate biasing, in: Proceedings of the 2004 IEEE ISCAS International Circuit and System Symposium, vol. 4, 2004, pp. 748–751.

[18] A.I. Galal, R. Pokhrael, H. Kanaya, K. Yoshida, Linearization technique using bipolar transistor at 5 GHz low noise amplifier, Int. J. Electron. Commun. 64 (2010) 978–982.

[19] A. Nam-Jin, Low-power 3.1–10.6 GHz ultra-wideband CMOS low-noise amplifier with common-gate input stage, Curr. Appl. Phys. 11 (2011) 87–92.

[20] Trung-Kien Nguyen, Chuang-Hwan Kim, Gook-Ju Ihm, Moon-Su Yang, Sang-Gug Klee, CMOS low-noise amplifier design optimization technique, IEEE Trans. Microw. Theory Tech. 52 (5) (2004).

[21] K. Shaeffer Derek, T.H. Lee, A 1.5 V, 1.5vGHz CMOS low noise amplifier, IEEE J. Solid-State Circuits 32 (1997) 745–759.

[22] A. van der Ziel, Noise in solid state Devices and Circuits, Wiley, New York, 1986.

[23] S. Toofan, A.R. Rahmati, A. Abrishamifar, G. Roientan Lahiji, A low-power and high-gain fully integrated CMOS LNA, Microelectron. J. 38 (2007) 1150–1155.

[24] I. Nam, B. Kim, K. Lee, CMOS RF amplifier and mixer circuits utilizing complementary characteristics of parallel combined NMOS and PMOS devices, IEEE Trans. Microw. Theory Tech. 53 (2005) 1662–1671.

[25] C.C. Chen, Z.Y. Huang, C.C. Huang, N.K. Lu, Time constant compensated LNA for ultra-wideband receiver, in: Proceedings of the International Symposium on Intelligent Signal Processing and Communications Systems, 2005, pp. 13–16.

[26] M. Rajashekharaiah, Gain control and linearity improvement for low noise amplifier in 5 GHz direct conversion receivers. Master of Science Thesis, May 2005.

[27] G. Gonzalez, Microwave Transistor Amplifiers: Analysis and Design, 2nd ed., Prentice-Hall, Upper Saddle River, NJ, 1997.