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A metal-oxide-semiconductor radiation dosimeter with a thick and defect-rich oxide layer

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Abstract

Enhancing the density of defects in the oxide layer is the main factor in improving the sensitivity of a metal-oxide-semiconductor (MOS) radiation dosimeter. This paper reports a novel MOS dosimeter with a very thick and defect-rich oxide layer fabricated by MEMS technology. The category of defects in SiO_2 and their possible effect on the radiation dose sensing was analyzed. Then, we proposed combining deep-reactive-ion etching, thermal oxidation and low pressure chemical vapor deposition to realize an oxide layer containing multiple and large interfaces which can increase defects significantly. The trench-and-beam structure of silicon was considered in detail. The fabrication process was developed for obtaining a thick and compact MEMS-made SiO_2. Our devices were irradiated by γ-rays of ^{60}Co at 2 Gy per minute for 2 h and a thermally stimulated current (TSC) method was used to determine the readout of the dosimeters. Results show that there is a peak current of about 450 nA, indicating a total TSC charge of 158 μC and sensitivity of 1.1 μC mm^{-3}·Gy, which is 40 times the sensitivity of previous MOS dosimeters.

Keywords: MOS dosimeter, trench-and-beam structure, MEMS-made SiO_2, TSC, high sensitivity

(Some figures may appear in colour only in the online journal)

1. Introduction

Radiation is pervasive in daily life and radioactive environments such as laboratories, hospitals and nuclear power plants are quite common. Exposure to radiation exceeding a certain dose causes damage to health, as well as the malfunction of devices and machines [1]. Therefore, we usually need to detect the dose of radiation received by people or objects in areas such as space travel, medical care and environmental monitoring. Several kinds of dosimeters have been explored such as thermo luminescent dosimeters (TLDs) [2], semiconductor diodes [3] and optically stimulated luminescence dosimeters (OSDLs) [4]. However, most of them are not suitable for working in space, as they do not meet the requirements of being of low weight and small size, as well as able to work following exposure to high doses. The radiation in deep space is very high and effective dosimeters are required for future space missions [5].

The metal-oxide-semiconductor (MOS) dosimeter not only has the advantages of a wide dynamic range, but also high accuracy, a very simple structure, a small size, low price and is compatible with IC technology [6]. It is therefore one of the most promising space dosimeters. Its structure consists of an oxide layer over the silicon substrate, with metal layers on both side surfaces. The oxide layer is the critical component and determines the essential characteristics of MOS dosimeters. It has the diamond cubic crystal structure in which the Si atom shows tetrahedral coordination, with four oxygen atoms surrounding a central Si atom. The O atom coordinates with two silicon atoms, so that the defects within the structure are

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complex [7]. These defects can capture the holes excited by the radiation which has a strong impact on the electrical properties of MOS resulting in the radiation effect [8].

A theory of analyzing arbitrary distributed traps induced by radiation in oxide and semiconductors using thermally stimulated current (TSC) was provided by Simmons in 1973 [8, 9], laying the theoretical foundation of MOS dosimeters. This theory shows that if electrons and holes generated by light can be hold in traps, we can use the TSC method to measure the amount of trapped charges. Various radiation doses can generate different amounts of charge in oxide and semiconductors, so we can deduce the radiation dose by measuring the trapped charges using the TSC method. In 1985, Shanfield used TSC to measure the hole traps in an irradiated MOS and found the relationship between the trapped charge and radiation dose [10]. Then, Fleetwood simplified the model of defects and charges in MOS and proposed a new method combining *C*-*V* measurements and TSC to determine the amount of radiation induced charges in MOS [11, 12]. However, traditional MOS structure exhibits such small currents (i.e. ~pA), i.e. very low sensitivity, which makes the measurement difficult because the thermal oxide layer is very thin and compact, lacking defects to capture charges. To overcome this limit of thermal oxide and improve the performance, a new method is required to make a thick and defect-rich oxide layer. CVD SiO_2 such as LPCVD SiO_2 is a substitution for thermal oxide because it is rich in defects, but it brings high stress which makes the Si substrate fragile when the CVD layer is thick [13]. Since defects which act as hole traps like E' center usually appear where bonds break [14], creating more interfaces in the oxide can increase the defect density and the total captured charges further. We therefore propose combining DRIE, thermal oxidation and CVD to prepare our oxide layer with the purpose of increasing the interface defects. This combination also reduces the stress of CVD SiO_2 on substrate at the same time, which enables us to prepare very thick oxide.

This paper proposes a novel MOS dosimeter with a MEMS-made thick and defect-rich oxide layer to increase its ability to capture radiation-induced charges. The theory, design, fabrication and testing are presented in detail in the following sections. We prove that our MOS dosimeter can capture more charge and increase the sensitivity.

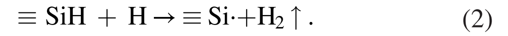
2. Theory and design

2.1. The defects in MOS

In the SiO_2/Si system, defects can be sorted by their location, such as SiO_2/Si interface defects and oxide traps [15]. Compelling evidence has associated interface traps with P_b centers, which are trivalent Si defects at the SiO_2/Si interface [16]. This trivalent Si defects are caused by lattice mismatchs between Si and SiO_2, and presented as single Si bonding dangled ($Si_3 \equiv Si\cdot$). The P_b centers can capture the holes whose Fermi level is lower than that of P_b and it can be expressed as [17]

$$P_b + \text{hole} \rightleftharpoons P_b^+. \tag{1}$$

For the extensive existance of H_2O, hydrogen is always contained in SiO_2, which can also lead the P_b centers. The dangled Si bond combines with hydrogen so that it is neutral at Si/SiO_2 interface. But the hydrogen is so rich that the two of hydrogen ions combine to form hydrogen gas and the rest of the silicon forms the P_b center as follows [18]:



$$\equiv \text{SiH} + \text{H} \rightarrow \equiv \text{Si}\cdot + \text{H}_2 \uparrow. \tag{2}$$

The oxide traps are formed at the process of deposition and are generally located within about 3 nm of the Si/SiO_2 interface called E' centers [19]. Feigl *et al* [20] identified the E' center observed in bulk silicon dioxides a weak Si–Si bond owing to an oxygen vacancy between two Si atoms, each back-bonded to three oxygen atoms ($O_3 \equiv Si\cdot$). The E' centers are one kind of hole traps and the process of capturing the holes is as below [21]:

$$\equiv \text{Si}\cdot\cdot\text{Si} \equiv + \text{hole} \rightarrow \equiv \text{Si}^+\cdot\text{Si} \equiv. \tag{3}$$

Lenahan *et al* found that the number of trapped holes in SiO_2 is almost as much as the number of E' centers, which indicates that the E' centers play a major role in the hole-capturing [17].

2.2. The carriers transport in MOS

There are predominantly three parts, made of three different kinds of materials, in MOS devices, such as the metal as front and back electrodes, SiO_2 as dielectric and silicon as substrate, in which carrier transportation is very different. In the electrode metal, it mainly relies on the free electrons, while in SiO_2 and Si it relies on both electrons and holes. The hole and electrons in Si have the same magnitude of the mobilities as $1350\,cm^2\,(V \cdot s)^{-1}$ and $480\,cm^2\,(V \cdot s)^{-1}$ respectively [22] so that most of the radiation-induced electrons and holes in Si will recombine quickly. In contrast, those in SiO_2 provide very low mobilities to $20\,cm^2\,(V \cdot s)^{-1}$ and $1 \times 10^{-5}\,cm^2\,(V \cdot s)^{-1}$ respectively [23]. Because the mobility of the electron is six orders of magnitude larger than that of the hole in SiO_2, electrons can be swept out of the oxide immediately by positive bias while holes will leave and move slowly toward the Si. If holes do not recombine with electrons during its moving process, they will be finally trapped by the defects in SiO_2 and Si/SiO_2 interface.

Figure 1 shows the carriers transport in MOS with positive bias on the metal gate. The electrons and holes induced by radiation will move towards the gate and Si/SiO_2 interface respectively. McLean and Hughes proposed that the holes hop to the Si/SiO_2 interface step-by-step and are trapped by defects in the SiO_2 [24]. The lattice potential is then changed by the trapped holes and it will impede the movement of holes. When the holes hop to the Si/SiO_2 interface, it will be finally trapped by defects nearby. These trapped holes add positive charges to the oxide and do not move under room temperature. They result in the shift in *C*-*V* curves of the MOS. But when the MOS is heated and given negative bias, these holes induced by radiation and captured by traps will be released at last,

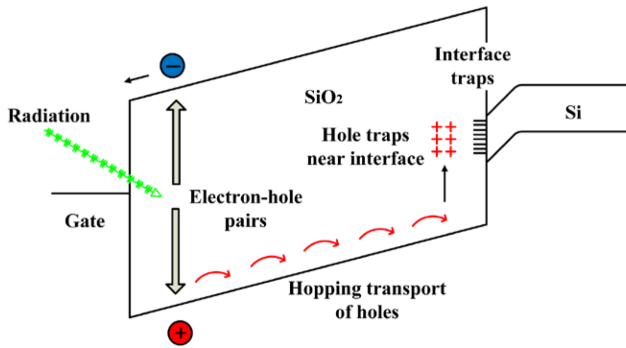


Figure 1. Energy band diagram and the holes transport in MOS with a positive gate bias.

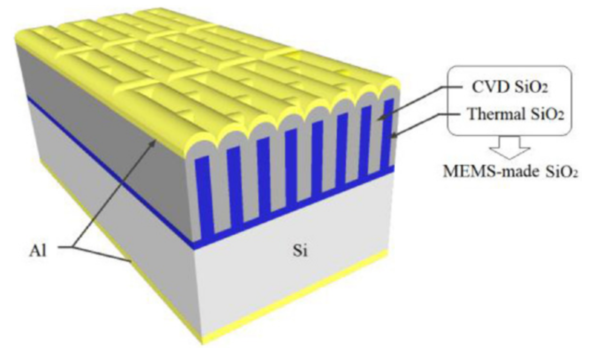


Figure 2. A three-dimension schematic view of the MOS dosimeter structure with MEMS-made SiO_2.

contributing to the most of TSC. By calculating the number of holes from the value of TSC and the relationship between the number of holes, the radiation dose will be obtained.

2.3. TSC method to calculate the number of trapped charges

The trap or defect in SiO_2 is a kind of micro-structure which is difficult to observe directly. In general, the TSC method has frequently been used to analyze their properties in semiconductors and insulators [25, 26]. In SiO_2 for example, the radiation stimulates the pairs of electron–holes and the defects trap the holes which are not recombined with electrons. When SiO_2 is heated to a certain temperature with an electric field applied to it, the holes trapped by defects will be released and can be collected by an ampere meter if it is not recombined during transportation. In theory, it is difficult to completely describe the TSC of distributed traps energy level and recombination center using equations with analytical solutions. Simmons and Taylor have proposed some assumptions and simplified models such as a single discrete trapping level, which is agreement with the experimental results. The formula (4) describes the relationship between current density and temperature of insulators with constant heating rate [27]:

$$J = \frac{1}{2} q L n_{t0} e_n \exp\left(-\frac{v \sigma_n N_c k T^2}{\beta (E_c - E_t + kT)} e^{(E_t - E_c)/kT} \right) \quad (4)$$

where q is the charge quantity of an electron, L is the thickness of the insulator, n_{t0} is the number of electrons in the trapping level positioned at an energy E_t, e_n is the emission coefficient for electrons out of the trap, v is the thermal velocity of an electron, σ_n is the capture cross section of the trap for electrons, N_c is the state density of conduction band, β is the constant heating rate in degrees per second, T is the temperature, k is the Boltzmann constant, E_t is the energy of the trap and E_c is the energy of conduction band.

When the defects have the single trapping level, there is usually a single peak in the *J-T* curve. If there are several trapping levels, the curve can be complicated. But we can still use the total charges collected to analyze trapped charges and trap density. So the TSC method can help us measure the number of trapped charges which are generated in SiO_2 by radiation.

Another method to calculated trapped charge is using *C-V* curves. *C-V* measurements are performed before and after radiation. We can calculate the shift in midgap voltage ΔV_{mg}. The total charge Q_{CV} can be calculated by

$$Q_{CV} = C_{ox} \times \Delta V_{mg} \quad (5)$$

where C_{ox} is the capacitance of oxide layer [28]. Fleetwood proposed models to calculate the trapped radiation-induced charge using both the TSC method and *C-V* characteristics [12]. His method can calculate both trapped positive and negative charges but the distribution of negative charge has to be determined beforehand to choose the appropriate model. The *C-V* method we use in this work is to judge the radiation effect and the number of charge induced by radiation is calculated by TSC.

2.4. The design of the defect-rich MOS

The oxide layer of MOS is the sensing part of radiation detector. In order to increase the sensitivity of radiation, enhancing the number and density of hole traps is the key. There are a great many hole traps such as P_b centers and E' centers located at or close to the SiO_2/Si interface. In addition, the SiO_2 grown in the hydrogen atmosphere can greatly increase the chance of bonding between Si and H, which is instable and can form the single Si bonding dangled ($Si_3 \equiv Si\cdot$). Furthermore, the SiO_2 deposited by LPCVD is not compact and must contain a lot of defects. Considering all the factors above, we proposed the MEMS-made oxide structure as a sensing part prepared by combining the processes of deep-reactive-ion etching (DRIE), thermal oxidation and low pressure chemical vapor deposition (LPCVD) (figure 2) [29]. The Si substrate will be etched by DRIE and then thermally oxidized forming thermal oxide pillars. Finally LPCVE SiO_2 will be used to fill the gaps between pillars. Between the thermal oxide and LPCVD SiO_2, the zigzag edge of the DRIE Si pillars can increase the interface area and also the defects as well resulting from the rough edge surfaces. This method makes it easy to achieve very thick SiO_2 because the thickness is mainly determined by the depth of DRIE Si. DRIE is adept in high aspect-ratio deep etching while it is very difficult to deposit thick SiO_2 for the thermal oxidization or LPCVD process. Therefore it can be deduced that this MEMS-made oxide layer will possess a much higher number of defects than ones which are simply thermal and LPCVD.

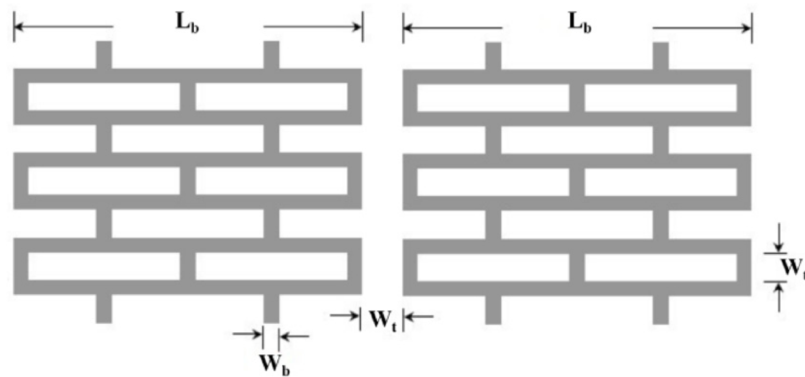


Figure 3. Schematic view of the trench-and-beam structure.

Our device structure is a simple MOS with Al electrodes on the sides of the MEMS-made oxide layer and silicon substrates (figure 2). The Si substrate is etched by DRIE to form a trench-and-beam structure (figure 3).The critical structure parameters include the length of the beam L_b, the widths of the beams W_b and the interval of the beams W_t. These parameters are closely related and depend heavily on the application and processing capability. The beam length L_b cannot be too long otherwise it will make the structure unstable. But if it is too short, it will increase the number of corners that are hard to oxidize. We chose 60 μm as a compromise according to a previous study [30]. Because the upper limit of our thermal oxidation process is 1 μm, we set the beam width W_b to be 1 μm. For the beams interval W_t, the narrower W_t is, the larger the area of interfaces that can be obtained. However there are two factors that should be considered first. One is the minimum line of our lithography machine of 1 μm. The other one is that Si pillars will widen two times after thermal oxidation. Therefore, we chose the beam interval W_t as 2 μm which determined the LPCVD SiO_2 should be at least 1 μm. In addition, it is very important that the groove-filling capability of LPCVD should be good, in order to achieve not only thick but also compact thermal and LPCVD double oxide layers. However, if the trench is too deep the opening would be sealed at first, and, by conformal deposition, leave the inside a void [30]. Therefore, RIE will be used to widen the opening just after DRIE so as to delay the opening sealing and reduce the chance of an air void appearing. We will experiment on different trench depths of 3 μm and 5 μm without pre-RIE and 4 μm ASE with 1 μm pre-RIE as a comparison.

3. Fabrication

The fabrication process started with an N type Si wafer of <100> orientation and 2–4 Ω·cm resistivity. The wafers in group A (figure 4 (left)) were directly etched by ASE to 3 μm and 5 μm in depth. The wafers in group B (figure 4 (right)) were firstly etched by RIE to 1 μm and then by ASE to 4 μm, thus making a trench 5 μm deep in total. Then 1 μm of thermal oxidation was carried on all wafers. After that, 2 μm of SiO_2 was deposited by LPCVD. The SiO_2 on the back side was wiped off by buffered hydrofluoric acid (BHF) and RIE.

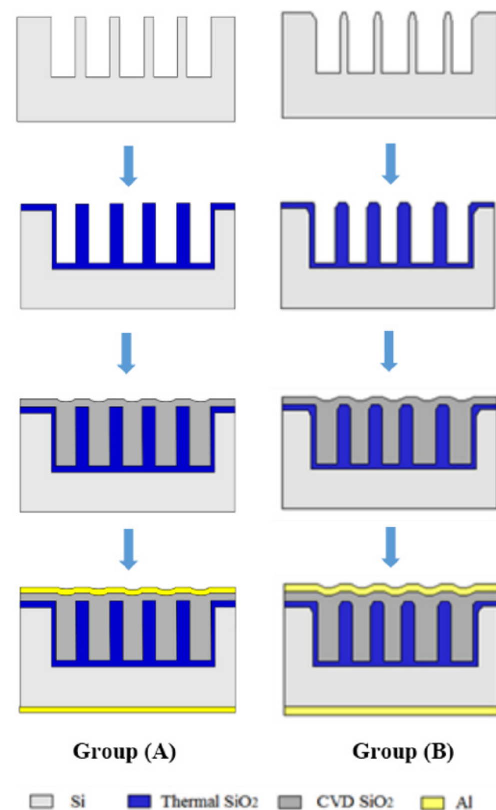


Figure 4. The fabrication process flow that creates a silicon oxide block. Group (A) is the beam-and-trench silicon structures etched by ASE only. Group (B) is the beam-and-trench silicon structures etched by RIE and ASE.

Then 1 μm of Al was sputtered on both sides of the wafers as electrodes. The whole wafer was diced to 3540 × 3570 μm dies as samples.

Figure 5 shows the SEM sectional views of three samples with different etching conditions in our work. We found that there are significant slits which are not filled by LPCVD SiO_2 (figure 5(a)) for ASE 5 μm sample but not for 3 μm one (figure 5(b)), i.e. that the trench depth of 3 μm was filled more compactly than the one of 5 μm. Jiang *et al* proposed that the sealing model of the trench occurs because the deposition rate on the top surfaces is higher than that on the sidewalls of the trench, hence the trench corner growing upward at an angle larger than 45° and air voids being formed in the sealed

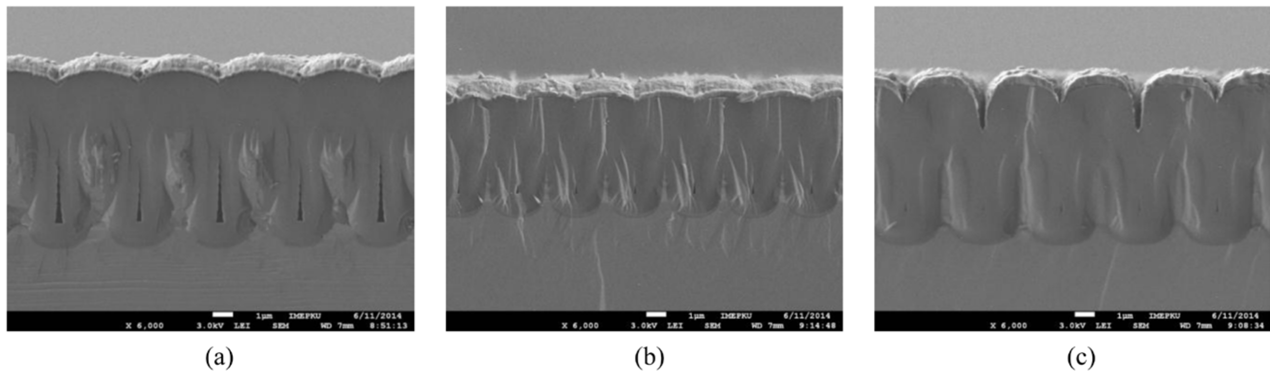


Figure 5. The SEM sectional views of samples: (a) etched by ASE to 5 μm, (b) etched by ASE to 3 μm, (c) etched by pre-RIE to 1 μm and ASE to 4 μm.

trenches [30]. From this point of view, it can be concluded that the deeper the trench, the larger the void is formed if the opening is the same. However, if the sample was firstly etched by RIE to 1 μm and then by ASE to 4 μm, there are very small slits (figure 5(c)), even smaller than those of ASE 3 μm samples. RIE not only widens the opening but also enlarges the convex angle of opening because it is isotopic. This can effectively delay the sealing of the opening. Our result shows that the combination of pre-RIE 1 μm and ASE 4 μm makes for the groove-filling ability of LPCVD and achieves the 5 μm compact MEMS-made oxide layer successfully.

4. Results and discussion

The device etched by pre-RIE 1 μm and ASE 4 μm was measured. Before this, it was mounted and the electrodes were wire-bonded to the pads on a socket. All devices were irradiated using the γ-rays of ^{60}Co at room temperature. The devices were irradiated with a 14 cm $\times$ 11 cm field at 2 Gy per minutes for 2 h in a positive bias of 1 V. The fading in thick oxide layer is very small with no bias on the gate [31], which was also proved by our observation. It is in fact well known that it is impossible to do TSC measurement correctly after the irradiation for a MOS dosimeter. We even had to delay the measurement several days because of the construction of the setup. Fading is unavoidable after irradiation. Therefore, the devices were laid in an ambient environment with no bias applied and we monitored the *C-V* every day in several days before TSC measurement. We did not observe a significant change of midgap voltage extracted from *C-V* so that it can be inferred that there is little fading in the MEMS-made SiO_2 dosimeter as is stated in [31]. Furthermore, it can evidently be speculated that this defect-rich MEMS-made SiO_2 has no increased fading at room temperature as a result of its very thick oxide structure made of 1 μm thermal oxide capped with at least 1 μm LPCVD oxide. The *C-V* characteristics were measured by an HP4192A LF impedance analyzer. Figure 6 shows the *C-V* curves before and after radiation. The left shift of *C-V* curve after the radiation indicated that there were positive charges accumulated in the oxide induced by the radiation.

Next the device was put into a furnace and the test was performed during the heating cycle. A schematic diagram of our

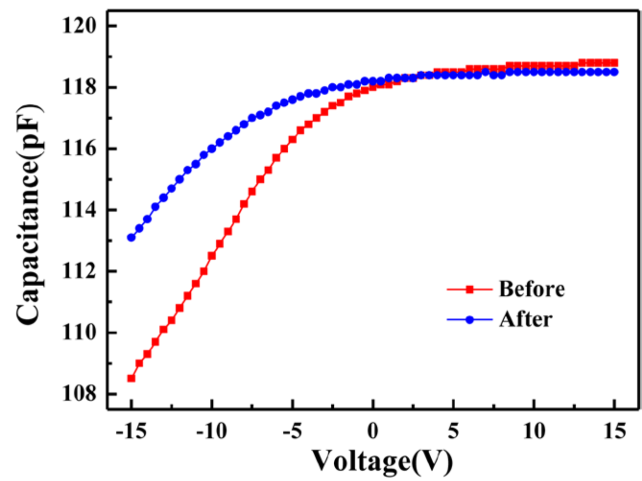


Figure 6. *C-V* curves before and after the radiation.

TSC system is shown in figure 7(a). The pads on the socket were connected independently through the hole of the oven to an HP4156B precision semiconductor parameter analyzer by wires which could endure the high temperature. All measurements shown here were taken in air because no difference has been found between TSC measurements made in nitrogen or air environments [28]. The device was under the negative bias of 1 V and heated to 120 °C at the rate of 2.55 °C min^{-1}. The temperature was monitored with a commercially available thermistor of Pt100 which was mounted near the devices as closely as possible. The data of time, temperature, and current were all taken once per second and transmitted to a computer. Figure 7(b) shows the device temperature as a function of the heating time during testing whose linearity is good. The nonlinearity between 0 min and 2.5 min occurs because the initial power had to overcome the thermal resistance of the furnace mass.

Figure 8 shows the TSC changed with the temperature. The total charges collected during measurement are obtained by numerically integrating the TSC with respect to the measuring time. There is a peak current of about 450 nA around 40 °C, indicating the total charge of 158 μC. For eliminating the size effect, the total charge was divided by the volume of the oxide to obtain the average charge density of 264 μC mm^{-3}. Then the sensitivity was calculated to be of 1.1 μC mm^{-3}·Gy, which

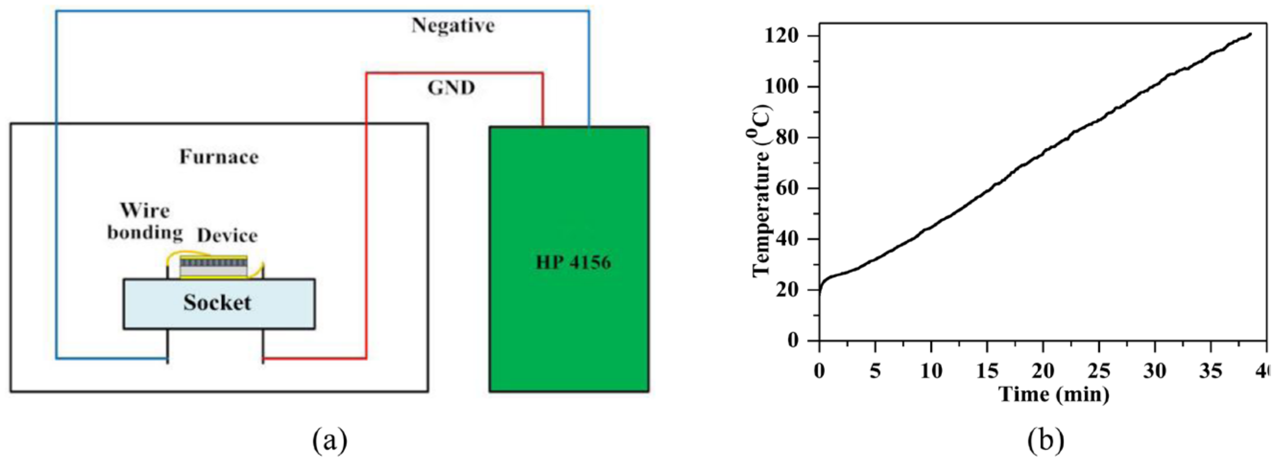


Figure 7. (a) Schematic diagram of the TSC system, (b) temperature versus time during the TSC measurement.

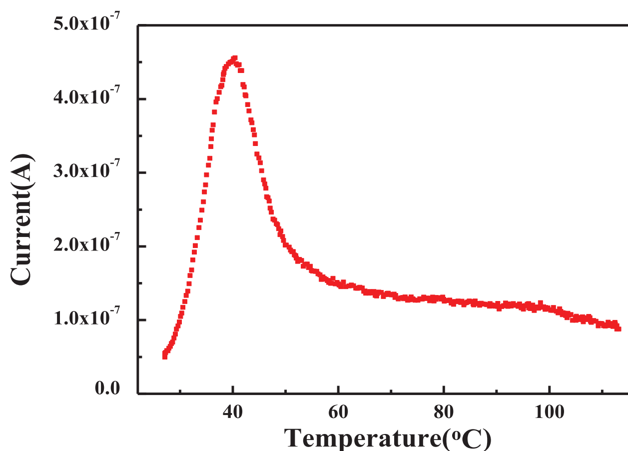


Figure 8. TSC versus temperature after the radiation.

is 40 times that of previous MOS dosimeters [11]. This demonstrates that our MEMS-made oxide layer can significantly improve the performance of MOS dosimeters.

5. Conclusion

We proposed a MEMS-made oxide structure prepared by a combined process of deep-reactive-ion etching (DRIE), thermal oxidation and low pressure chemical vapor deposition (LPCVD). This combined technique integrates several kinds of methods to increase the defects in oxide. First, it can form zigzag and rough multiple defect-rich interfaces between thermal and LPCVD SiO_2. Second, it utilize the relative loose LPCVD SiO_2 also containing numerous defects. Third, it can realize very thick SiO_2 easily to increase the defect number. The opening sealing ahead and inner voids left are the critical problem in this combined technique to prepare the thick SiO_2 layer. Experiments show that pre-RIE can effectively achieve the groove-filling ability of LPCVD, and the pre-RIE 1 μm and ASE 4 μm can achieve the 5 μm compact MEMS-made oxide layer successfully. At last, our devices were irradiated by γ-rays of ^{60}Co at 2 Gy per minute for 2 h. The TSC data reveals that there is a peak current about 450 nA, indicating a total TSC charge of 158 μC and sensitivity of 1.1 μC mm^{-3}·Gy, which is 40 times the sensitivity of previous MOS dosimeters. This demonstrates that the MEMS-made oxide layer can significantly improve the performance of MOS dosimeters. Evidently, this combined technique of DRIE, thermal oxidation and LPCVD did increase the number and density of defects in oxide, as expected. Comprehensive optimization of the trench-and-beam structure and process can advance the performance of this MOS radiation dosimeter further.

Acknowledgments

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