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RESEARCH ARTICLE

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A low-power voltage-controlled oscillator with phase noise suppressing techniques

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Abstract

A 0.5-V low-power VCO by using TSMC 0.18-μm CMOS process has been proposed. For achieving low phase noise and low power consumption, several techniques have been utilized. The forward body biasing technique can lower the supply voltage and power consumption. The noise filtering, feedback capacitors, and switched biasing technique can reduce the phase noise and power consumption. The PMOS transistors, which has lower flicker noise than the NMOS transistors, are used for further lowering the phase noise. The body-controlled cross-coupled pair is proposed for choosing the oscillation frequencies without using additional varactors, which lower the oscillation signal loss and phase noise. The measured results show the phase noise at 1 MHz offset frequency from the carrier signal is −118.6 dBc/Hz with $1/f^3$ corner frequency of 230 kHz while the control voltage is 0 V. The frequency tuning range is from 2.4 to 2.46 GHz under power consumption from 0.5 to 0.8 mW. The figure of merit at 1 MHz offset frequency from the carrier signal is −189 dBc/Hz.

KEYWORDS
CMOS, low phase noise, low power, VCO

1 | INTRODUCTION

Recently, low-power circuit design is a popular topic for extending the battery life of the portable devices. VCOs should lower phase noise (PN), power consumption (P_D), and cost. However, there exists a trade-of between these design parameters. For reducing PN and P_D, several techniques has been proposed.

Generally, the tail current source contributes the thermal and flicker noises, which corrupt the PN in a VCO.[1] Hence, the noise filtering technique has been proposed for reducing the thermal noise contribution of the tail current source at the second harmonics of the oscillation signals.[2] And feedback capacitors, which can increase the oscillation signal swing, are proposed. Moreover, a switched biasing technique is proposed for reducing the conduction time of the tail current sources.[3,4] The proposed noise filtering, feedback capacitors, and switched biasing technique can reduce PN under low P_D.

Moreover, a body-controlled cross-coupled pair is proposed as varactors for reducing the fixed capacitance of the LC tank.[5] Besides, a forward body biasing technique has been utilized for lowering the threshold voltage V_T, supply voltage (VDD) and P_D. And the PMOS transistors, which have lower flicker noise, are used in the entire VCO for reducing PN.

2 | CIRCUIT ARCHITECTURE AND DESIGN CONSIDERATION

The schematic of the proposed VCO is shown in Figure 1. The body-controlled cross-coupled pair (M_1-M_2) generates a negative impedance and resonates with L_1 for a stable

oscillation. M_1 and M_2 can be reused as varactors for altering the oscillation signal frequency. The output buffers (L_3, L_4, C_6, C_7, M_5, and M_6) are used for isolating the loading effects from next stages. For reducing V_T, VDD and P_D, the transistors in this circuit are used the forward body biasing technique.[6] The body voltage V_P of the transistors in the proposed VCO is 0.1 V for reducing V_T as 0.4 V. The noise filter (L_2, L_3, and C_1), feedback capacitors (C_2 and C_3), and switched biasing technique (C_4, C_5, M_3, and M_4) are the proposed for suppressing PN.

2.1 | Noise filtering technique

The PN can be promoted by reducing the thermal and flicker noises and increasing output oscillation signal swing or Q_L.[7] The noise filter is proposed for reducing the thermal noise and maintaining Q_L.

The thermal noise of the tail current sources (M_3 and M_4) at multiples of the oscillation signal frequency ω_O will corrupt the PN through mixing processes. C_1 is proposed for suppressing the thermal noise at $2\omega_O$ from M_3 and M_4.

When the oscillation signals vary, M_1, M_2, M_3, and M_4 will be altered during the saturation, triode and off regions. The impedance thorough M_1, M_2, M_3, and M_4 will be different. Q_L will vary and result in poor PN. Hence, L_2 and L_3 are inserted between the drains of the tail current sources and the sources of M_1 and M_2 for increasing the impedance and Q_L at ω_O. L_2 and L_3 are chosen to resonate with the parasitic capacitance from the sources of M_1 and M_2 at $2\omega_O$. L_1 uses a center-taped inductor for reducing the chip area.

2.2 | Feedback capacitors

The oscillation signal swing can be enlarged for lowering PN. Several circuits may increase P_D and get higher oscillation signal swing. However, the proposed feedback capacitors can increase the oscillation signal swing without enlarging P_D. C_2 and C_3 in parallel with M_1 and M_2 form positive feedbacks, which can increase the oscillation swing under low P_D. However, the oscillation frequency will be lowered while C_2 and C_3 are used. Hence, the sizes of M_1 and M_2 should be reduced for enlarging the oscillation frequency. The tuning range is limited by C_2 and C_3. The simulated result of the oscillation signal V_X is shown in Figure 2. The oscillation signal swing of V_X with C_2 and C_3 has larger amplitude than the one without C_2 and C_3.

2.3 | Switched biasing technique

NMOS and PMOS transistors in strong inversion have higher flicker noise power density than in depletion and accumulation regions. The flicker noise power density of PMOS transistors in triode region is smaller than the one in saturation region. The switched biasing technique is proposed for supressing the flicker noise from M_3 and M_4. The gates of M_3 and M_4 connect with the oscillation signals V_X and V_Y through C_4 and C_5. The oscillation signals can alter the gate voltages of M_3 and M_4. Hence, M_3 and M_4 operate in cutoff and triode regions. The flicker noise of M_3 and M_4 will be reduced in the regions. The conduction time of M_3 and M_4 can be reduced for low flicker noise and P_D. The gate voltages V_{B1} and V_{B2} of M_3 and M_4 are equal to 0.1 V.

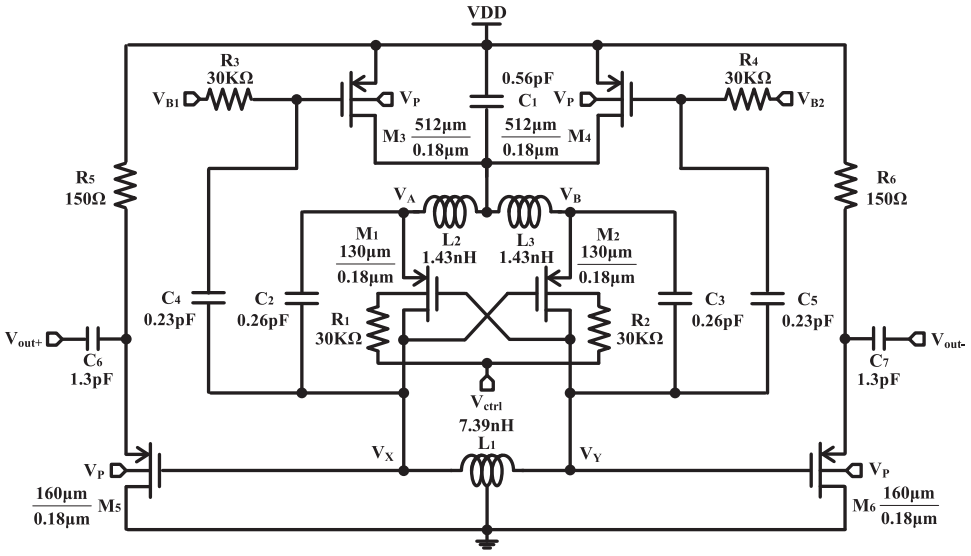

FIGURE 1 Schematic of the proposed VCO.

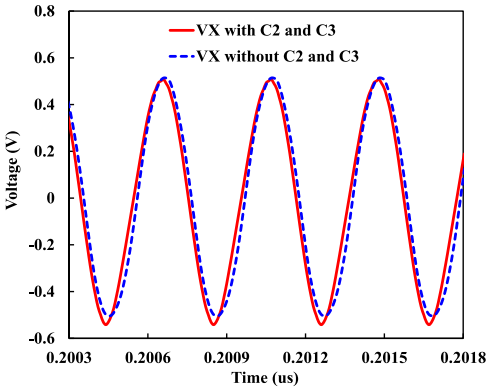

FIGURE 2 The simulated result of V_X with and without C_2 and C_3.

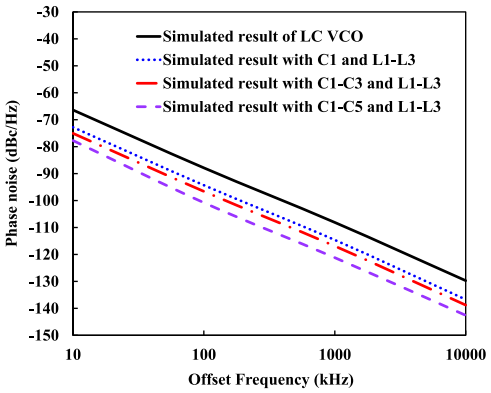

FIGURE 3 The simulated PN reduction contributed from the proposed noise filtering, feedback capacitors, and switched biasing technique while V_{ctrl} is 0.3 V. PN, phase noise.

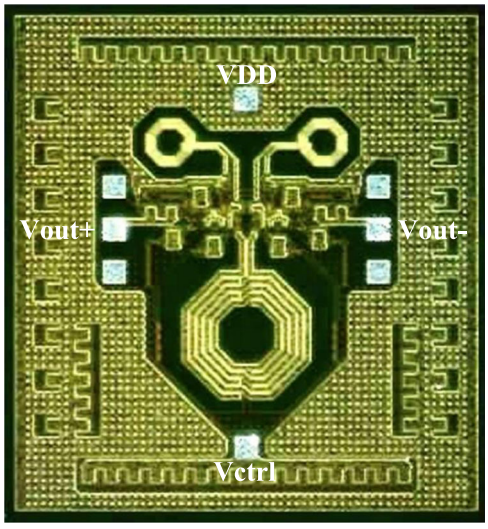

FIGURE 4 The chip micrograph of the proposed VCO.

3 | PHASE NOISE OF THE VCO

For comparing the PN suppression from the proposed noise filtering, feedback capacitors, and switched biasing technique, the simulated PN under several combinations is proposed. The simulated PN contributed from different techniques while V_{ctrl} is 0.3 V is shown in Figure 3.

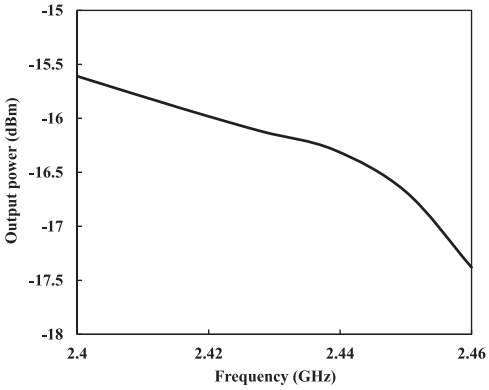

FIGURE 5 The measured output power of the proposed VCO.

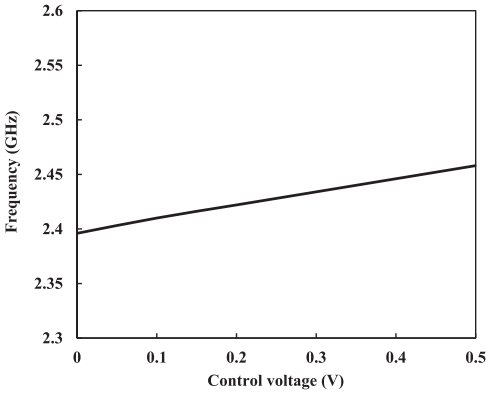

FIGURE 6 The measured tuning range of the proposed VCO.

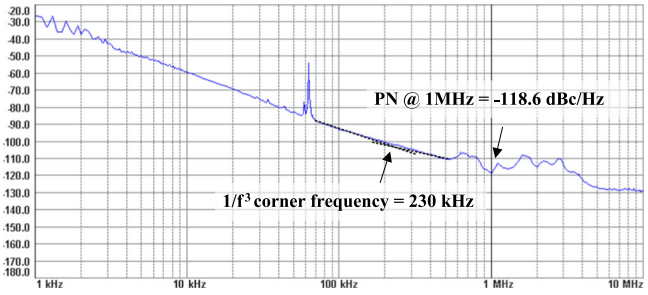

FIGURE 7 The measured PN with the $1/f^3$ corner frequency of the proposed VCO.

TABLE 1 Performance comparison of state-of-the-art LNA.

	This work	Ding et al.[9]	Cheng et al.[10]	Huang et al.[11]	Ding et al.[9]	Shasidharan et al.[12]	Wang et al.[13]
CMOS Process (nm)	180	40	180	65	40	180	180
VDD (V)	0.5	0.6	1.1	1.1	0.6	1.2	0.5
f_O (GHz)	2.4–2.46	1.57	2.4	27.7	1.57	2.45	2.25
PN @1 MHz (dBc/Hz)	−118.6	−118.6	−122.85	−103.9	−118.6	−120	−119.4
P_D (mW)	0.5–0.8	1.32	1.4	3.3	1.32	1.73	3.23
FOM @1 MHz (dBc/Hz)	−189	−181.3	−189	−187.6	−181	−185	−181

The simulated PN of the VCO without using the proposed techniques is −108.1 dBc/Hz at 1 MHz offset frequency from the carrier signal. The simulated PN of the VCO using the noise filter is −114.6 dBc/Hz. The simulated PN of the VCO using the noise filter and feedback capacitors is −116.7 dBc/Hz. The simulated PN using the noise filter, feedback capacitors, and switched biasing technique is −121.1 dBc/Hz.

4 | MEASUREMENT RESULTS OF THE VCO

The proposed low-power VCO chip was fabricated by TSMC 0.18-μm CMOS technology. The chip micrograph of the proposed VCO has been shown in Figure 4. The chip areaoccupies 0.8 × 1 mm including the bypass capacitors and pads. The chip was measured on wafer with VDD of 0.5 V. The measured output power of the oscillation signal ranges from −15.6 to −17.3 dBm at a frequency from 2.4 to 2.46 GHz without the cable loss as shown in Figure 5. The measured tuning range is from 2.4 to 2.46 GHz with the VCO gain (K_{VCO}) of 118 MHz/V as shown in Figure 6. The measured PN at 1 MHz offset frequency from the carrier signal is −118.6 dBc/Hz when V_{ctrl} is 0 V with the $1/f^3$ corner frequency of 230 kHz as shown in Figure 7. The measured P_D ranges from 0.5 to 0.8 mW without the output buffers. The performance of VCOs can be estimated by a figure of merit (FOM) equation as follows[8]:

$$\mathrm{FOM} = PN\text{-}20\log\left(\frac{\omega_0}{\Delta\omega}\right) + 10\log\left[\frac{P_D}{1mW}\right]. \quad (1)$$

FOM at 1 MHz offset frequency from the carrier signal is −189 dBc/Hz. Table 1 summarizes the performance comparison of state-of-the-art VCOs.

5 | CONCLUSION

In this paper, a 0.5-V low-power VCO in TSMC 0.18-μm CMOS technology is proposed. With the proposed PMOS topology, noise filter, feedback capacitors, and switched biasing technique, the measured PN at 1 MHz offset frequency from the carrier signal is −118.6 dBc/Hz with the $1/f^3$ corner frequency of 230 kHz. The proposed forward body biasing technique reduce V_T and V_{DD} with a low P_D from 0.5 to 0.8 mW. FOM is −189 dBc/Hz. The experimental results demonstrate the proposed VCO is suitable for low-power applications.

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DATA AVAILABILITY STATEMENT
Research data are not shared.

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