

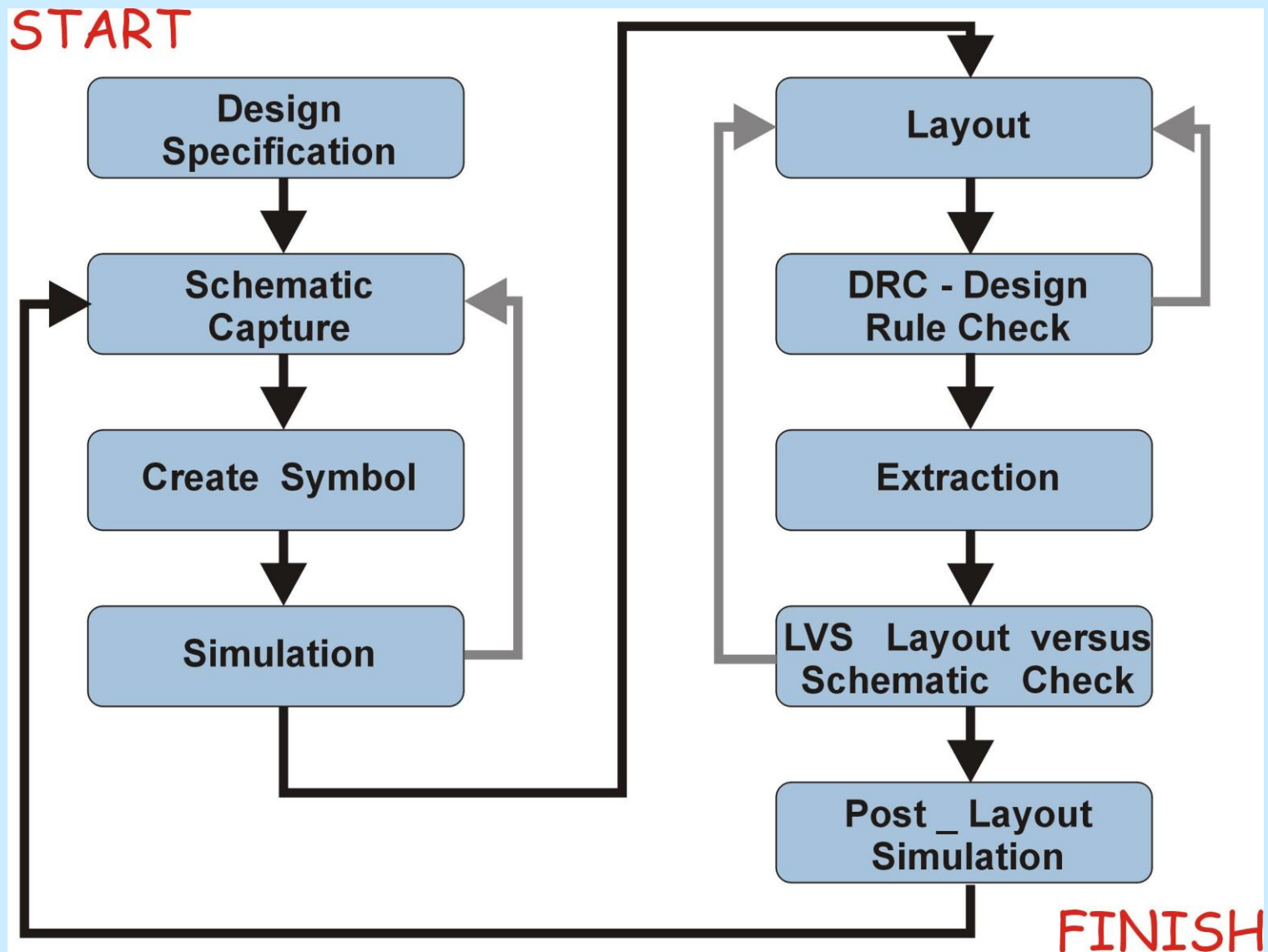
Micromagic

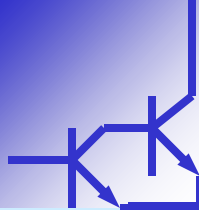

**CADENCE**
Tools

Lecture bases on CADENCE Design Tools Tutorial

<http://vlsi.wpi.edu/cds>

Analog design flow





CADENCE Tools for IC Design

Cadence is a set of different design tools used at different stages of the design process.

Which tools we exactly need ?

Sue ← ~~Composer~~ → Schematic editor

Max ← ~~Virtuoso~~ → Layout editor

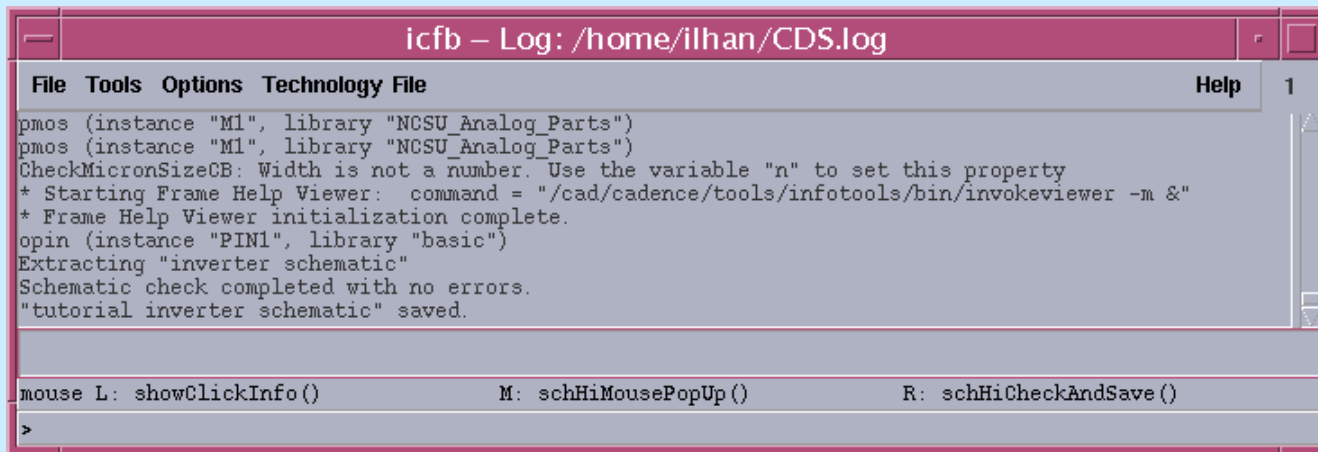
~~Analog Artist~~ → preparing simulation → ciw
(SpectreS in this tutorial) LibraryMgr or other single TCL file

~~DIVA~~ → Design Rule Check (DRC) , Layout Versus Schematic Check (LVS) , Extraction

micromagic built-in gemini tool.
It is not Google Gemini !!

First steps with Cadence

- To start Cadence software enter: ~~icfb &~~ $\longrightarrow$ ciw
- The cadence window after start up:



The screenshot shows a window titled "icfb - Log: /home/ilhan/CDS.log". The window has a menu bar with "File", "Tools", "Options", "Technology", "File", and "Help". The main area displays the following log content:

```
pmos (instance "M1", library "NCSU_Analog_Parts")
pmos (instance "M1", library "NCSU_Analog_Parts")
CheckMicronSizeCB: Width is not a number. Use the variable "n" to set this property
* Starting Frame Help Viewer:  command = "/cad/cadence/tools/infotools/bin/invokeviewer -m &"
* Frame Help Viewer initialization complete.
opin (instance "PIN1", library "basic")
Extracting "inverter schematic"
Schematic check completed with no errors.
"tutorial inverter schematic" saved.
```

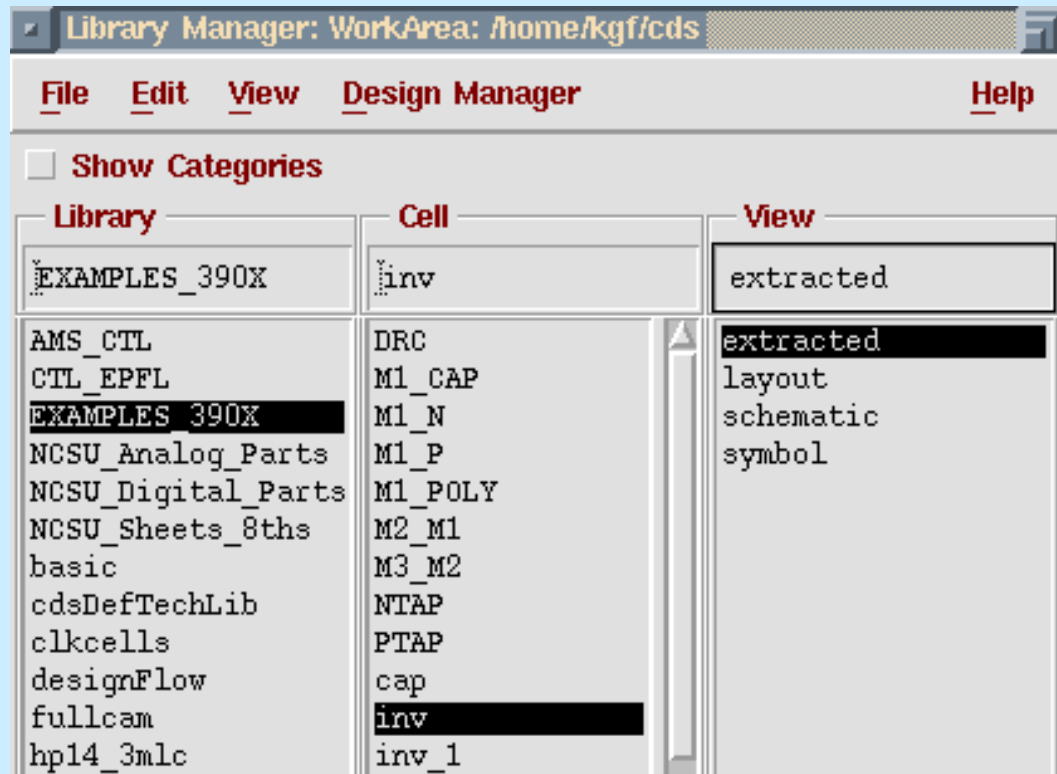
At the bottom, there is a status bar with the following text:

```
mouse L: showClickInfo()          M: schHiMousePopUp()          R: schHiCheckAndSave()
>
```

- To see your cadence libraries open **Library Manager** from „Tools menu“

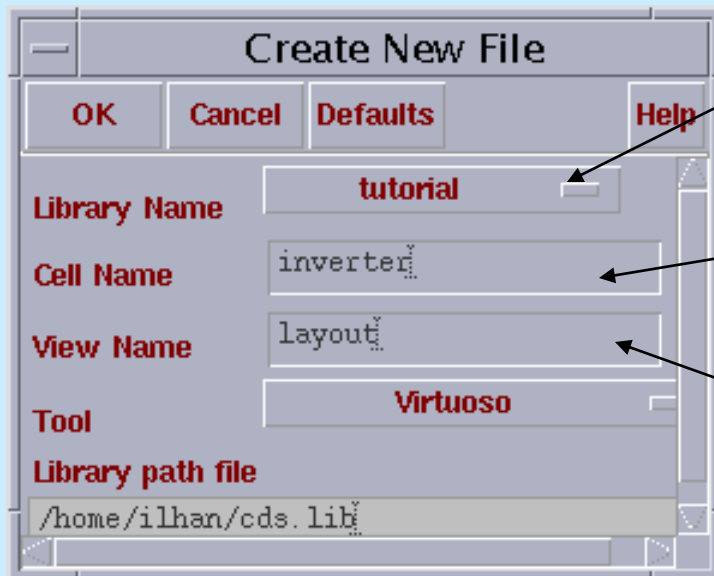
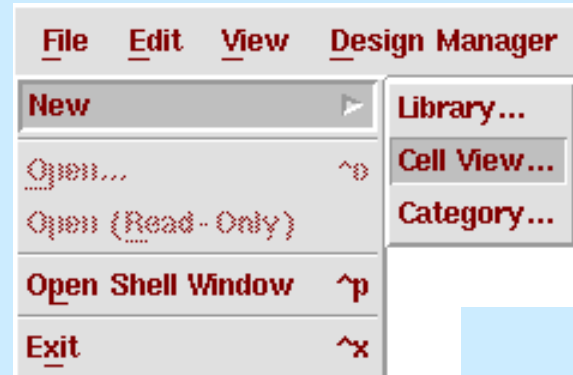
First steps with Cadence

- Cadence libraries:
 - **Technological Libraries** (usually names written with upper cases)
 - **User Libraries**
- Libraries contain **cells** - basic elements of your design
- Every cell may have different **views** - different views created at different stages of the design and edited with different tools



Creating new libraries and cells

1. In *File* on the menu of *Library Manager* choose *New* -> *Library* or *Cellview*.
2. Exemplary „Creat New File window“



Library Name

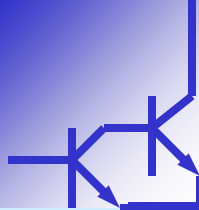
Choose your working directory and library name

Cell Name

Enter the cell name

View Name

Enter view name depending on the level of the design hierarchy.
Eg. schematic or layout

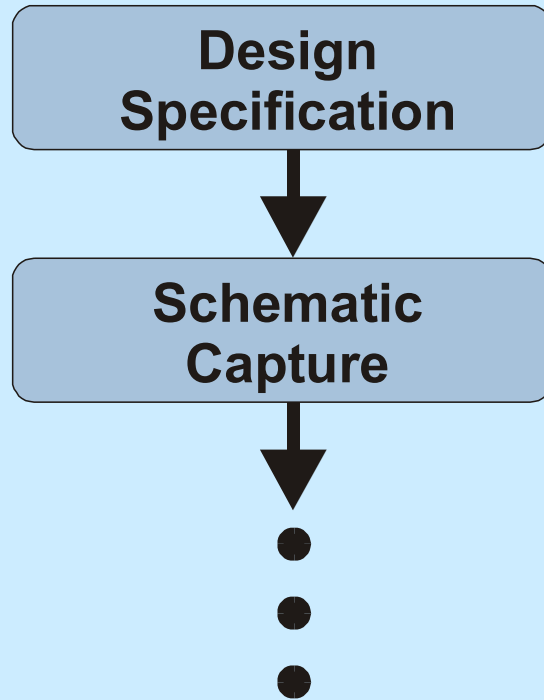


Design Example

CMOS - Inverter

Creating Schematics

START

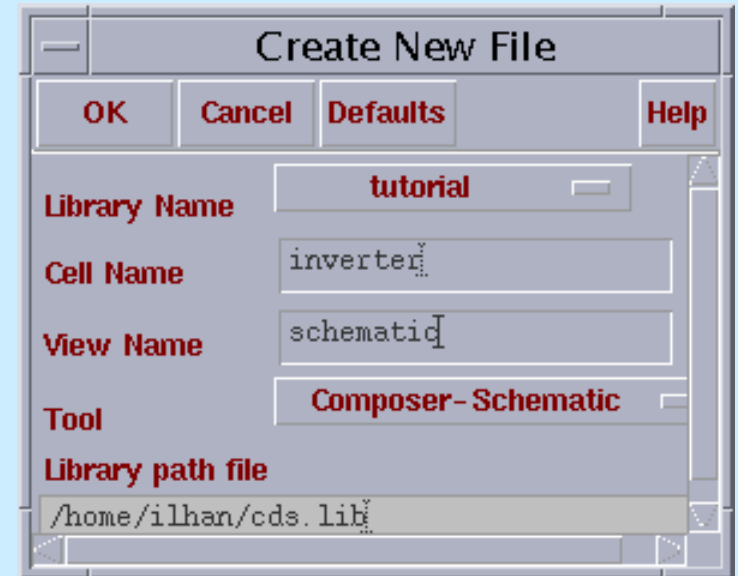


- The traditional method for capturing (i.e. describing) your transistor-level or gate-level design is via the schematic editor.
- Schematic editors provide simple, intuitive means to draw, to place and to connect individual components that make up your design.
- The resulting schematic drawing must describe the main electrical properties of all components and their interconnections.

Open a new schematic window

•View Name

Indicates the level of the design hierarchy. The correct view name choice is "schematic" for our example.



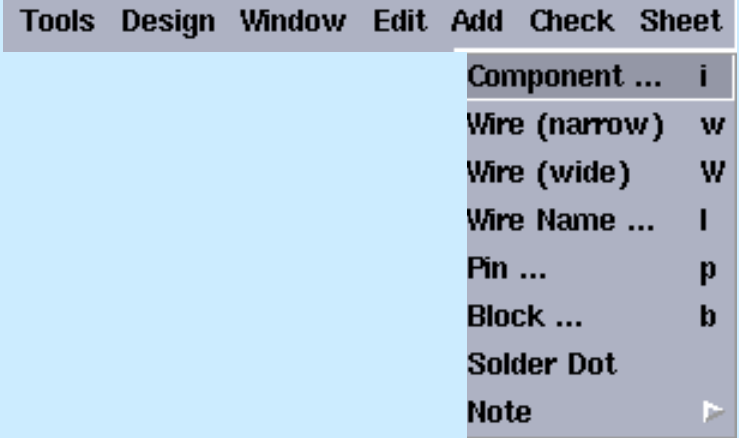
Click OK to finish

Add components

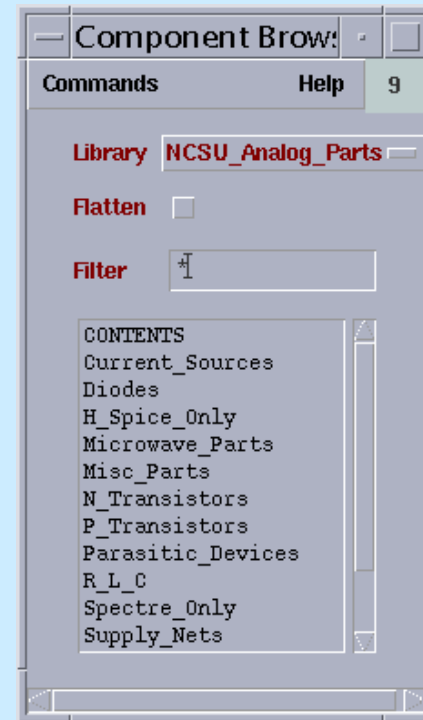
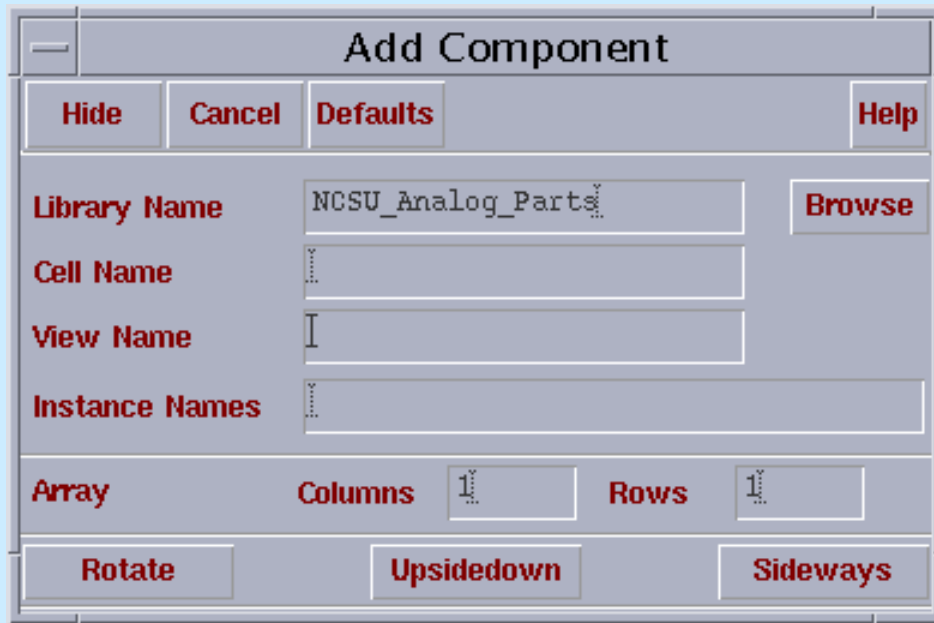
The first thing to do is to add and place components which will be used in the schematic.

We need the components as follows:

- PMOS : p-type MOSFET
- NMOS : n-type MOSFET
- VDD : vdd! global net marker
- GND : gnd! global net marker



Add components



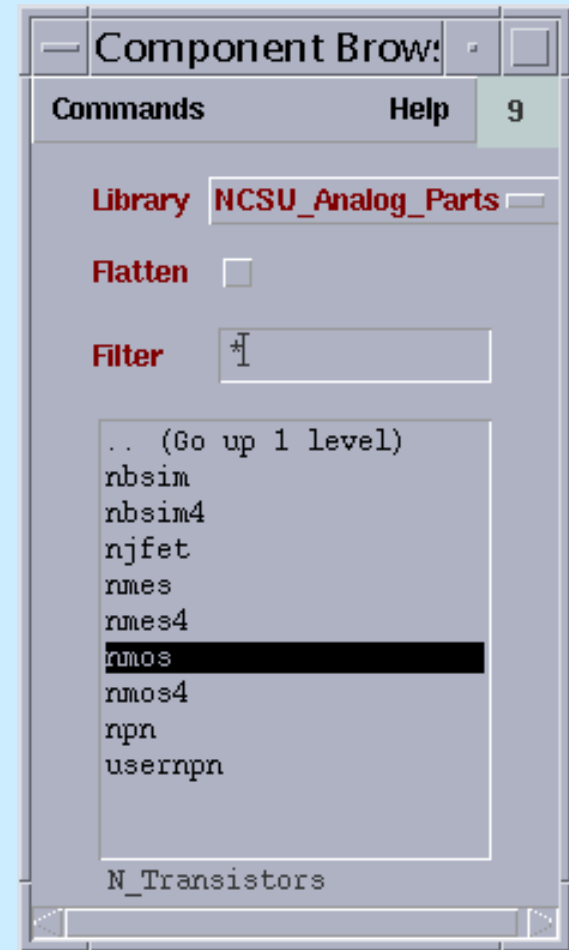
- **Add Component Window**
Enter the *Library Name*,
Cell Name and the *View Name*
Name of the component

- **Component Browser**
enables the designer to
browse easily through the
available libraries and select
the desired components.

Add components

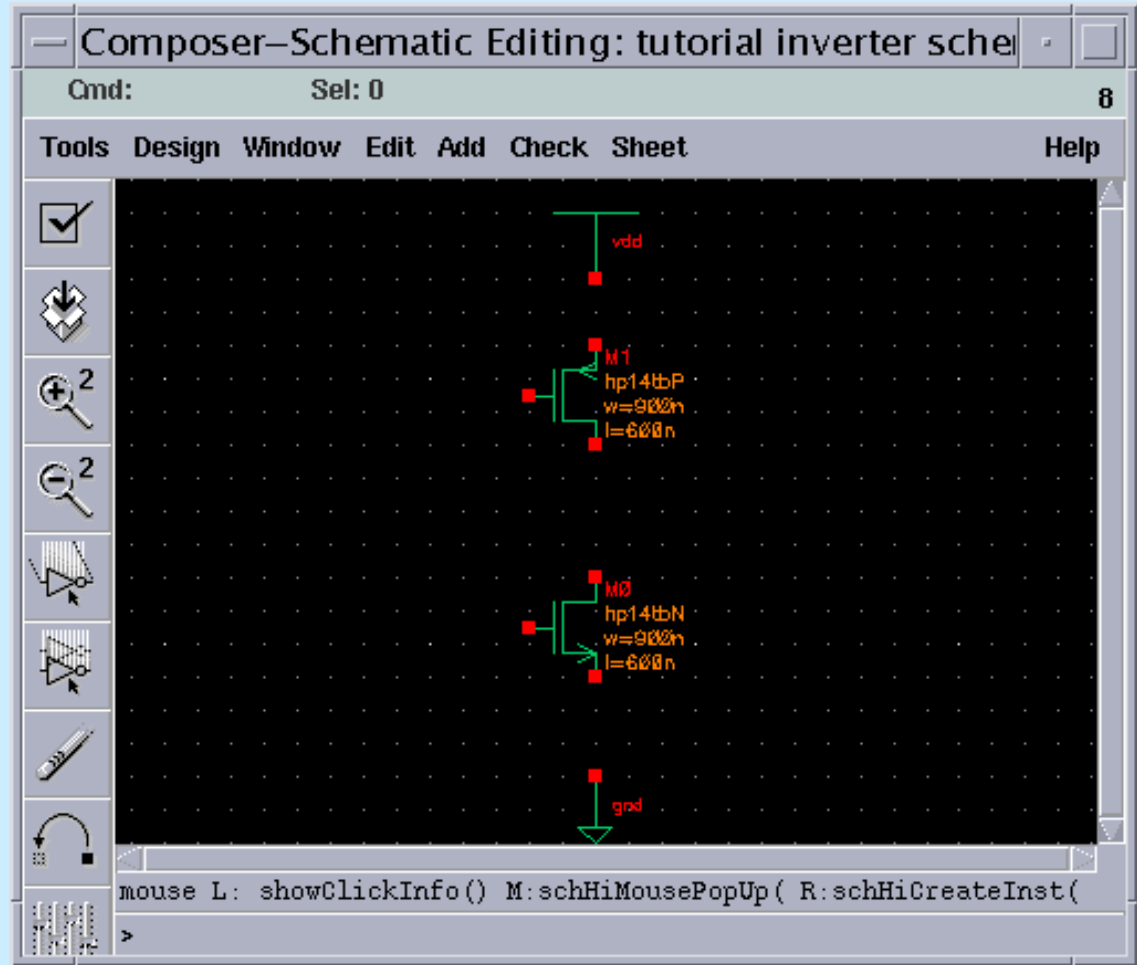
Pick up the MOS transistors from the *Component Browser* window.

- Open the "N_Transistors" folder by clicking once on it.
- Pick up the NMOS transistor by clicking once on "nmos", which is a model for a three terminal n-type MOSFET.

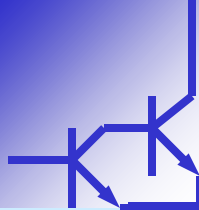


Add components

- Click on a location in the schematic window, where you want to put the transistor.
- Use the same procedure to select and to place the PMOS transistor.

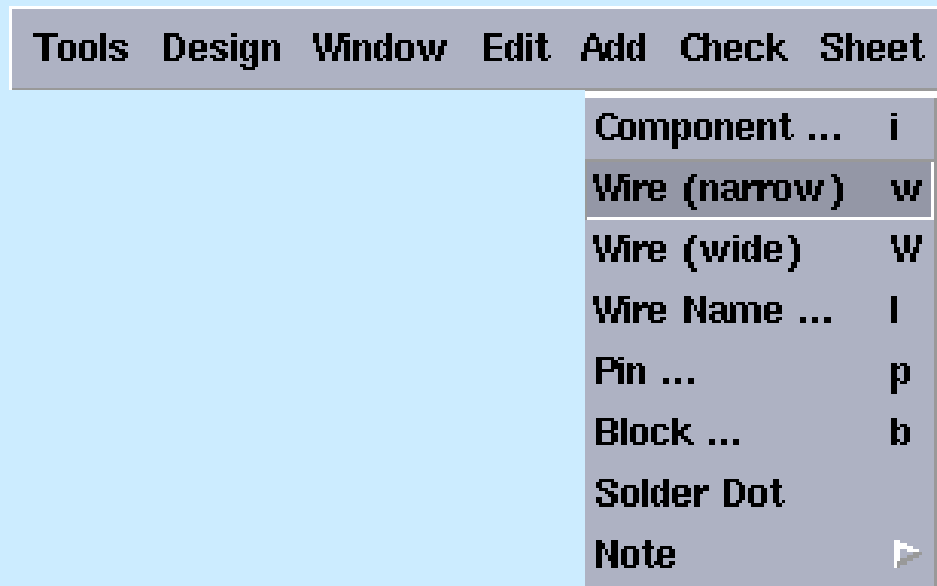


Picking up the supply voltage components involves the same steps as in adding transistors to the schematic.



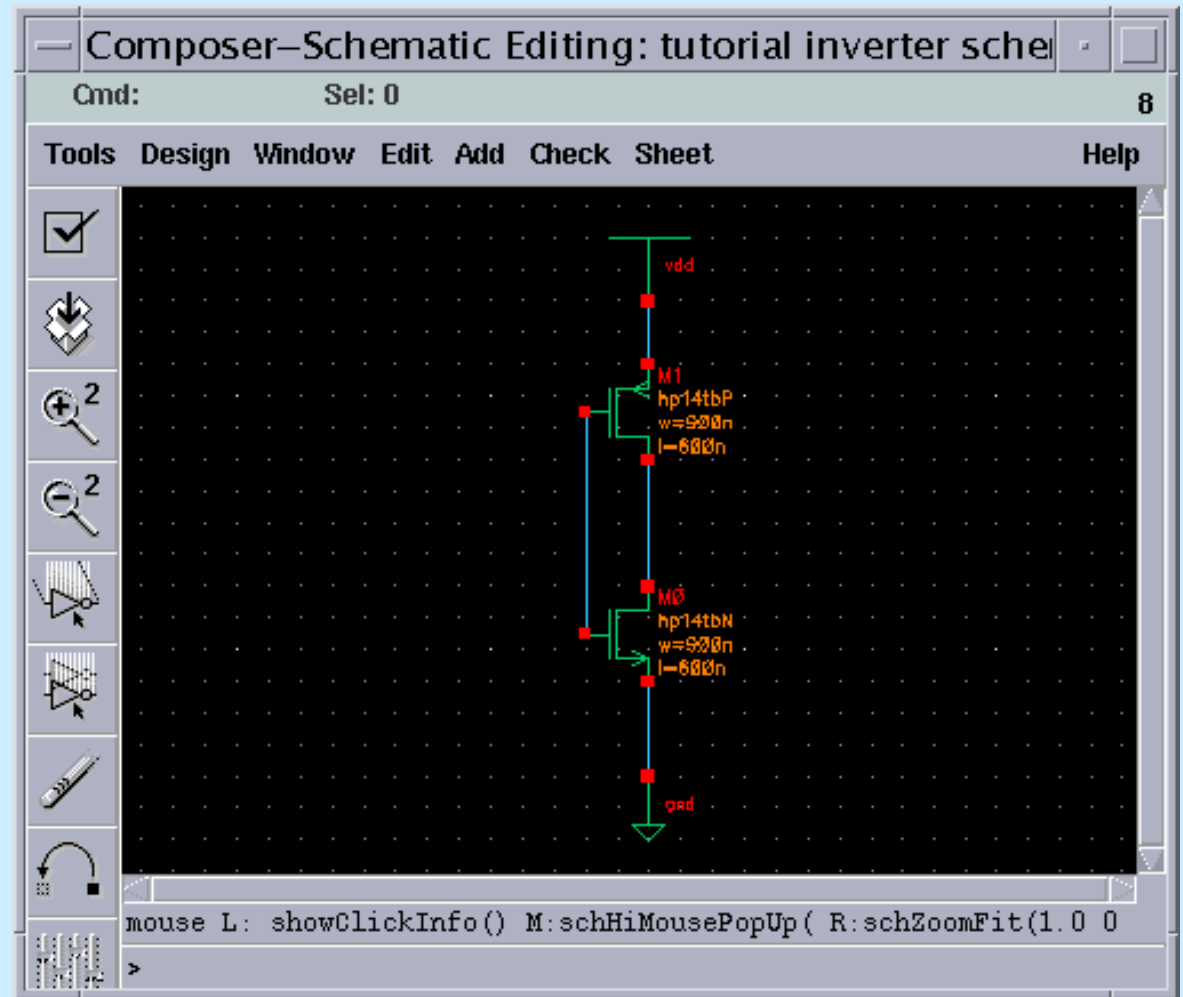
Conecting components

To connect the components in a schematic, we use wires by choosing *Add* and then *Wire (narrow)* on the menu banner.



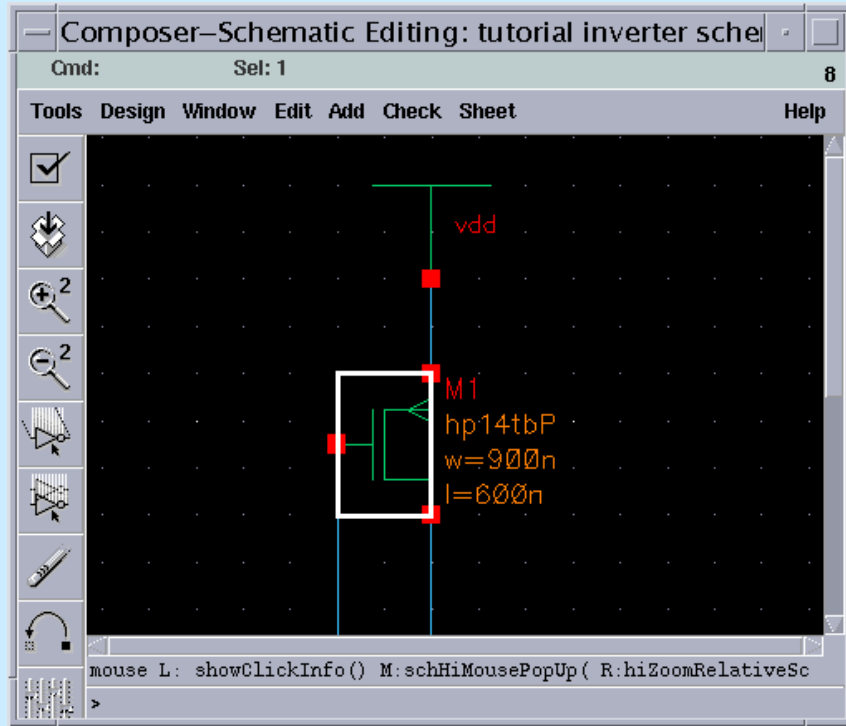
Connecting components

Connecting any two nets in the schematic is done by first clicking at one of the nets and then at the other one.

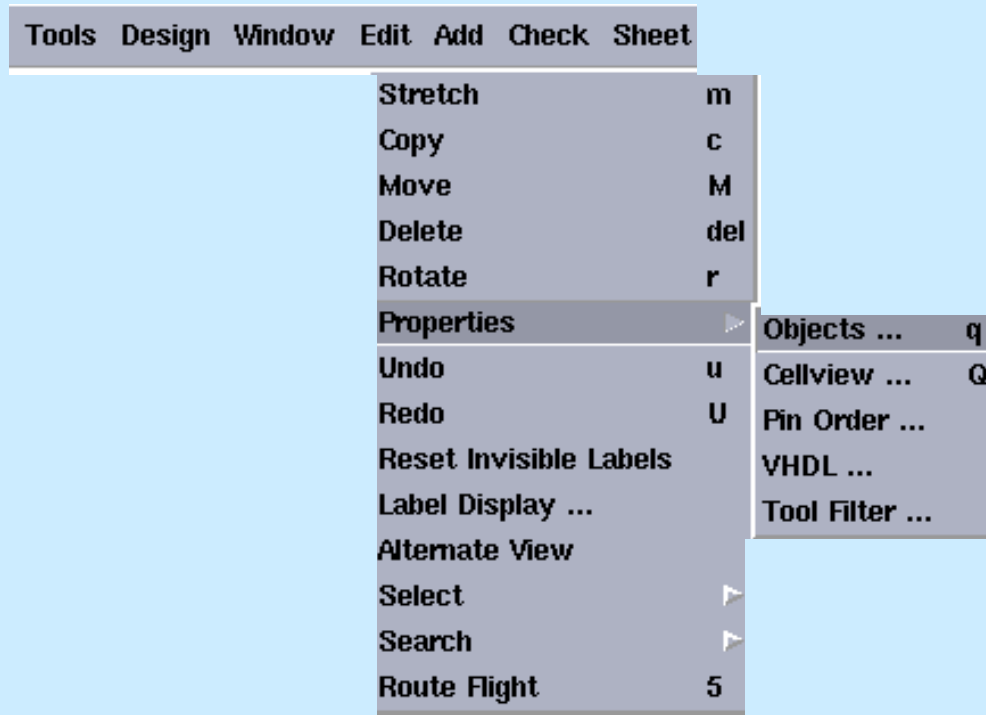


Press ESC key to leave the wiring mode.

Edit properties of components



<= 1. Select component
by clicking on it



2. Choose *Properties* =>
and then *Object* from
the *Edit* menu.

Edit properties of components

3. Edit the properties =>

by clicking on the corresponding field. You may change the values for *Width* or *Length* depending on your design specifications.

Edit Object Properties

OK Cancel Apply Defaults Previous Next Help

Apply To

Show ☐ system ☒ user ☒ CDF

Instance Properties

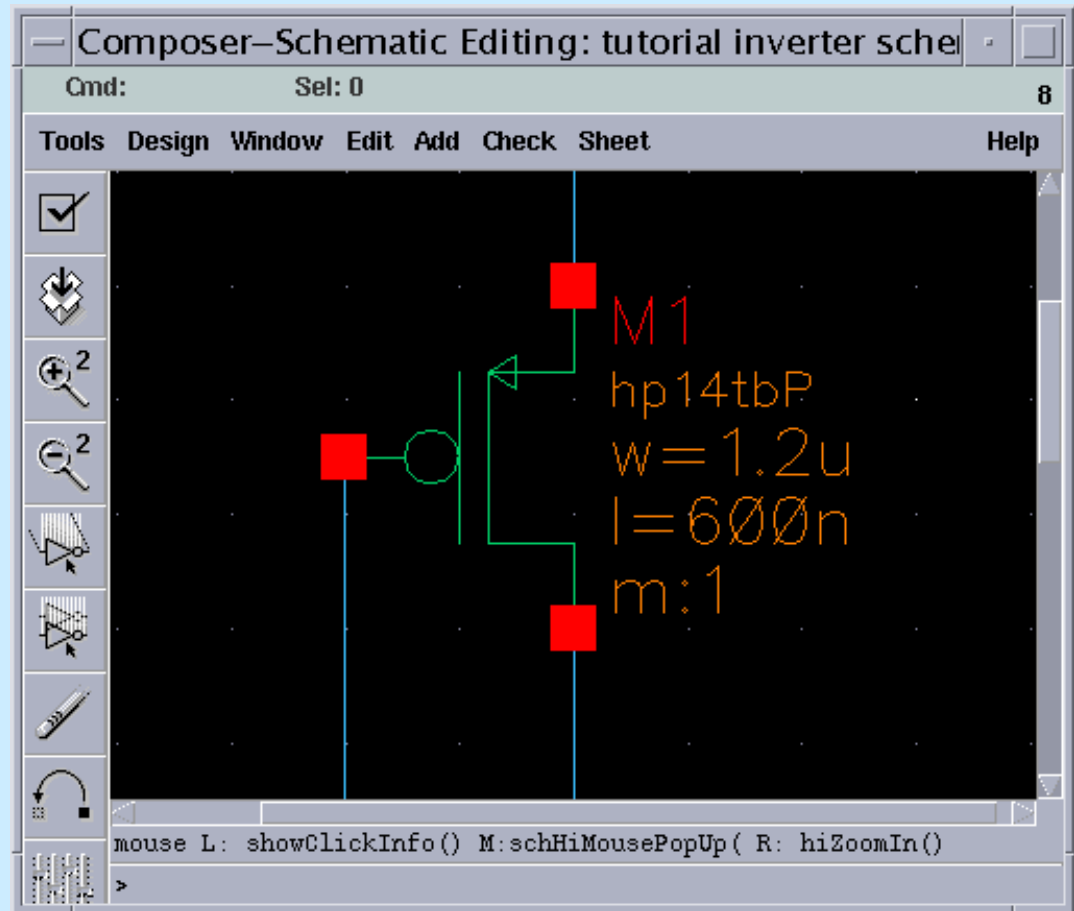
Property	Value	Display
Library Name	NCSU_Analog_Parts	off
Cell Name	pmos	off
View Name	symbol	off
Instance Name	M1	off

CDF Parameters

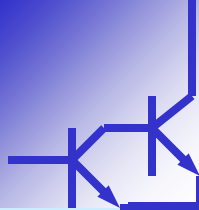
CDF Parameter	Value	Display
Model name	hp14tbP	off
Model Type	☒ system ☐ user	off
Bulk node connection	vdd	off
Multiplier	1	off
Fingers	1	off
Width (grid units)	6	off
Width	900n M	off
Width (minimum)	900n M	off
Length (grid units)	4	off
Length	600n M	off
Length (minimum)	600n M	off
Drain diffusion area	1.35e-12	off
Source diffusion area	1.35e-12	off

Edit properties of components

4. Click OK after => editing the properties in the *Edit Object Properties Window*.



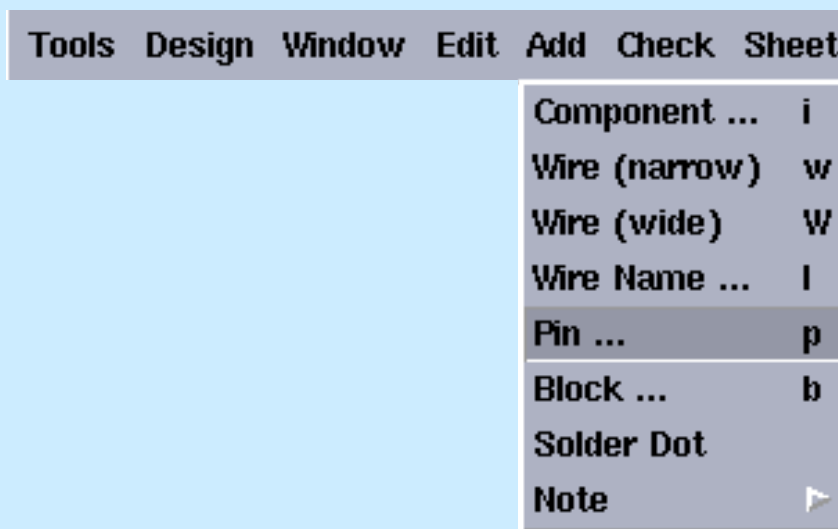
The most important parameters always appear in the schematic window.



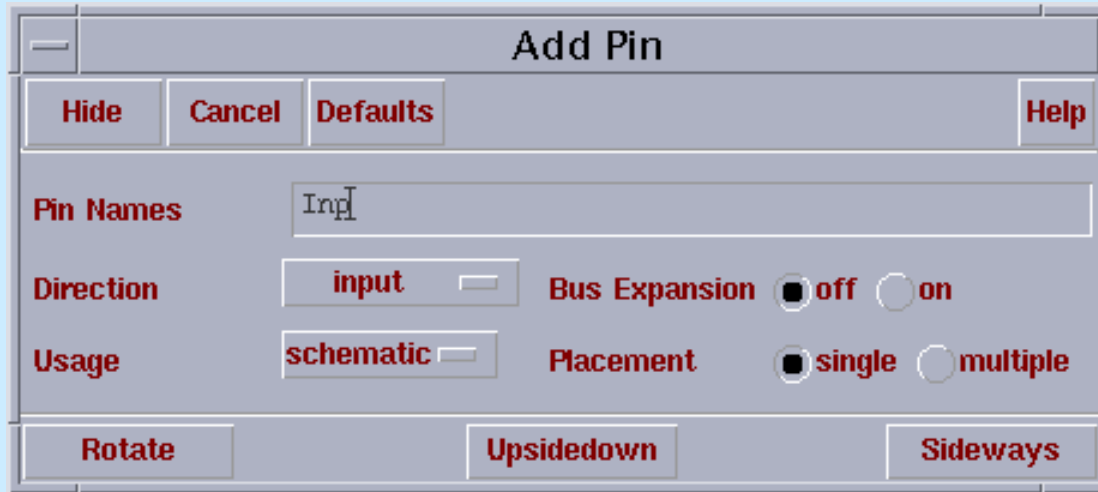
Placing the pins

You must place I/O pins in your schematic to identify the inputs and the outputs.

1. Click *Add* on the $\Rightarrow$ menu and then select *Pin* on the pull-down menu.



Placing the pins

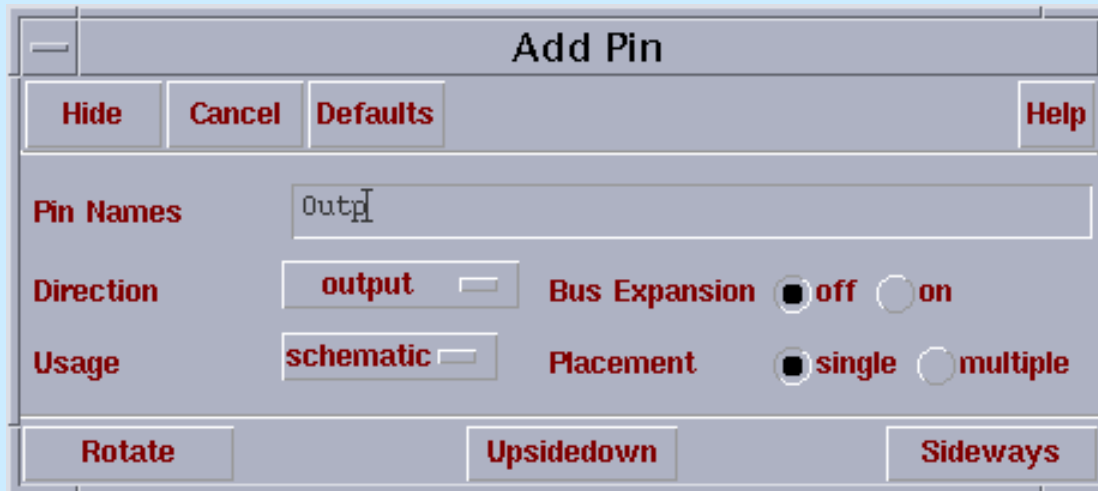


The 'Add Pin' dialog box is shown with the following settings:

- Pin Names:** InpI
- Direction:** input (selected)
- Usage:** schematic (selected)
- Bus Expansion:** off (selected)
- Placement:** single (selected)

Buttons at the bottom: Rotate, Upsidedown, Sideways.

2. Enter the name of your pins in the *Pin Names* field. Choose the direction.



The 'Add Pin' dialog box is shown with the following settings:

- Pin Names:** OutpI
- Direction:** output (selected)
- Usage:** schematic (selected)
- Bus Expansion:** off (selected)
- Placement:** single (selected)

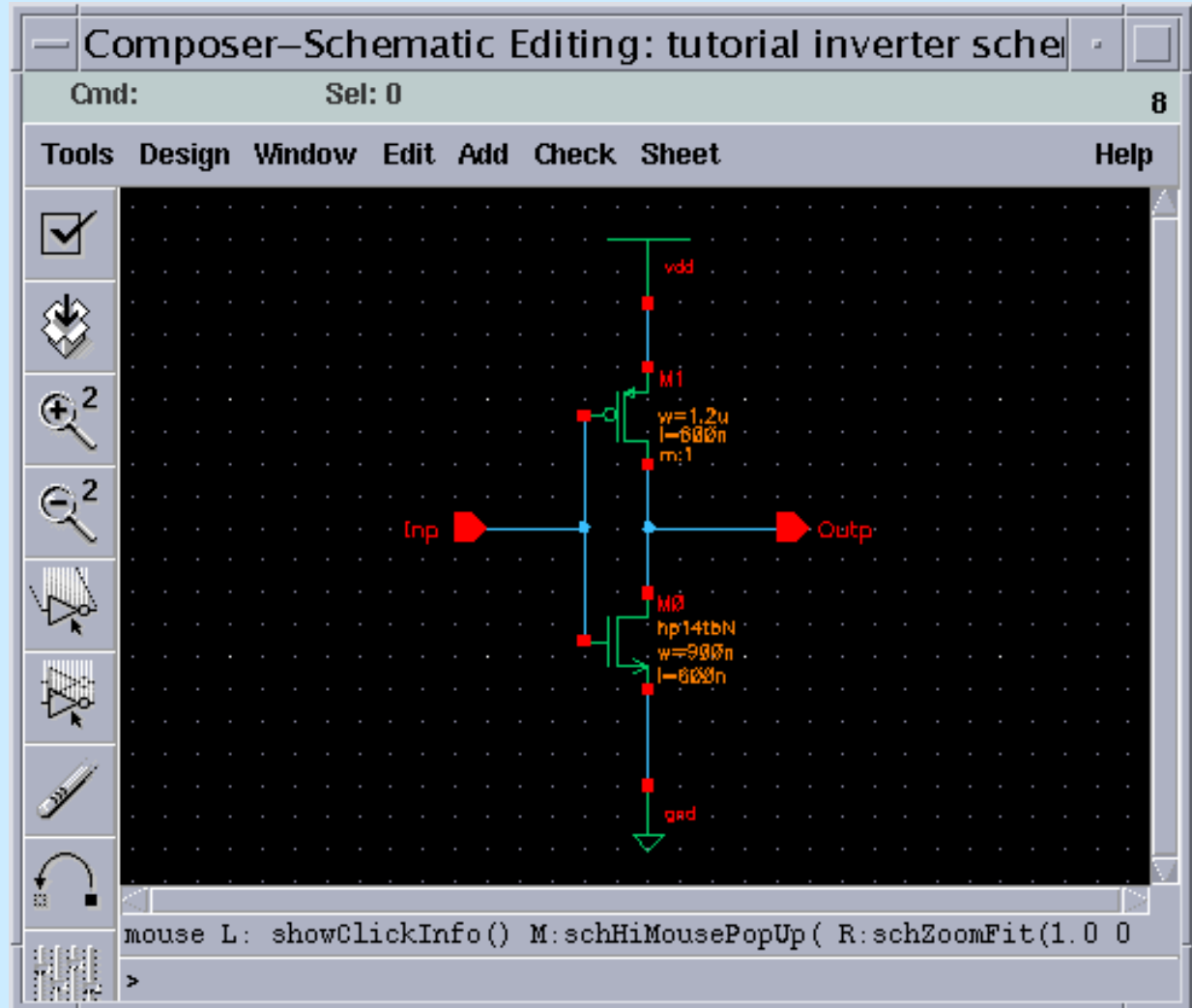
Buttons at the bottom: Rotate, Upsidedown, Sideways.

Place pins by clicking on a location in the schematic window.

Placing the pins

Connect the =>
pins to the
corresponding
nodes using wires.

The wiring
procedure is the
same as described
in the previous
steps.



Check and Save

Click *Design* on the menu banner =>
and then select *Check and Save*.

Tools Design Window Edit Add Check Sheet

Check and Save	X
Save (not needed)	S
Save As ...	^s
Hierarchy	^
Create Cellview	^
New ...	
Open ...	
Discard Edits ...	
Make Read Only	
Probe	^
Options	^
Plot	^
Renumber Instances ...	

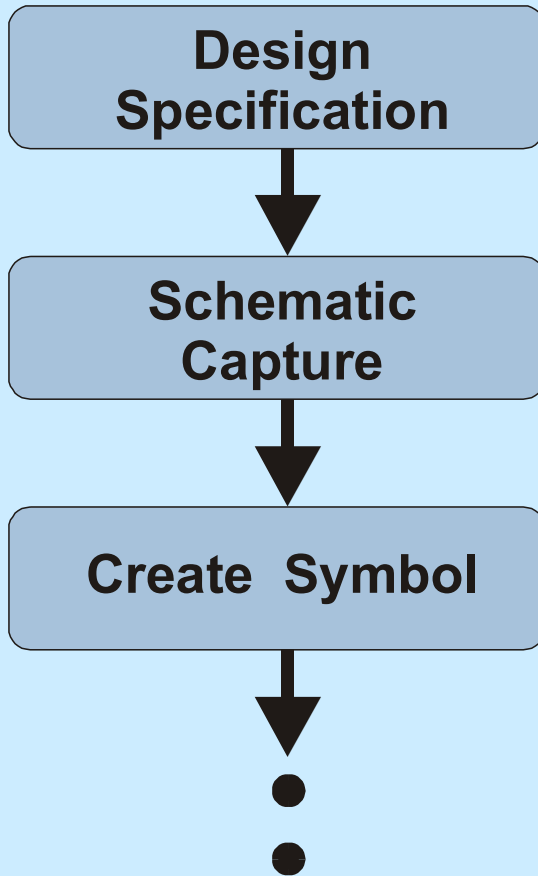
```
icfb - Log: /home/ilhan/CDS.log
File Tools Options Technology File Help 1
pmos (instance "M1", library "NCSU_Analog_Parts")
pmos (instance "M1", library "NCSU_Analog_Parts")
CheckMicronSizeCB: Width is not a number. Use the variable "n" to set this property
* Starting Frame Help Viewer:  command = "/cad/cadence/tools/infotools/bin/invokeviewer -m &"
* Frame Help Viewer initialization complete.
opin (instance "PIN1", library "basic")
Extracting "inverter schematic"
Schematic check completed with no errors.
"tutorial inverter schematic" saved.

mouse L: showClickInfo()           M: schHiMousePopUp()           R: schHiCheckAndSave()
>
```

<= Check the
message field
every time you
save a design.

Creating cellview

START

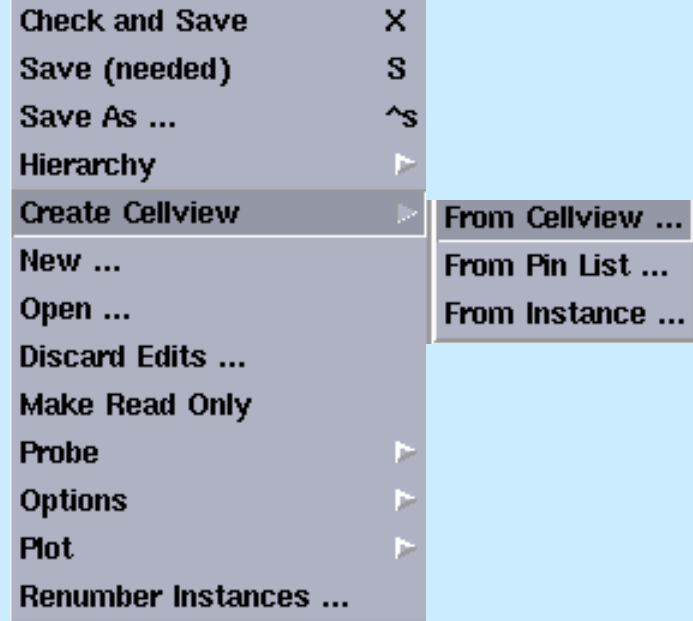


If a certain circuit design consists of smaller hierarchical components (or modules), it is usually very beneficial to identify such modules early in the design process and to assign each such module a corresponding symbol (or icon) to represent that circuit module.

Creating cellview

From the *Design* menu, select **Create Cellview** and then *From* => **Cellview**

Tools Design Window Edit Add Check Sheet



<= Check the view names You have to ensure that the target view name is symbol.

Locating the pins

After clicking OK in the Cellview From Cellview, window the following window pops up :

The dialog box is titled "Symbol Generation Options". It has buttons for "OK", "Cancel", "Apply", and "Help". Below these are three text fields: "Library Name" with the value "Tutorial", "Cell Name" with the value "inverter", and "View Name" with the value "symbol". Below these is a section titled "Pin Specifications" with a table of pin locations and attributes.

		Attributes
Left Pins	Inp	List
Right Pins	Outp	List
Top Pins		List
Bottom Pins		List

At the bottom of the dialog are four checkboxes: "Load/Save", "Edit Attributes", "Edit Labels", and "Edit Properties", all of which are currently unchecked.

Edit your pin attributes and locations.

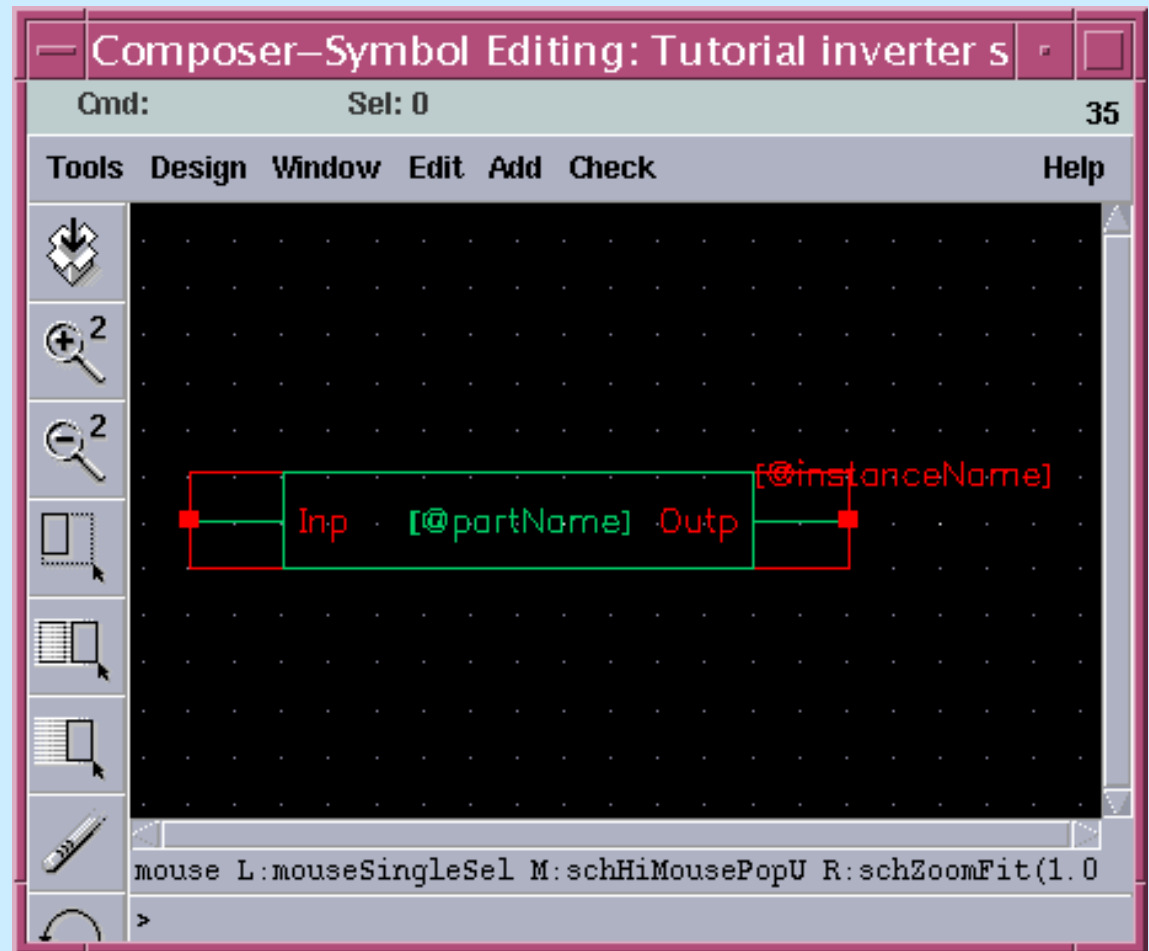
In the default case, you will have your

- input(s) on the left of the symbol
- output(s) on the right of the symbol.

Change pin locations by putting the pin name in the corresponding pin location field

Editing the shape of the symbol icon

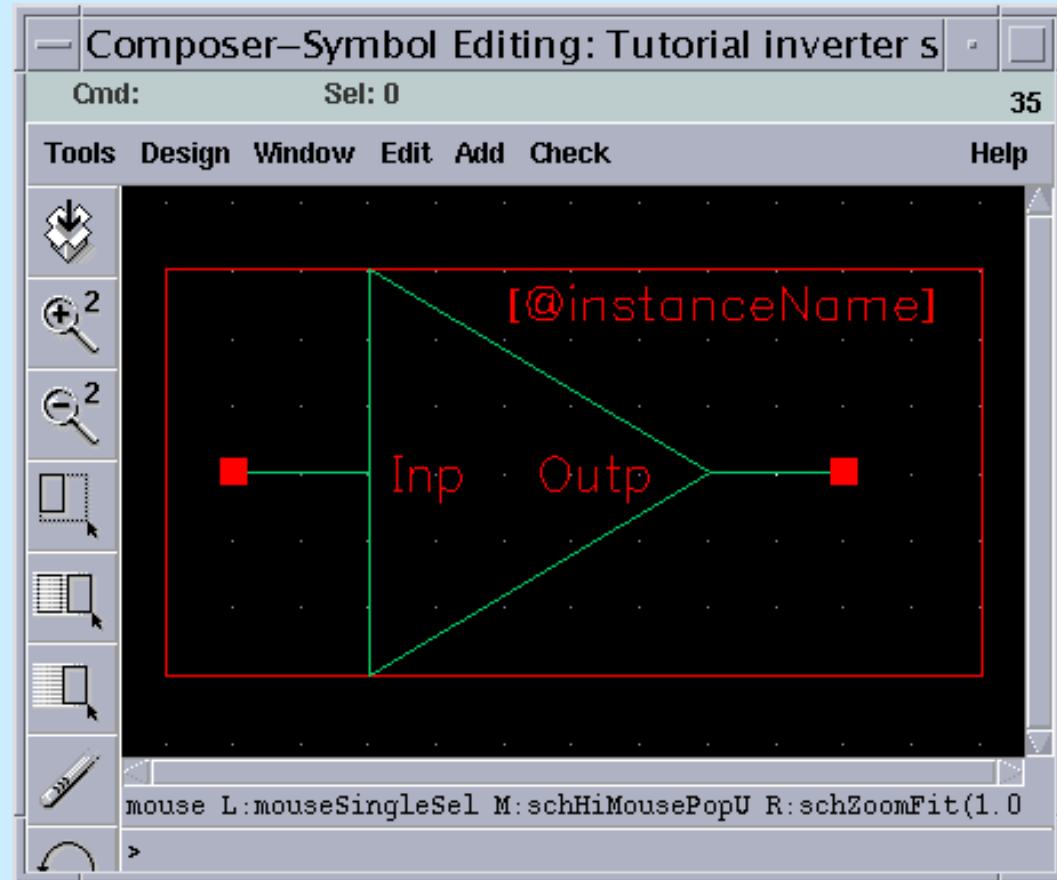
In the new window, the automatically generated symbol is shown.



Editing the shape of the symbol icon

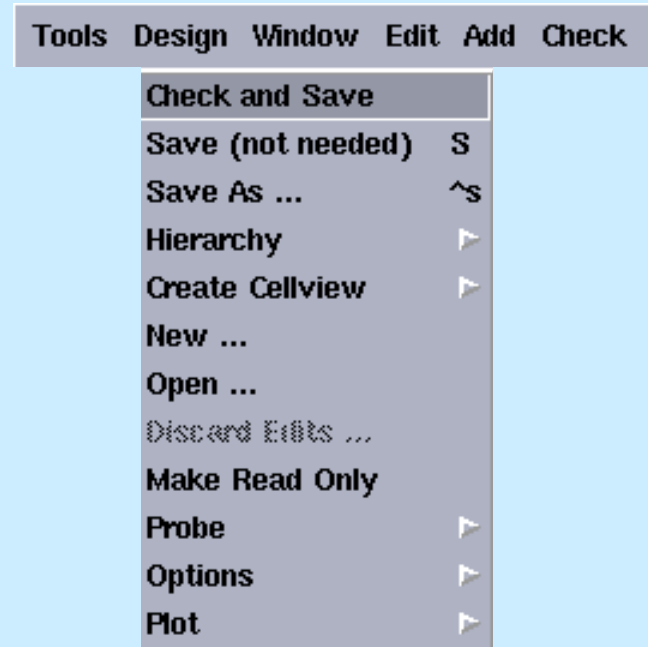
You can do the following operations on your symbol

- Deleting/replacing some existing parts
- Adding new geometric shapes
- Changing the locations for pins and instance name
- Adding new labels



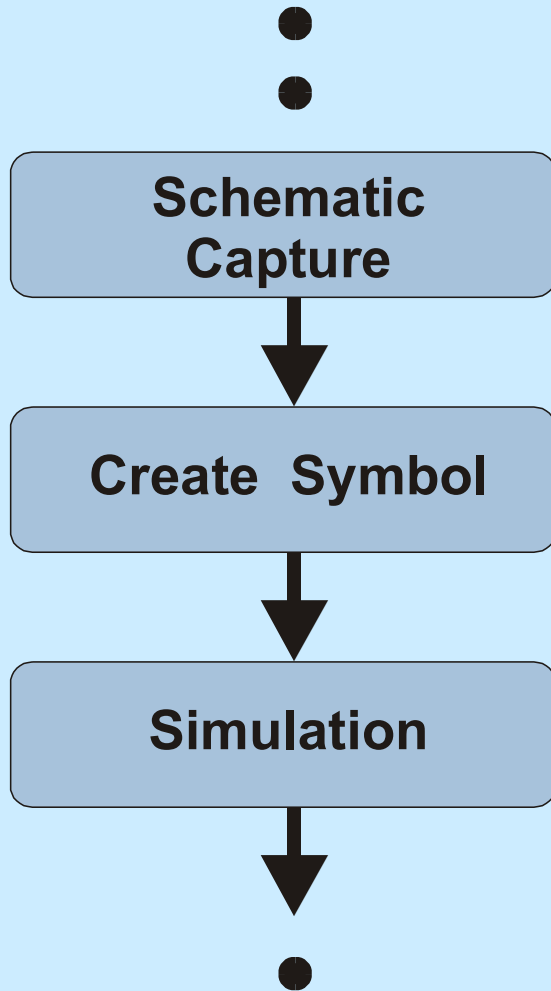
Check and Save - Once Again

- **Save** - doesn't check anything.
- **Checking** a symbol means comparing the symbol view with the corresponding schematic view, by matching all of the pin names.



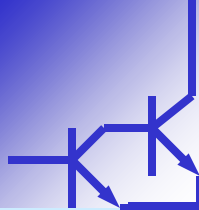
To check and save the symbol, choose *Check and Save* from the *Design* menu

Simulation



- The electrical performance and the functionality of the circuit must be verified using a Simulation tool.

- Based on simulation results, the designer usually modifies some of the device properties.

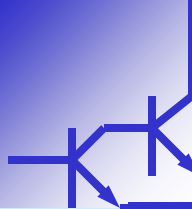


Simulation -New Schematic Design

1. Open a new schematic.

- Follow the same procedure described in „Open a new schematic" to create a new schematic where you will put your simulation schematic for the inverter.
- Give a name to your new schematic which makes it clear that the new schematic is to *simulate* the inverter.

• **Note** : You should first create the *symbol* of the circuit schematic which you want to simulate



Simulation - Select and place components

The first step is to add and to place the components which will be used to simulate the inverter.

The components we need for the simulation of the inverter are the following :

- Inverter - Symbol created for the inverter
- VDD - Power supply voltage
- GND - Ground line
- vdc - DC voltage source
- vpulse - Pulse waveform generator
- C - Capacitor

Simulation - Select and place components

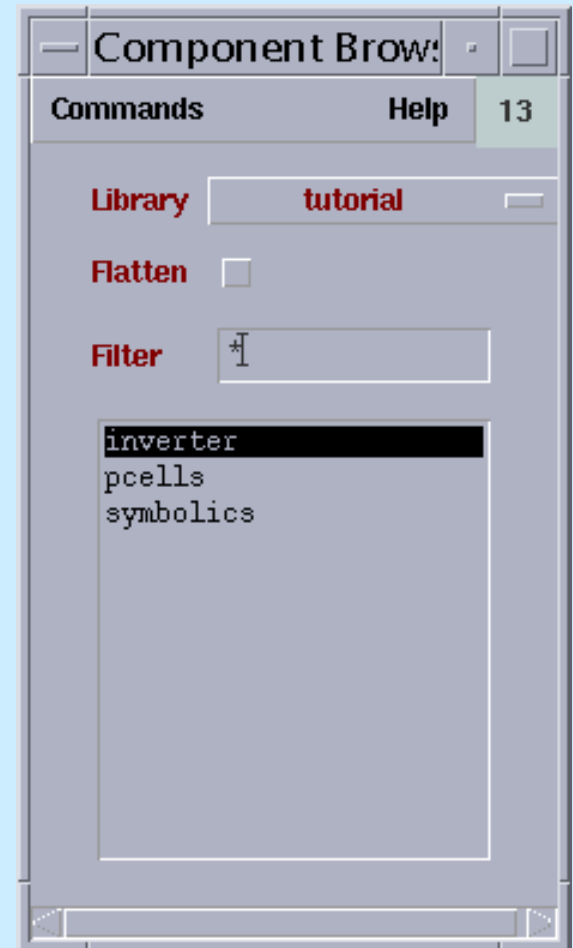
How to pick up a *symbol* from library, and to place it in the schematic ?

NCSU_Analog_Parts
NCSU_Digital_Parts
NCSU_Sheets_8ths
basic
designFlow
hp14_3mlc
hp14_TechLib
tutorial
All

< = To pick up the inverter symbol, change the library of the *Component Browser* to library, "tutorial".

Simulation - Select and place components

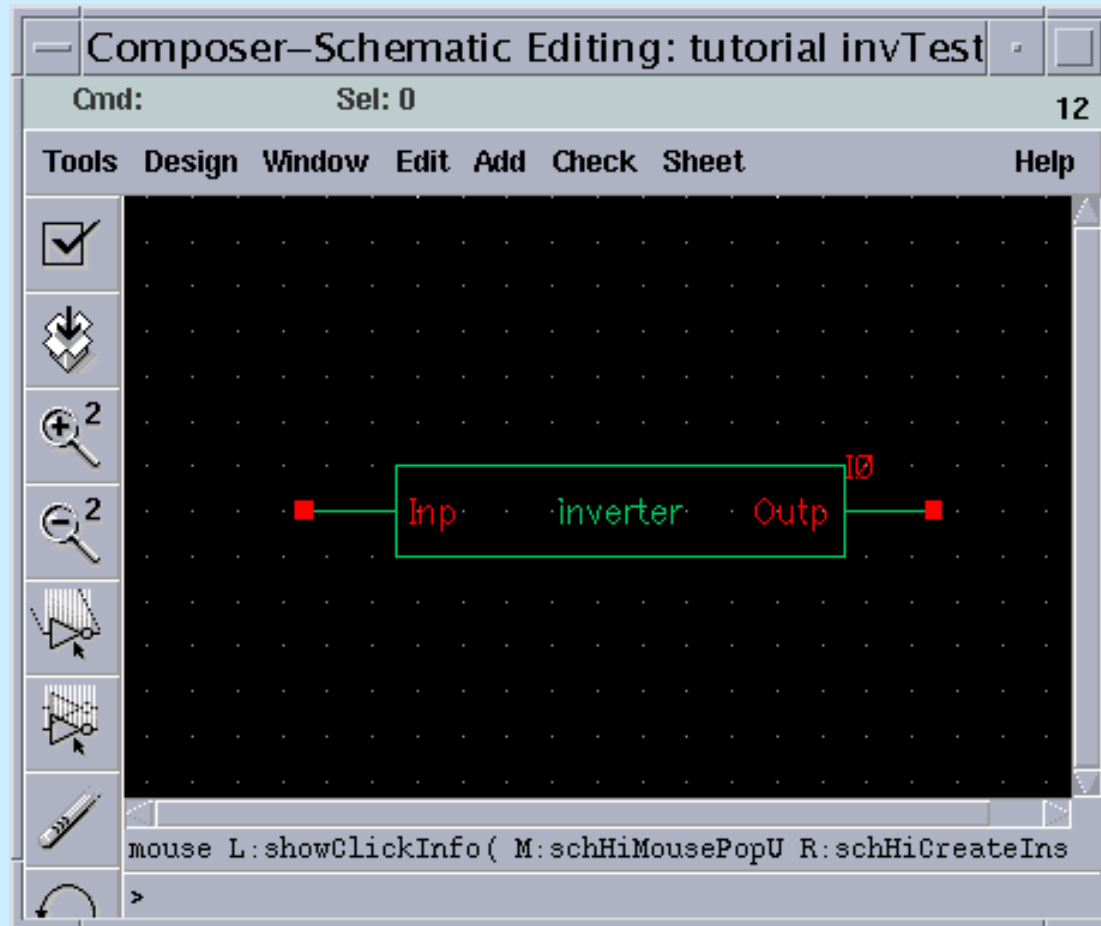
- After the library "tutorial" is selected, there will be a new list of
- components which are included in this library
 - every symbol that you created within this library will show up here.



By clicking on "inverter" in the component list in the *Component Browser*, you can pick up the symbol you created for the inverter

Simulation - Select and place components

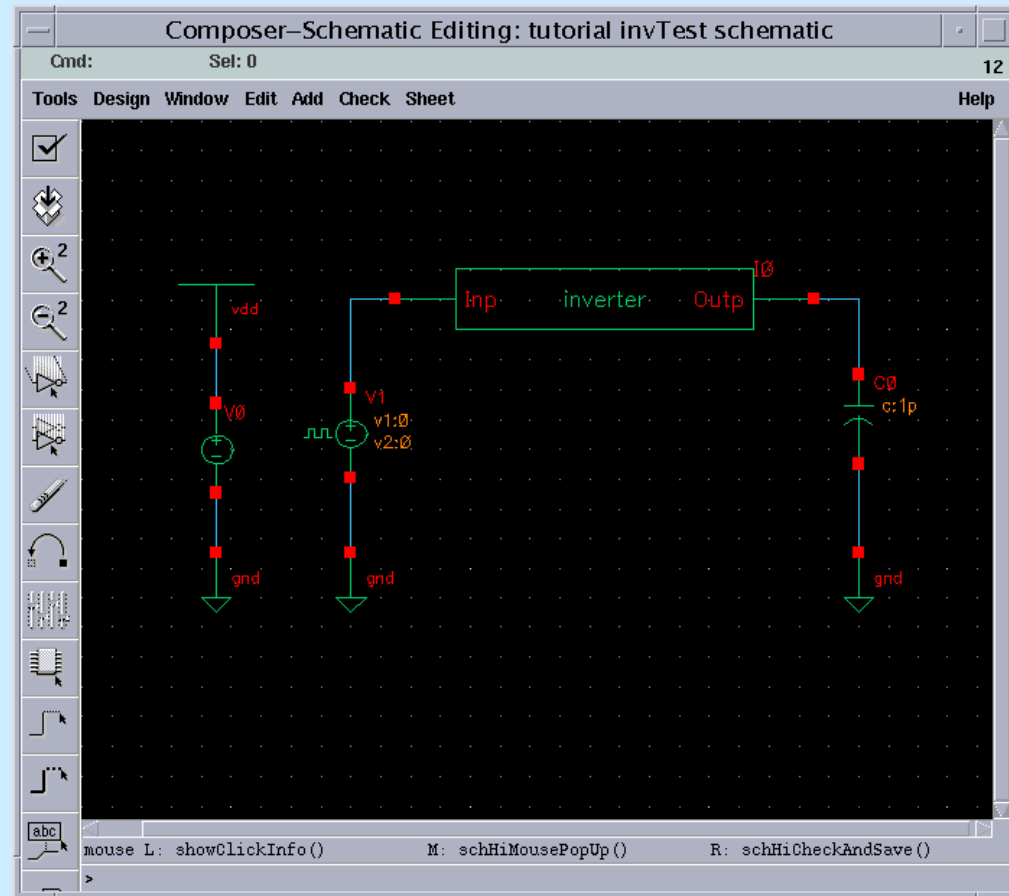
You can go to the schematic window and place the symbol of the inverter to a point by clicking on it



Simulation - Select and place components

Pick up and place the rest of the components required for the simulation.

- Place the supply nets, "vdd" and "gnd".
- Place the voltage sources, "vdc" and "vpulse".
- Place the capacitance which will be the output load, "cap".



Match placed componets as was showed on the picture. Use the same method as previously.

Simulation - Define the voltage source VDC

A DC-voltage source called "vdd" is required as the power supply voltage in all digital circuits.

The value of this voltage usually depends on the technology used.

Edit the **DC voltage** field in => the *Edit Object Properties* window and type the VDD value which is 3.3V

Edit Object Properties

OK Cancel Apply Defaults Previous Next Help

Apply To: ☐ only current ☐ instance

Show: ☐ system ☒ user ☒ CDF

Browse Reset Instance Labels Display

Property	Value	Display
Library Name	NCSU_Analog_Parts	☐ off
Cell Name	vdd	☐ off
View Name	symbol	☐ off
Instance Name	V	☐ off

Add Delete Modify

User Property	Master Value	Local Value	Display
IvsIgnore	TRUE		☐ off

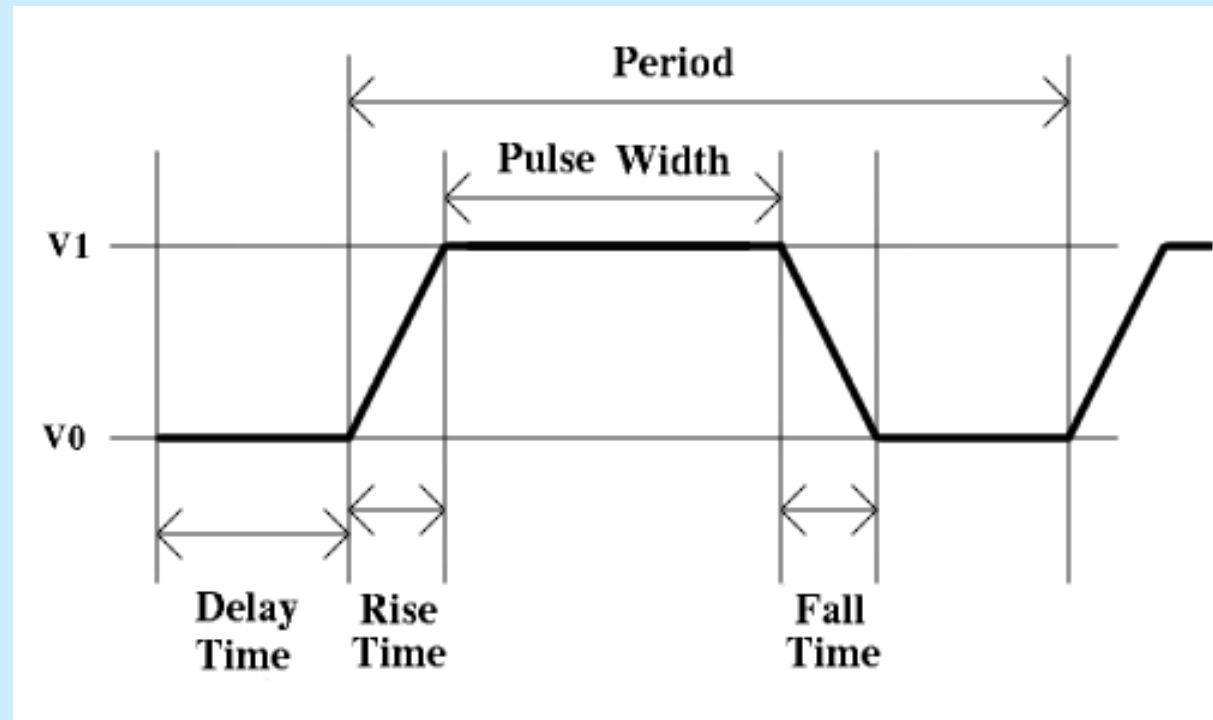
CDF Parameter Value Display

AC magnitude		☐ off
AC phase		☐ off
DC voltage		☐ off
Noise file name		☐ off
Number of noise/freq pairs		☐ off
Temperature coefficient 1		☐ off
Temperature coefficient 2		☐ off
Nominal temperature		☐ off

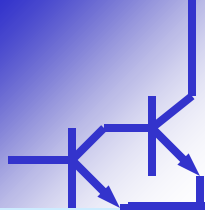
Simulation - Define the voltage source V_{pulse}

- The pulse generator is a voltage source which can produce pulses of any duration, period and voltage levels.
- This source will be used to generate the input data

How to use parameters to define the input pulse waveform? =>



Simulation - Define the voltage source Vpulse



The values for the => pulse generator parameters which are used to define the input waveform.

Change them using the method as previously.

OK	Cancel	Apply	Defaults	Previous	Next	Help
----	--------	-------	----------	----------	------	------

Apply To: ☐ only current ☐ instance ☐

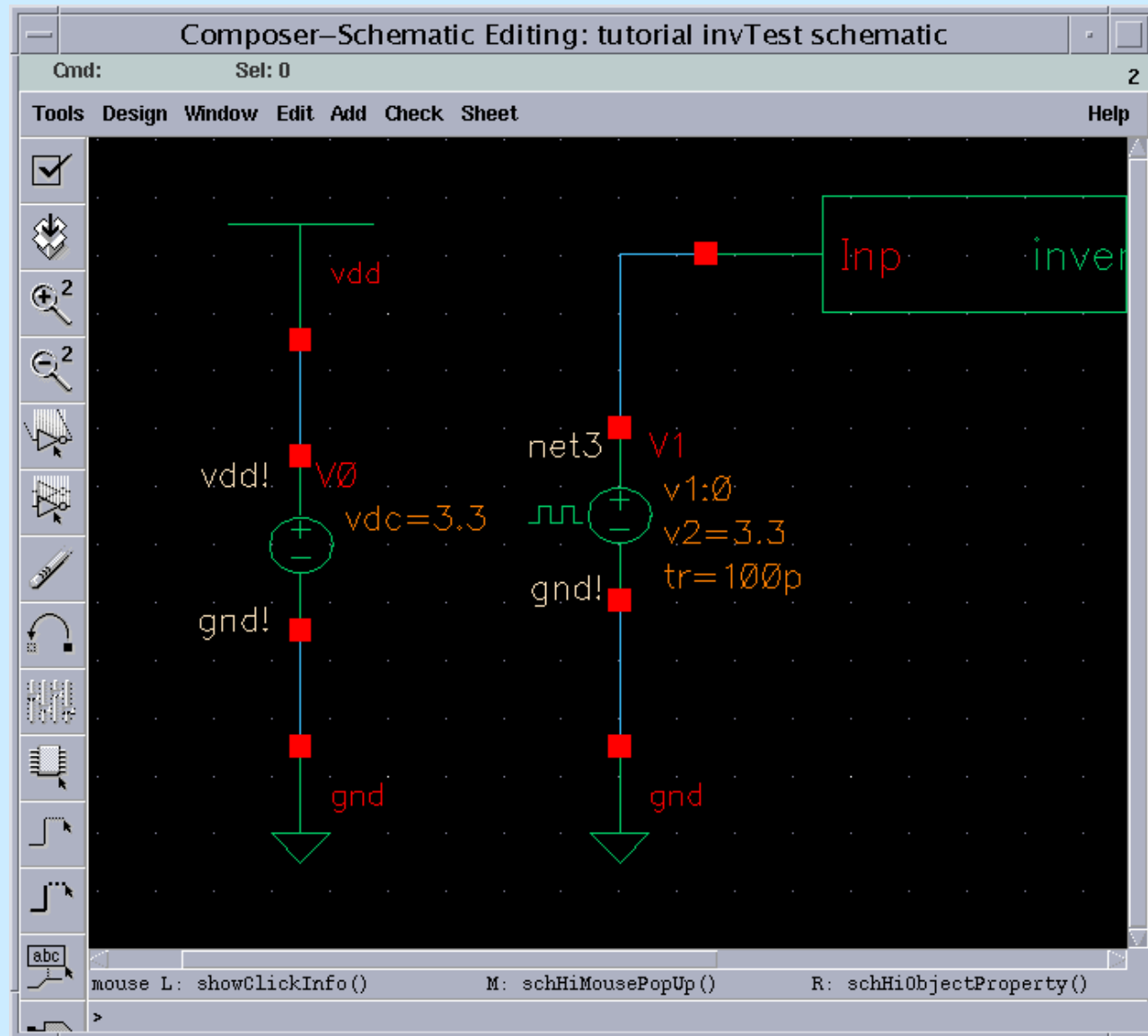
Show: ☐ system ☒ user ☒ CDF

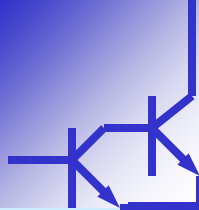
Browse		Reset Instance Labels Display	
Property	Value	Display	
Library Name	NCSU_Analog_Parts	off ☐	
Cell Name	vpulse	off ☐	
View Name	symbol	off ☐	
Instance Name	V1	off ☐	

User Property	Add		Delete		Modify		Display
	Master Value	Local Value	Master Value	Local Value	Master Value	Local Value	
Ivsignore	TRUE						off ☐

CDF Parameter	Value	Display
AC magnitude		off ☐
AC phase		off ☐
Voltage 1	0 V	off ☐
Voltage 2	3.3 V	off ☐
Delay time	3n s	off ☐
Rise time	100p s	off ☐
Fall time	100p s	off ☐
Pulse width	5n s	off ☐
Period	12n s	off ☐

Simulation - Define the voltage source - results





Simulation - Determine the output load

Edit the properties of the capacitor which is the output load of the inverter.

Change capacitance =>
from the default value
(1 pF) to 25 fF

Edit Object Properties

OK Cancel Apply Defaults Previous Next Help

Apply To ☐ only current ☐ instance

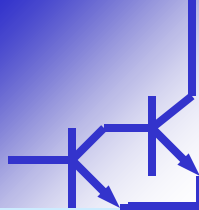
Show ☐ system ☒ user ☒ CDF

Browse Reset Instance Labels Display

Property	Value	Display
Library Name	NCSU_Analog_Parts	☐ off
Cell Name	cap	☐ off
View Name	symbol	☐ off
Instance Name	C0	☐ off

Add Delete Modify

CDF Parameter	Value	Display
Capacitance	25f F	☐ off
Initial condition		☐ off
Model name		☐ off
Width		☐ off
Length		☐ off
Multiplier	1	☐ off



Simulation - Adding labels

- labeling a node = adding names to the wires.
- it allow to observe important nodes (or wires) during simulations.
- adding pins (during drawing the schematic) $\neq$ labeling a node

How can I do it ?

First, select *Wire Name* in the *Add* command list. =>

Tools Design Window Edit Add Check Sheet

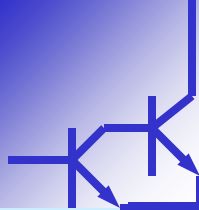
Component ...	i
Wire (narrow)	w
Wire (wide)	W
Wire Name ...	I
Pin ...	p
Block ...	b
Solder Dot	
Note	▶

Simulation - Adding labels

- type all the label names one after the other in the *Names* field
- there isn't any information related to the direction of the nodes - only the pins are defined with a direction.

The image displays two side-by-side screenshots of the 'Add Wire Name' dialog box in a circuit simulation software. Both windows have a title bar 'Add Wire Name' and buttons for 'Hide', 'Cancel', 'Defaults', and 'Help'. The 'Names' field is a text input area. In the left window, it is empty. In the right window, it contains the text 'in out'. Below the 'Names' field, there are settings for 'Font Height' (0.0625), 'Font Style' (stick), 'Justification' (lowerCenter), 'Entry Style' (fixed offset), 'Bus Expansion' (off), 'Placement' (single), and 'Purpose' (label). A 'Show Offset Defaults' button is also present. At the bottom of each window is a 'Rotate' button.

We will label the two wires as "in" and "out".

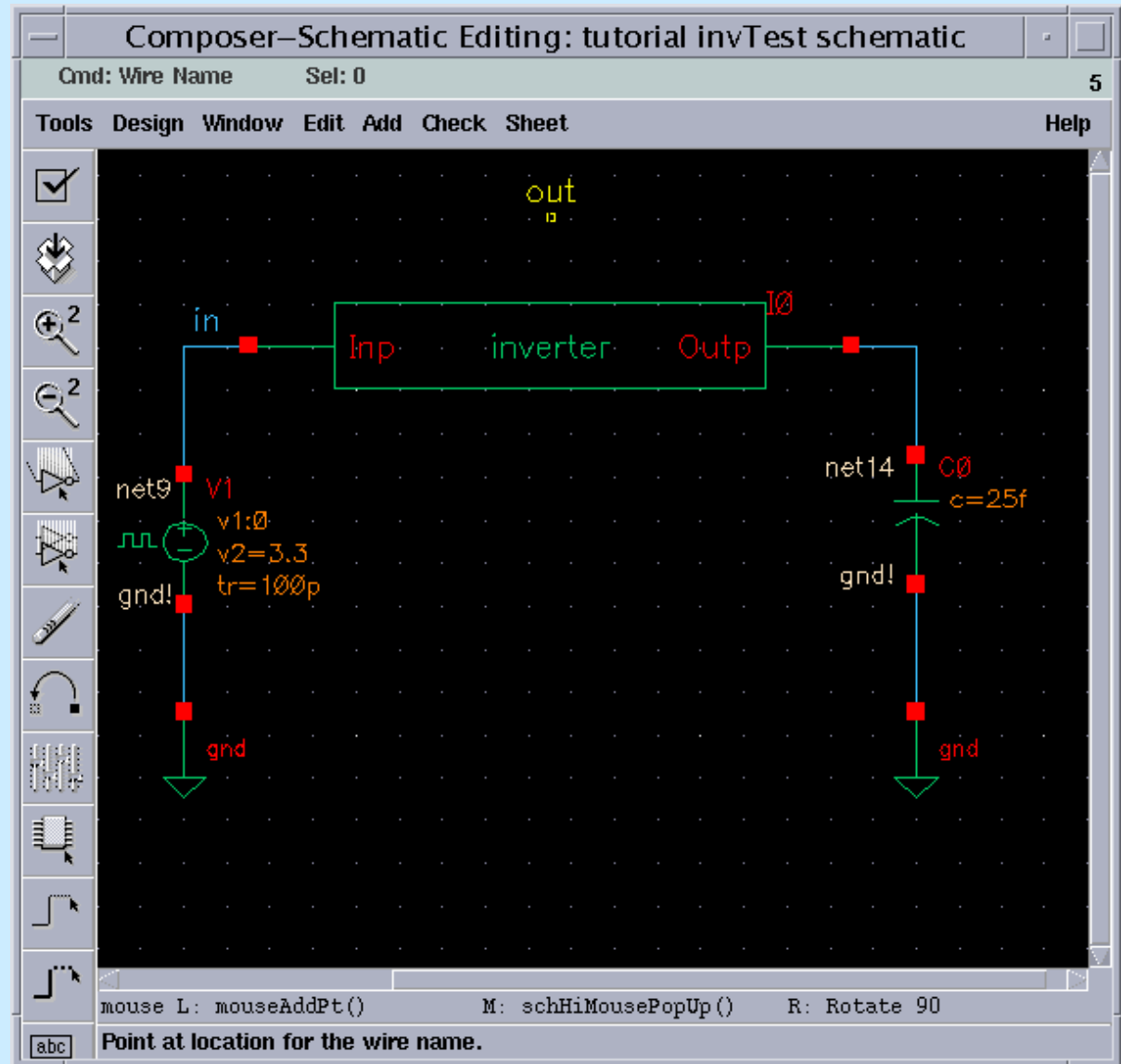


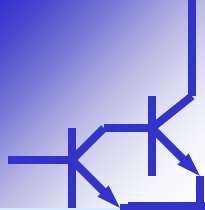
Simulation - Adding labels

- After all the labels are typed, move the mouse cursor on the schematic
- You will see the first label floating with the mouse cursor. Click on the corresponding net to name the net with this label.
- As soon as you put the first label, the second label will appear on the mouse cursor.
- This procedure is repeated until you are finished putting all label names you entered in the *Add Label* window.

Simulation - Adding labels results

Note: Save your design by using *Check and Save* in the *Design* command list. Be sure that the CIW doesn't report any errors or any warnings.





Simulation - Open the simulator window

Tools Design Window Edit Add Check Sheet

Analog Artist

Datapath/Schematic

Design Synthesis ▶

Diva

Floorplan/Schematics

Hierarchy Editor

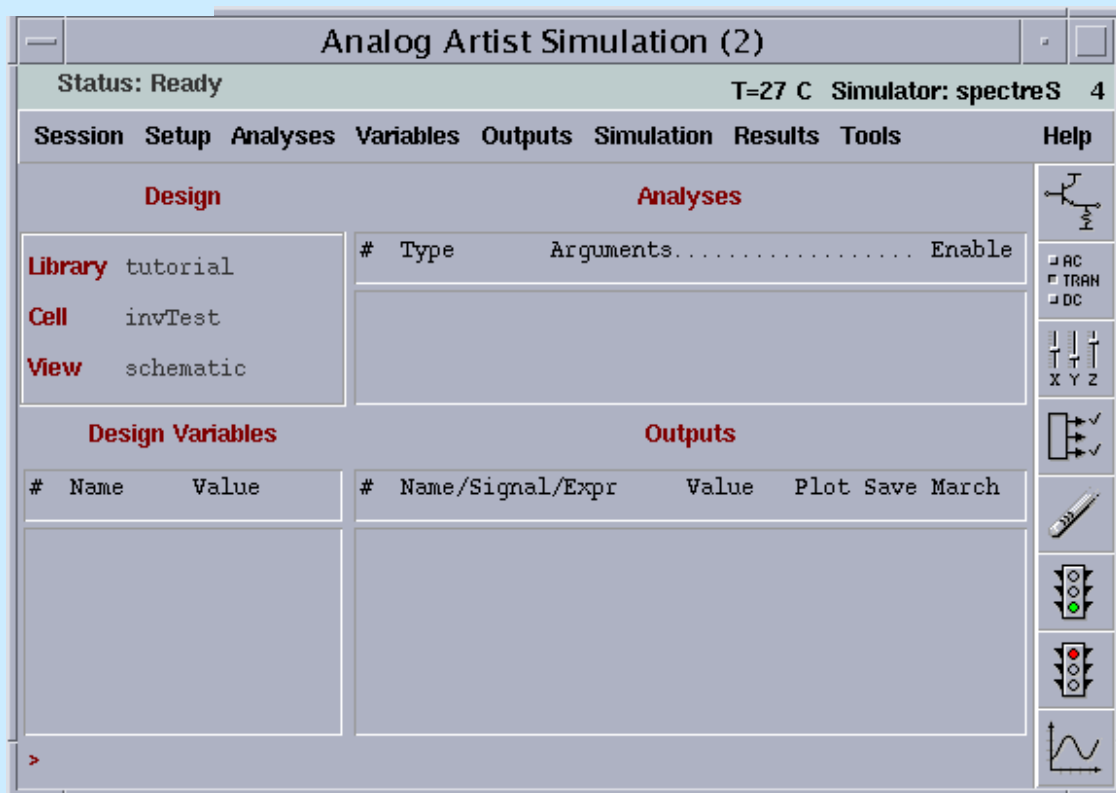
Mixed Signal Opts.

Schematics

Simulation ▶

Vampire

<= Open the *Analog Artist* window.



Simulation - Edit the Simulation Parameters

Session Setup Analyses Variables Outputs Simulation Results Tools

Choose ...

Delete

Enable

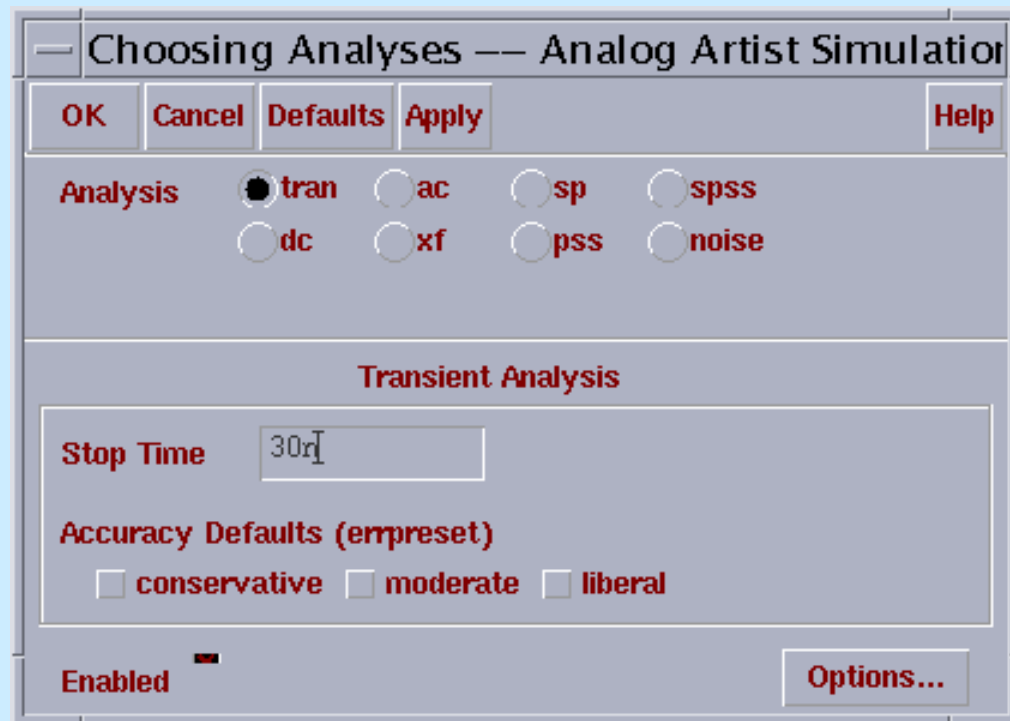
Disable

- there are many available analysis options you can choose.
- each of these options provides a specific sub-region within the *Choosing Analysis* window.

We want to obtain the delay information for the inverter, we choose the transient simulation type, so that the output can be traced in time domain.

Simulation - Edit the Simulation Parameters

In the *Transient Analysis* region, type a value in the *Stop Time* field to determine how long the simulation will take place.



Simulation - Run the Simulation

Session Setup Analyses Variables Outputs Simulation Results Tools

Setup ...

Delete

To Be Saved ▶

To Be Marched ▶

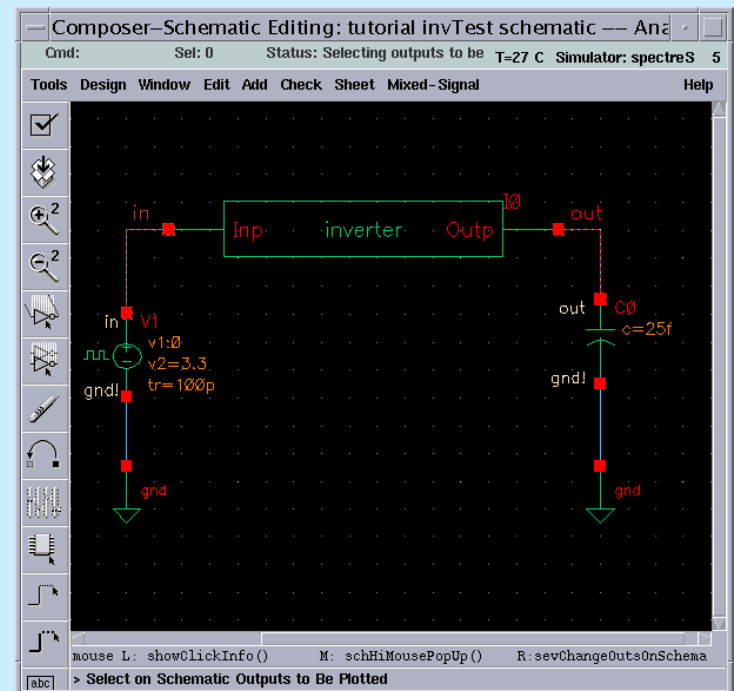
To Be Plotted ▶

Select On Schematic

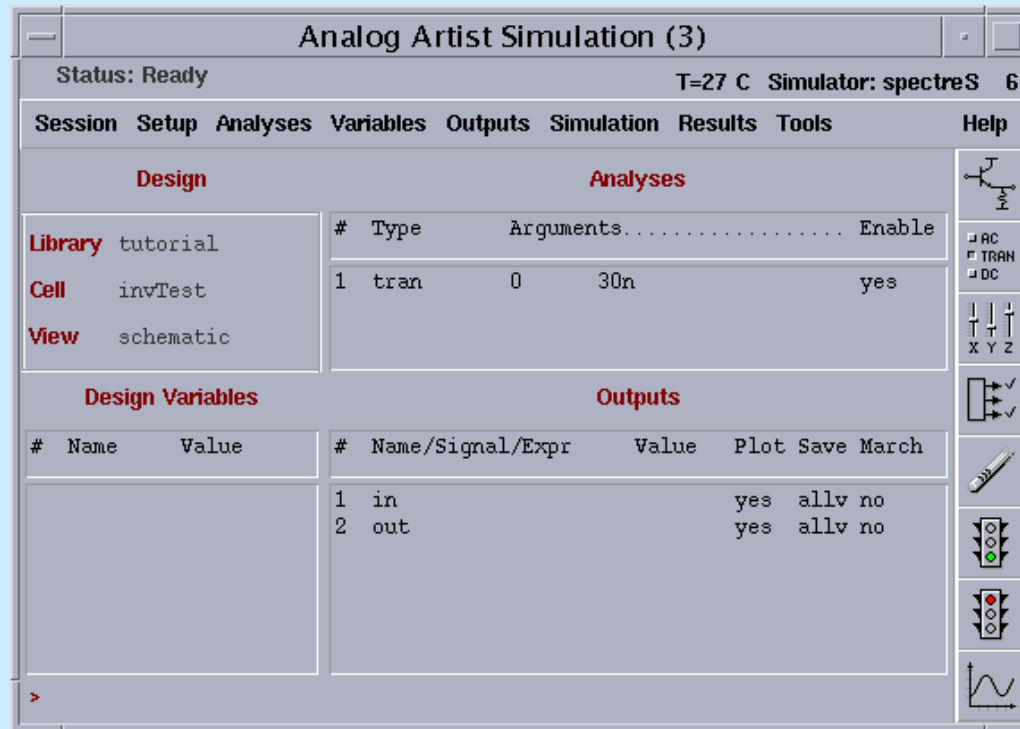
Add To

Remove From

- click on *Outputs* in the *Analog Artist Simulation* menu banner
- select *To Be Plotted* and then *Select on Schematic*.
- when the schematic window becomes automatically active, **select the nodes to be observed**



Simulation - Run the Simulation

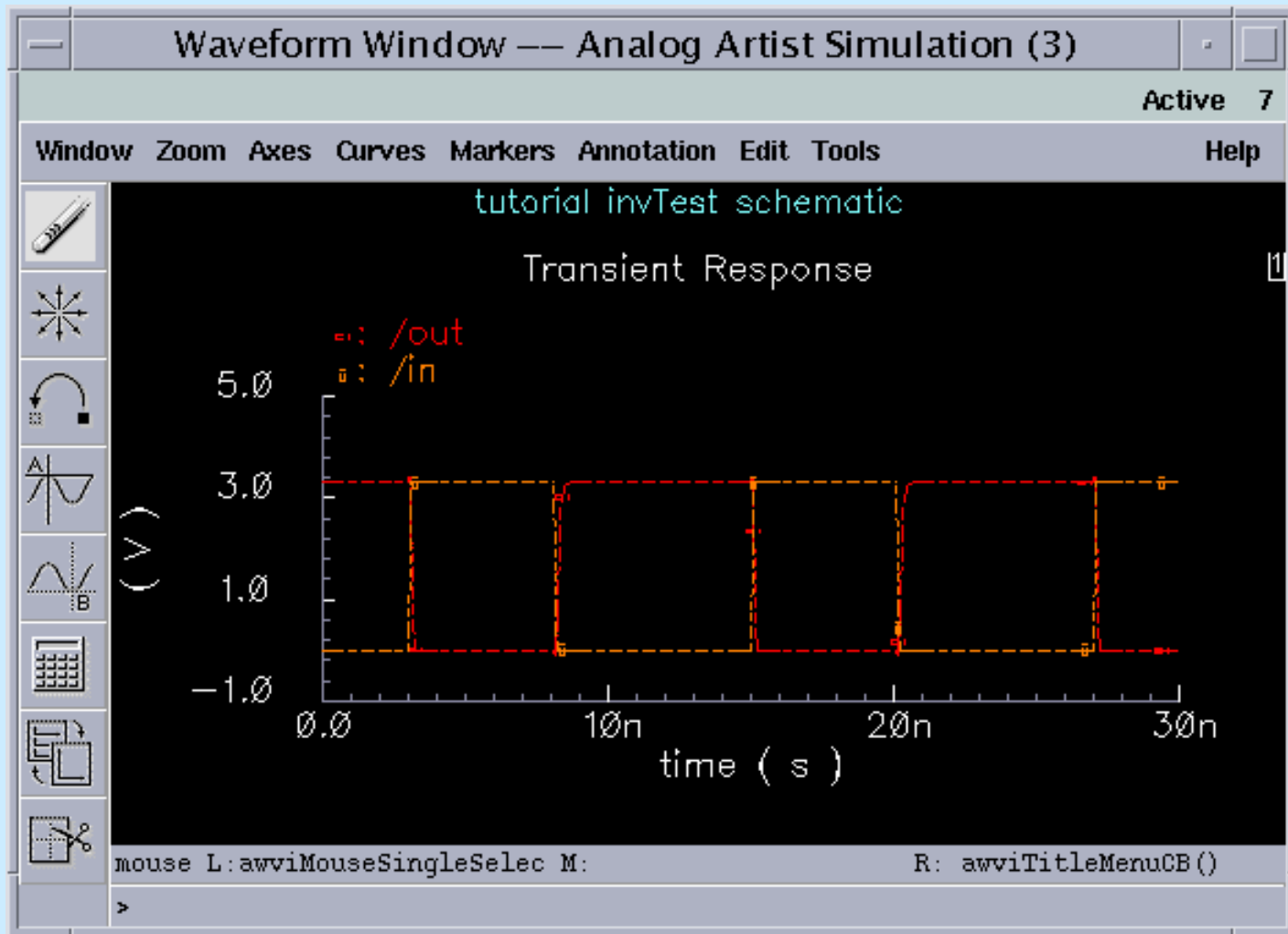


Session Setup Analyses Variables Outputs Simulation Results Tools

- Run
- Stop
- Options
- Netlist
- Command Type-In ...
- Output Log ...
- Convergence Aids

< = Start the simulation by clicking *Simulation* and then selecting *Run*.

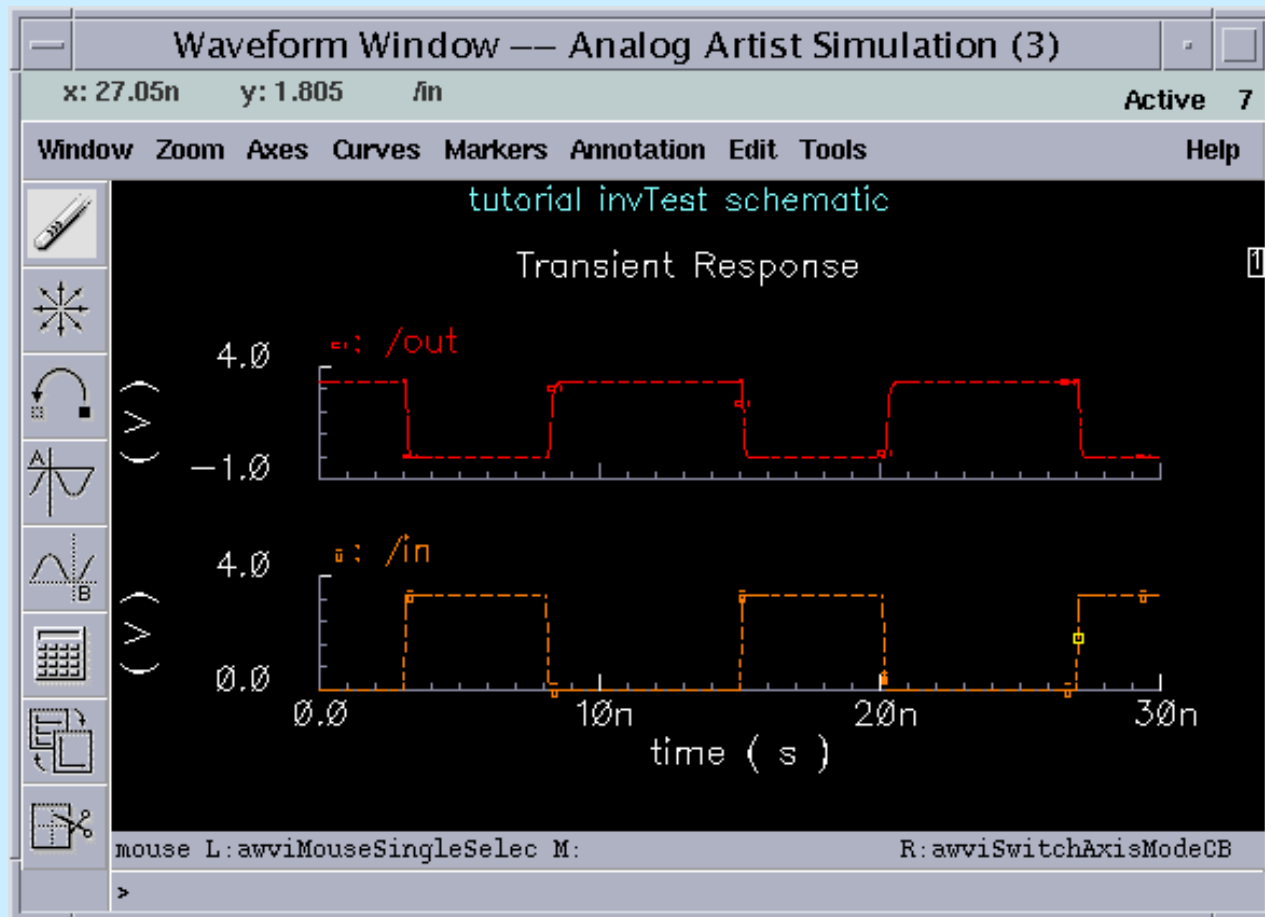
Simulation - Run the Simulation

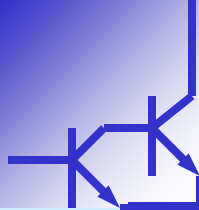


The waveform window appears after the simulation is completed.

Simulation - Run the Simulation

To separate the waveforms, from the menu
Axes select option To Strip..





Simulation - Re-run the Simulation

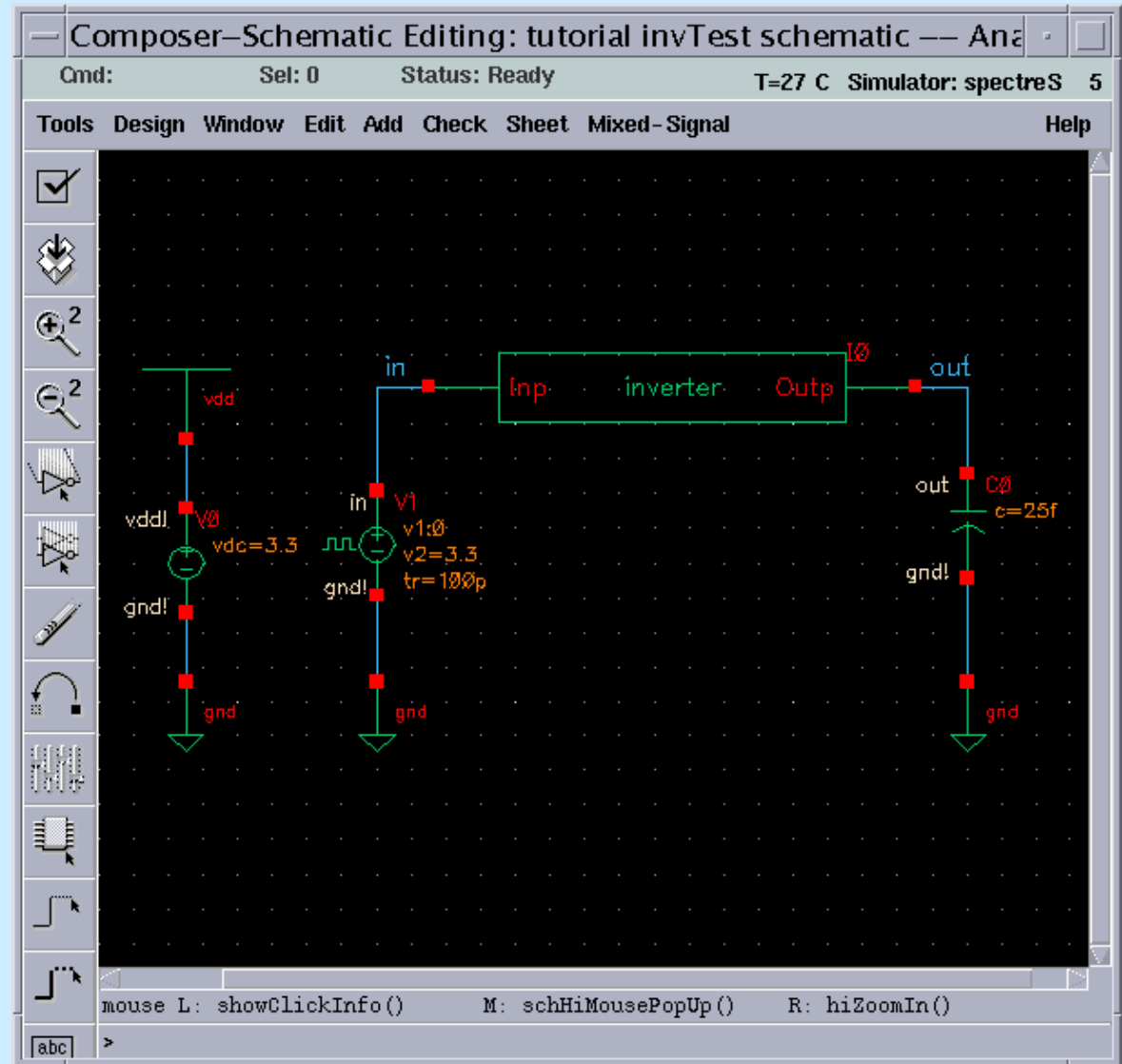
If you are not satisfied with the simulation results, there are two different aspects that can be modified :

- **The simulation environment is not satisfactory.**
This means that the setup to simulate your design should be modified. Make sure that the power supply voltages are connected properly.
- **You have to modify your circuit design.**
Usually, you will need to change the W/L ratios of the transistors to meet your design specifications.

Simulation - Re-run the Simulation

How to re-run the simulation after editing ?

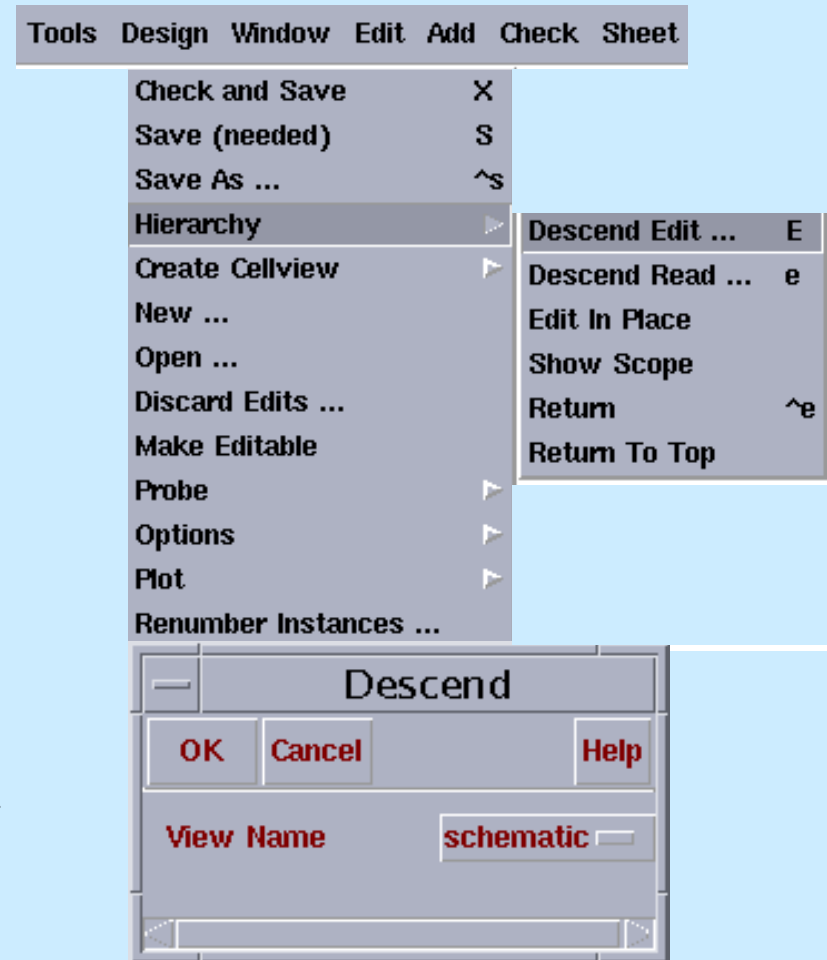
Go back to the => schematic window and select the symbol of your design.



Simulation - Re-run the Simulation

Click on *Design* in the => menu banner, select *Hierarchy* and then *Descend Edit*.

Click on OK in the *Descend* window which asks the designer which view of the design is to be => edited.



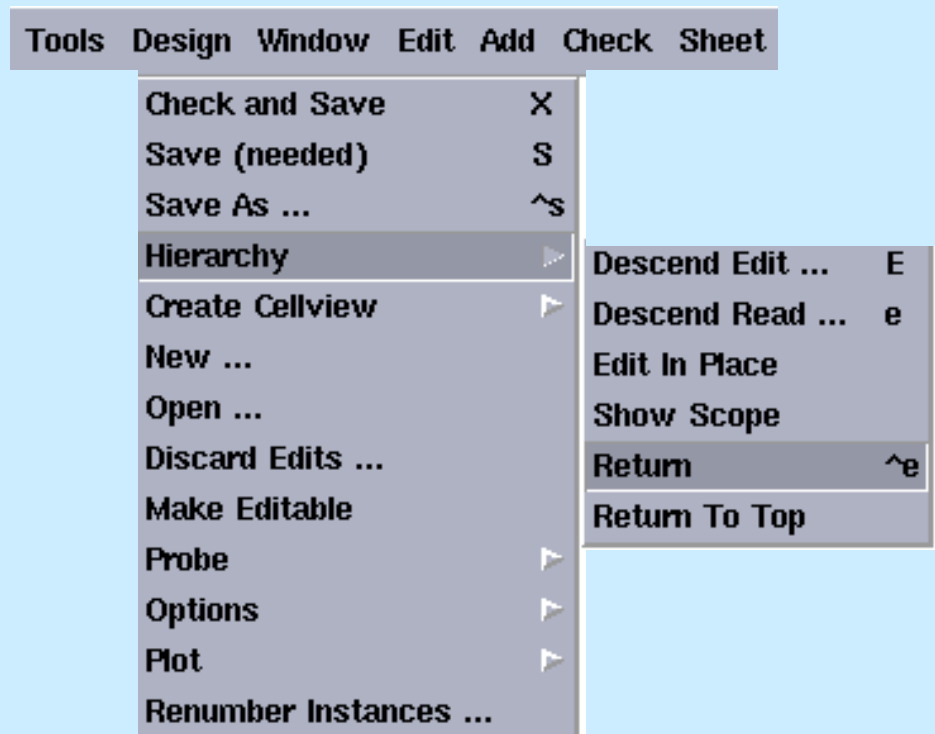
The existing schematic window now displays the schematic view for the inverter, by going one level down through the design hierarchy.

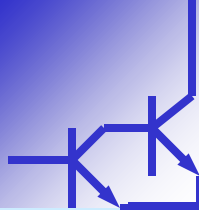
Simulation - Re-run the Simulation

- Make the appropriate changes in the editable schematic of the design. *To change the existing W/L ratio for a specific transistor, you have to edit its object properties.*

- Check and save your new schematic.

- Click on Design in the menu banner, select Hierarchy and then Return.



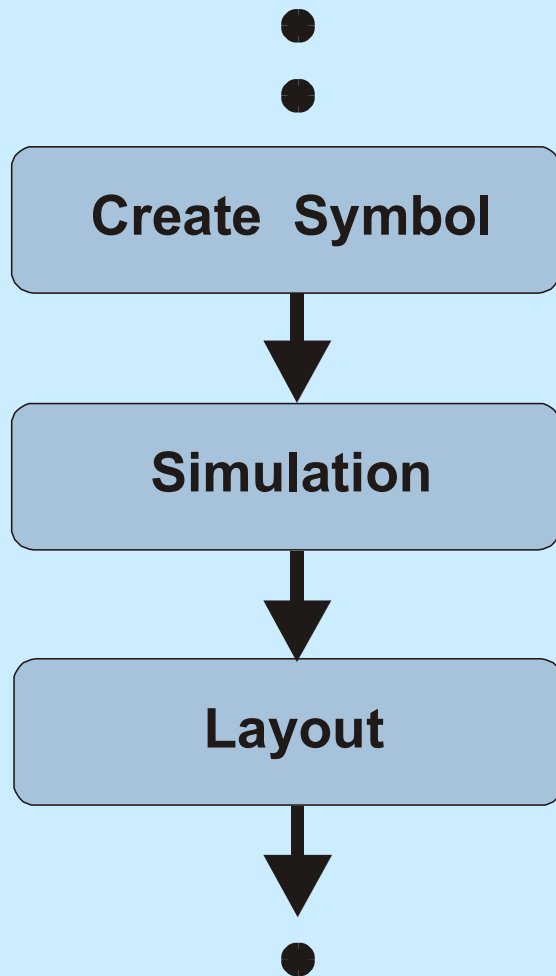


Simulation - Re-run the Simulation

Go to the *Analog Artist* window and run the simulation again.

- As the simulation runs, you can switch to the waveform window, because the waveforms will be updated after the simulation is finished.
- You can iterate on your design as described in this section of the tutorial.
- When you want to end the simulation, quit the *Analog Artist* simulator. This will automatically close the *Waveform* window, too.

Mask Layout

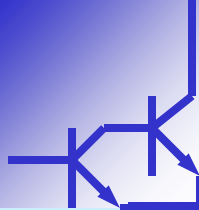


- The mask layout is one of the most important steps in the full-custom (bottom-up) design flow.

- It describes the detailed geometries and the relative positioning of each mask layer to be used in actual fabrication.

- Physical layout design is very tightly linked to overall circuit performance.

- The detailed mask layout of logic gates requires a very intensive and time-consuming design effort.



CMOS Inverter Layout

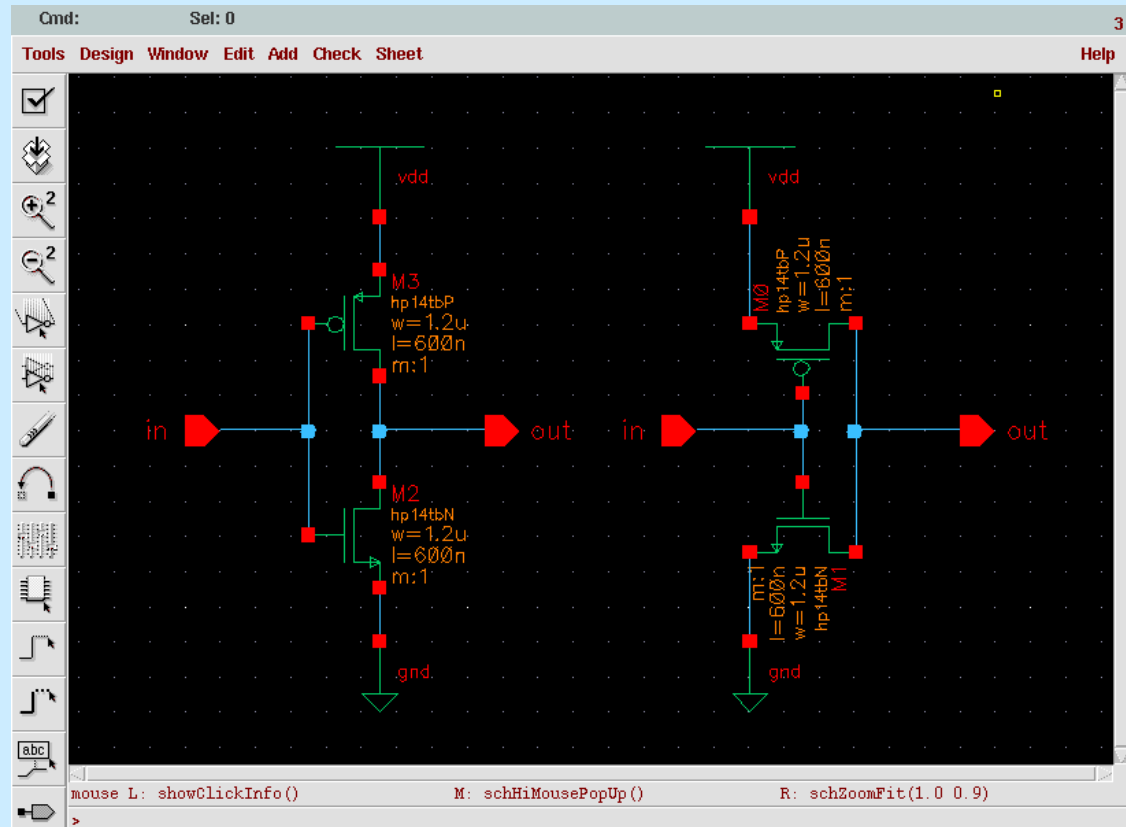
Design Idea

To draw the mask layout of a circuit, two main items are necessary at the beginning:

1. A circuit schematic
2. A signal flow diagram

Circuit Schematic

The layout is drawn according to the schematic (and not the other way around).

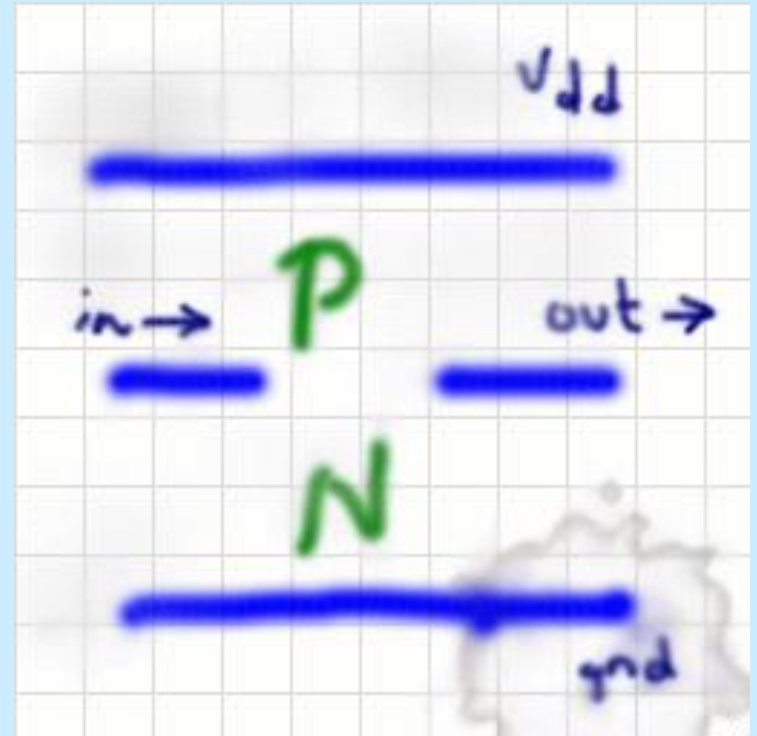


While both schematics are identical, the one on the right is drawn in a way to resemble the final layout.

Signal Flow Diagram

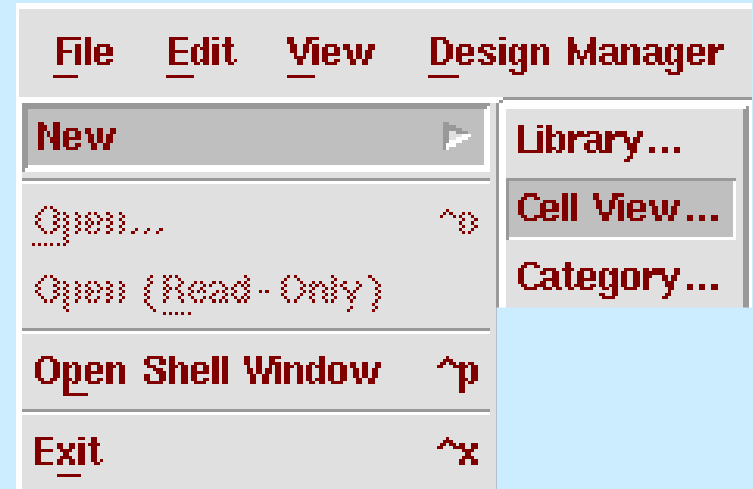
The most important factor determining the actual layout is the signal flow.

The signal flow diagram is just a concept that you can visualize for a particular circuit.

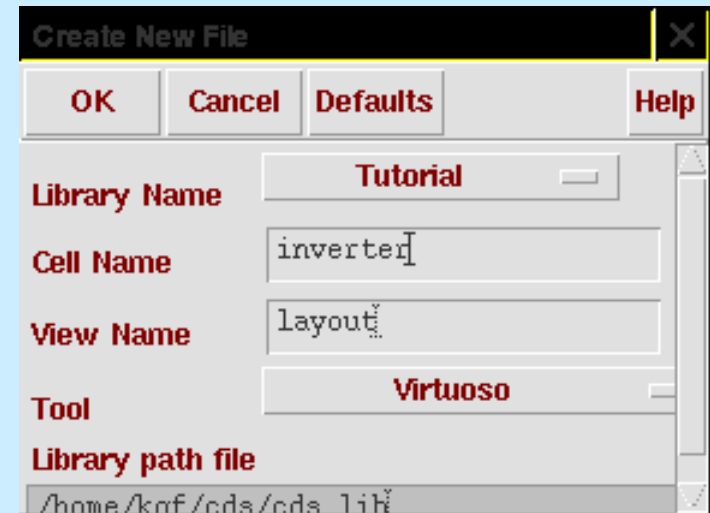


Create Layout Cellview

1. From the Library Manager :
File --> New --> Cellview



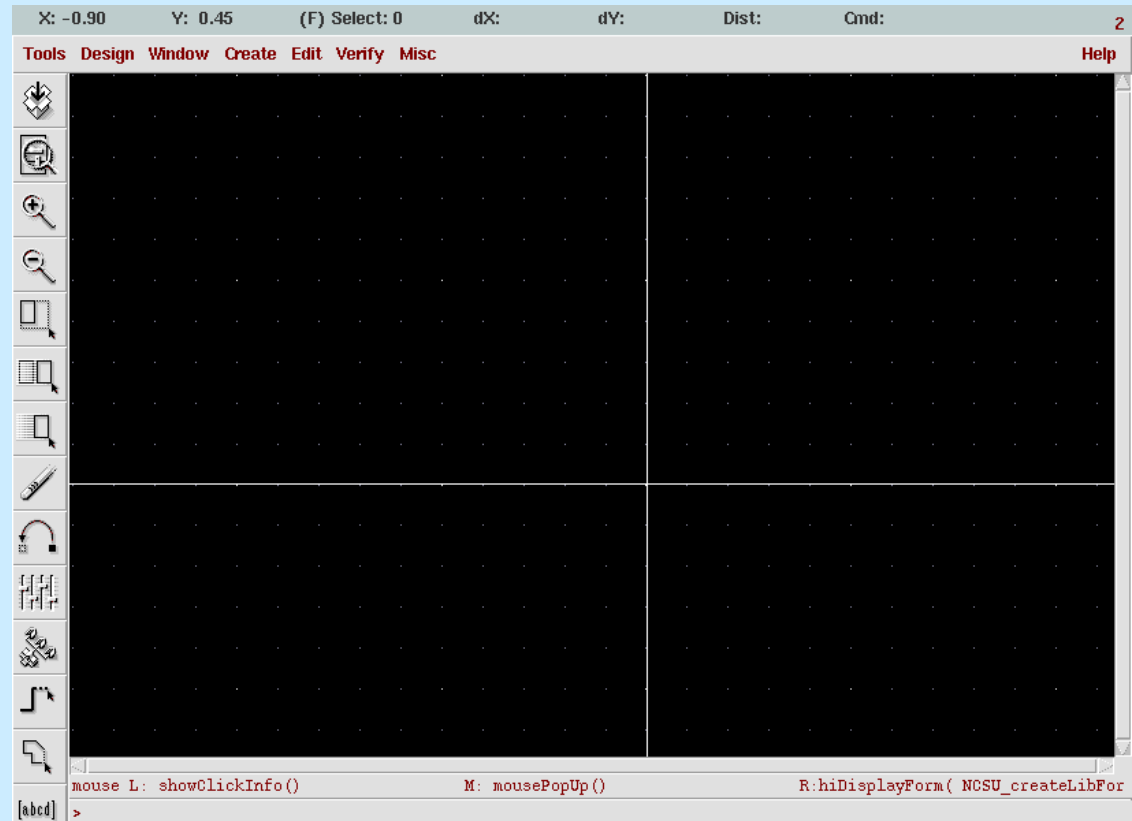
2. Enter cellname and choose
layout cellview



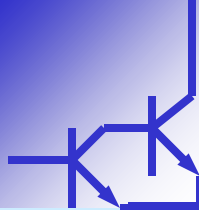
Virtuoso and LSW

Two design windows will pop-up after you have entered the design name.

LSW

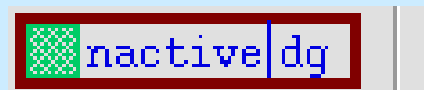


Virtuoso

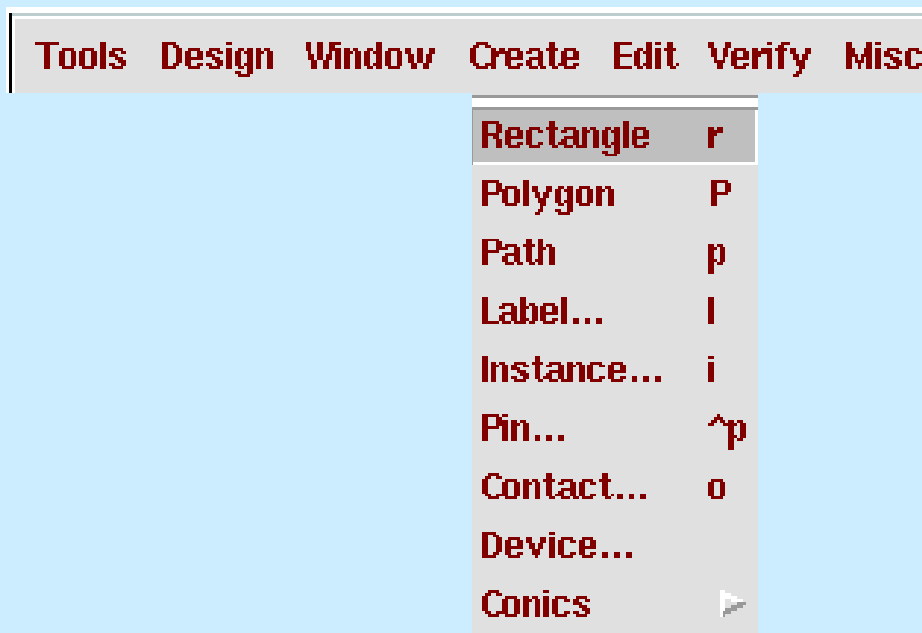


Drawing the N-Diffusion (Active)

1. Select *nactive* layer from the LSW



2. From the *Create* menu
in Virtuoso select
Rectangle
(Create --> Rectangle)

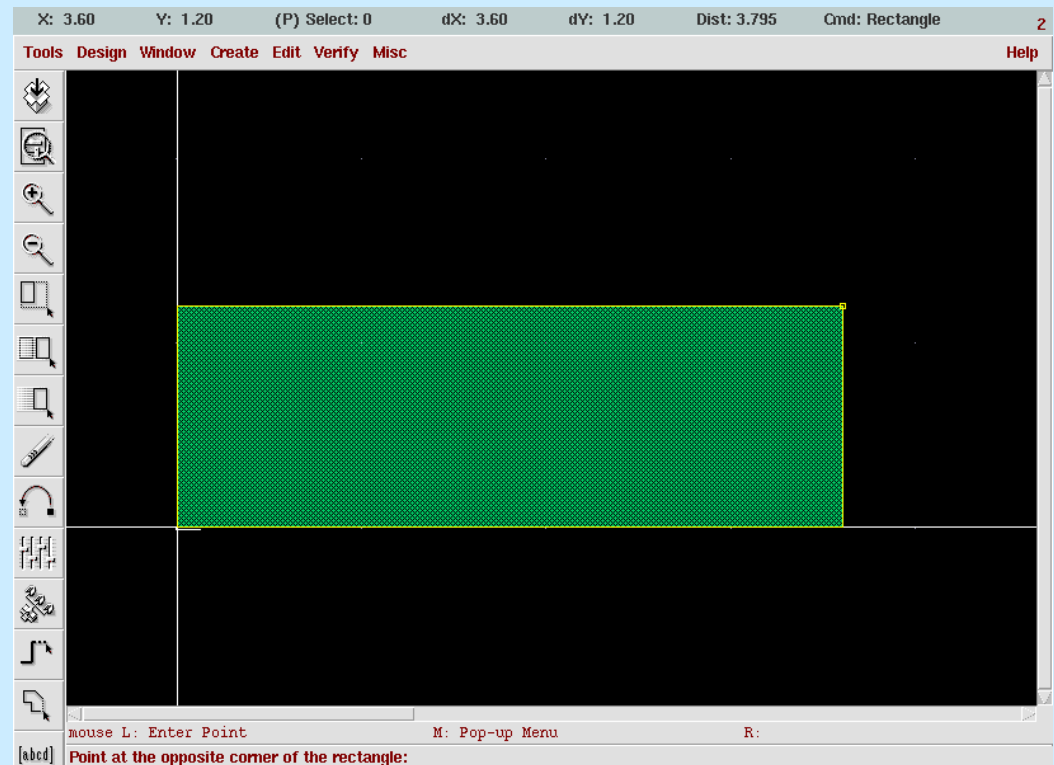


Drawing the N-Diffusion (Active)

3. Draw the box

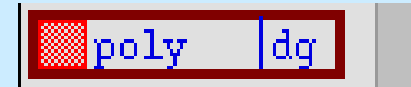
Select the first corner of rectangle in the layout window, click once, and then move the mouse cursor to the opposite corner.

- A grid of half a lambda is used



The Gate Poly

1. Select *poly* layer from the LSW



2. From the menu *Misc* choose *Ruler*
(*Misc* --> *Ruler*)

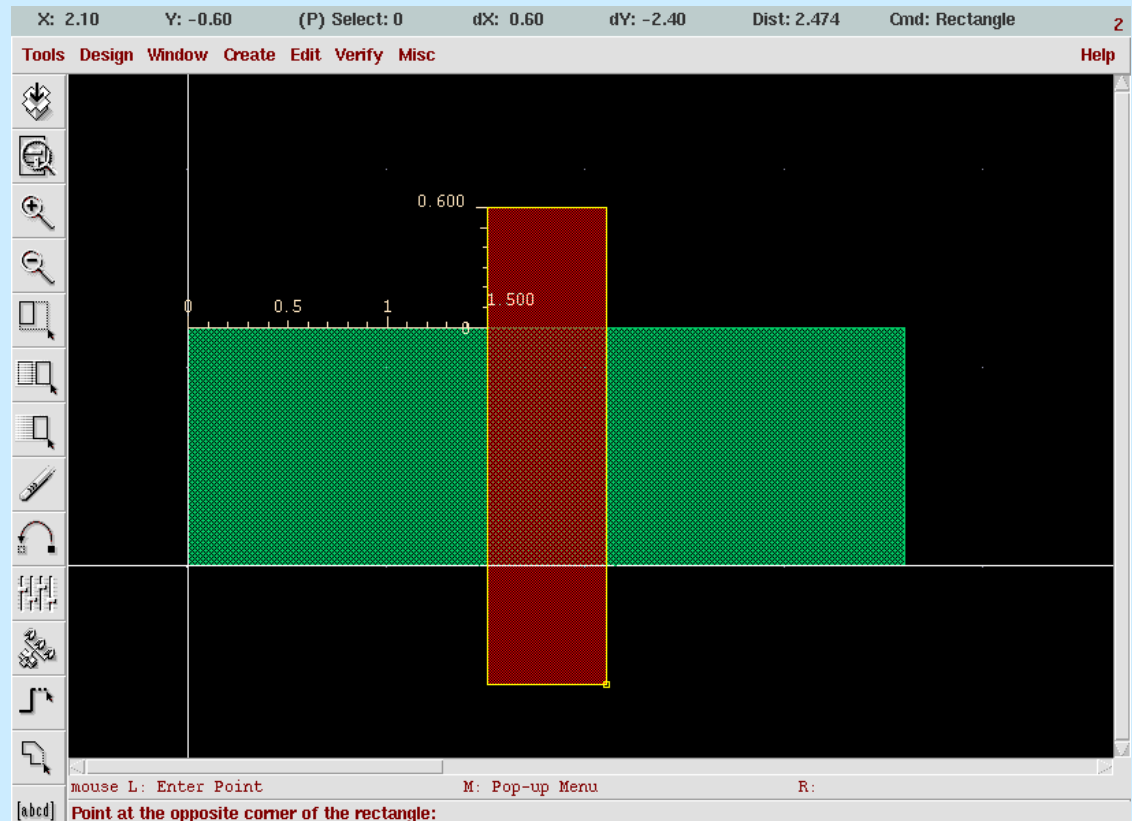


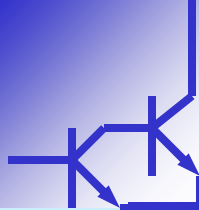
! The ruler is a very handy function.

The Gate Poly

3. Draw poly rectangle

Design rules tell us that poly must extend at least by 0.6μ (2 Lambda) from edge of diffusion

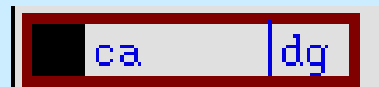




Making Active Contacts

Contacts will provide access to the drain and source regions of the NMOS transistor.

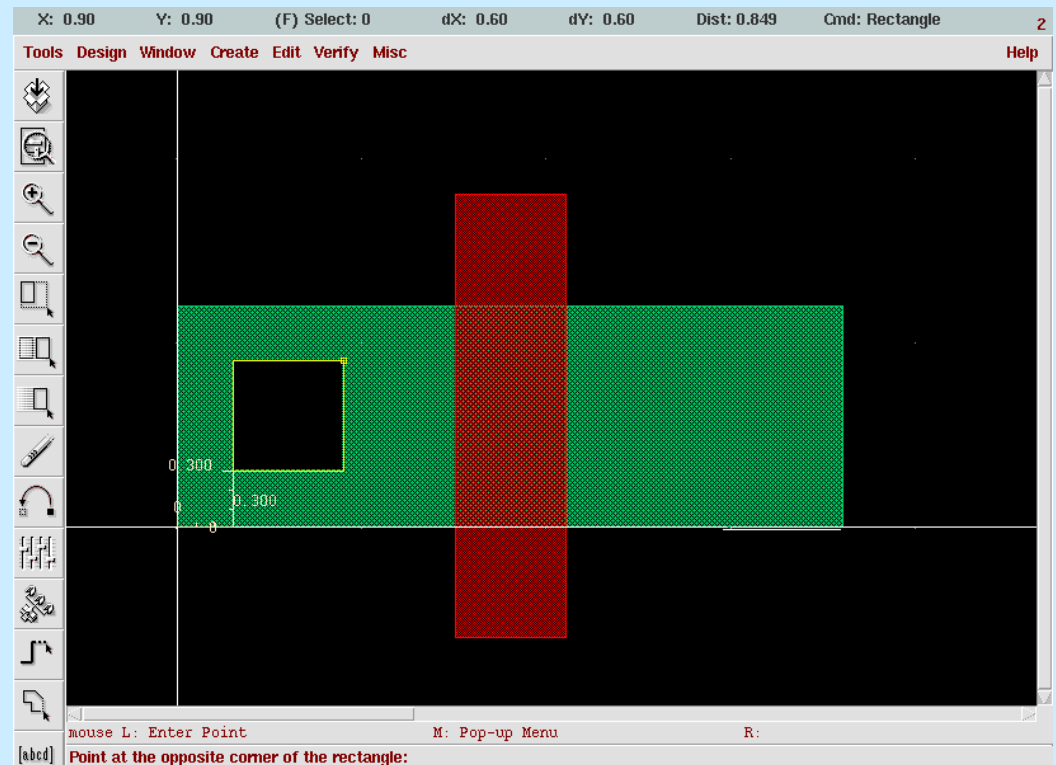
1. Select the *ca* (Active Contact) layer from the LSW.



Making Active Contacts

2. Use the ruler to pinpoint a location $0.30u$ from the edges of diffusion.

3. Create a square with a width and height of $0.6u$ within the active area.

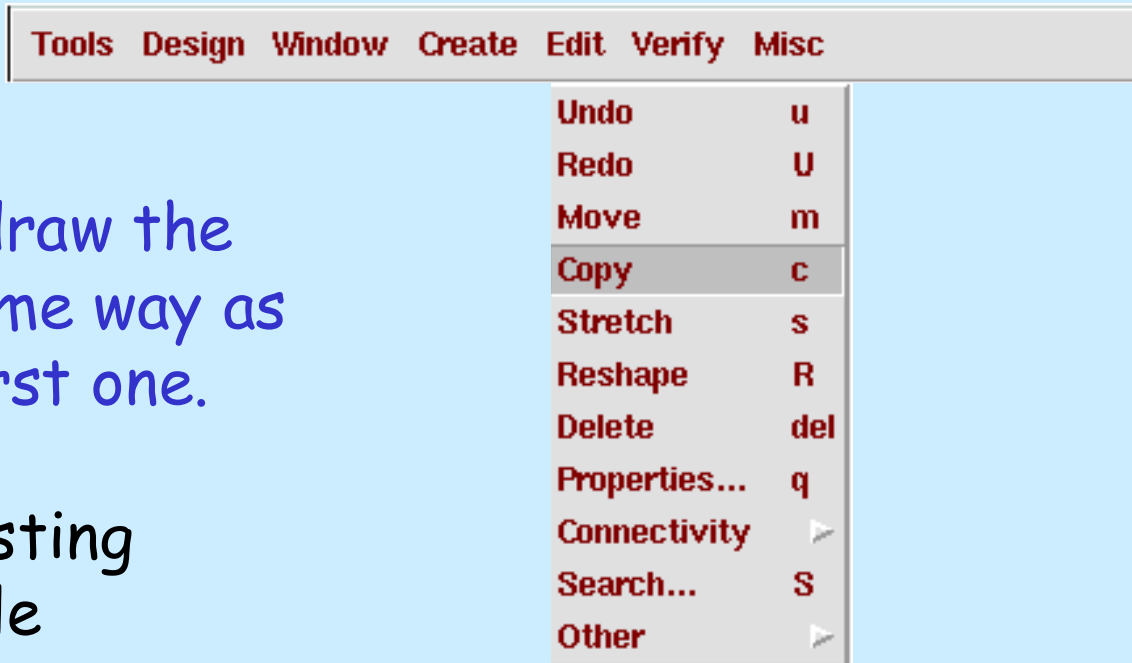


Making Active Contacts

4. From the *Edit* menu choose *Copy*
(Edit --> Copy)

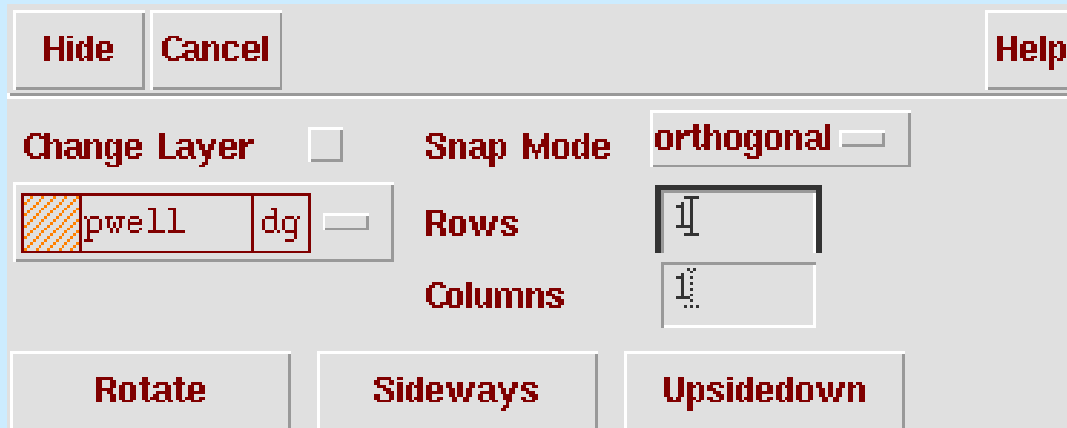
• You could choose to draw the second contact the same way as you have drawn the first one.

• However, copying existing features is also a viable alternative.



Making Active Contacts

When the *Snap Mode* is in *orthogonal* setting the copied objects will move only along one axis.

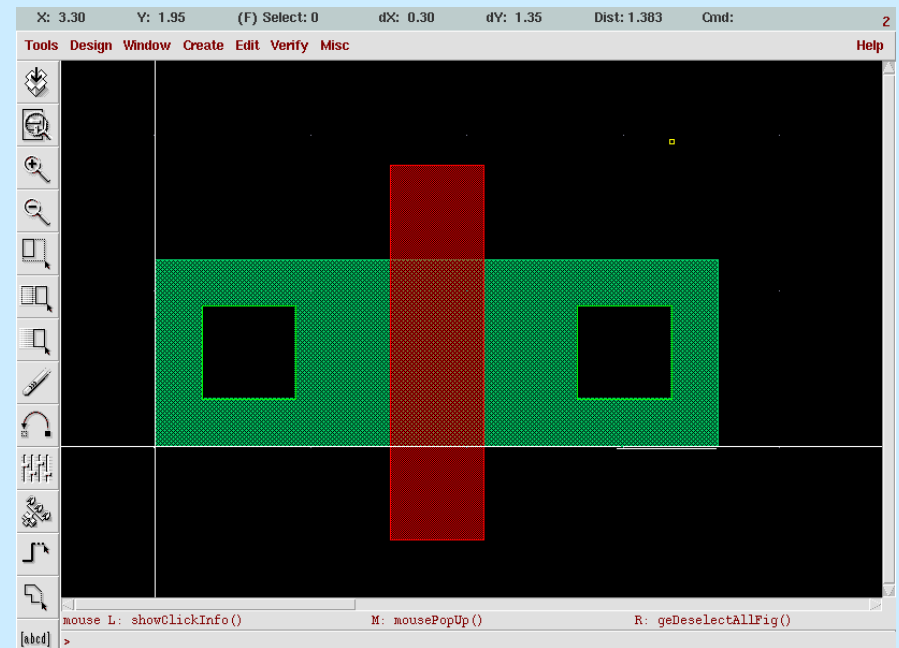
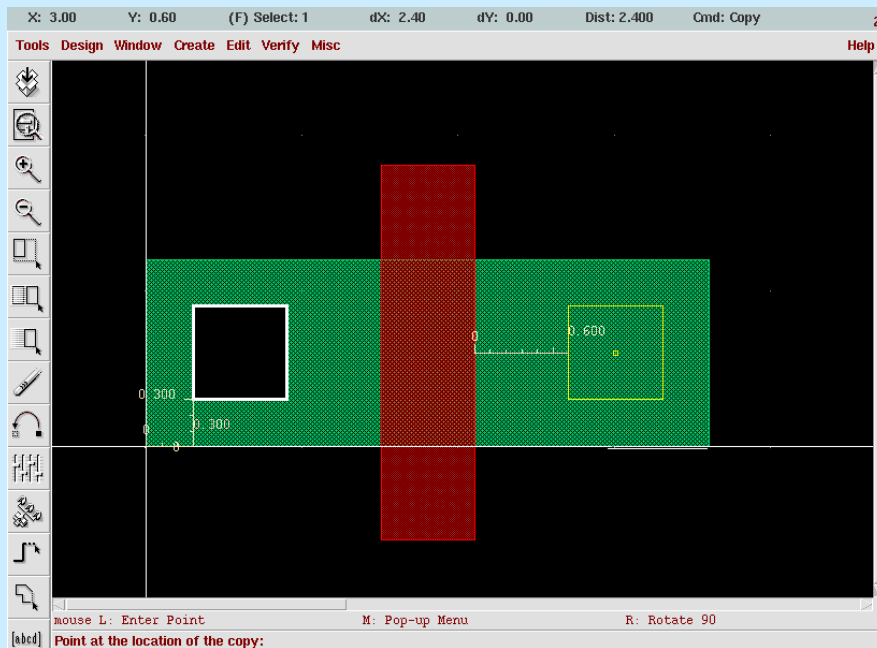


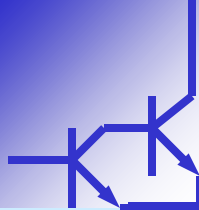
Copy dialog box.

Making Active Contacts

5. Copy the contact

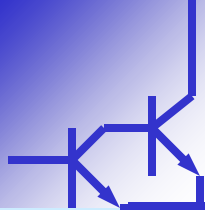
- Select the object (click in the contact- the outline of contact will attach to your cursor).
- Move the object and click at the final location.





Covering Contacts with Metal-1

- Active contacts define holes in the oxide (connection terminals).
- The actual connection to the corresponding diffusion region is made by the Metal layer.

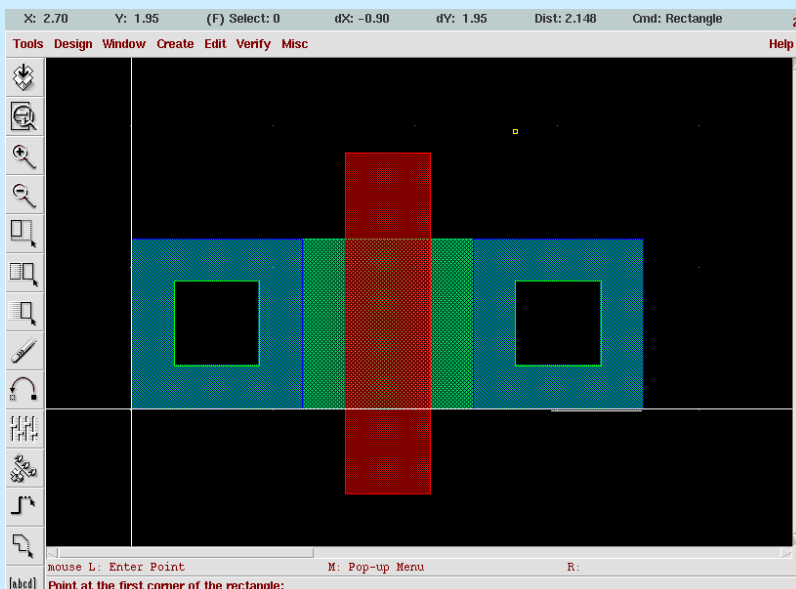


Covering Contacts with Metal-1

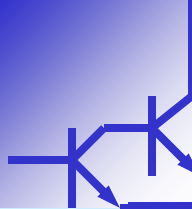
1. Select layer *Metal-1* from the LSW



2. Draw two rectangles 1.2u wide to cover the contacts



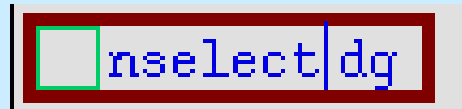
Note that Metal-1 has to extend over the contact in all directions by at least 0.3 u (1 lambda).



The N-Select Layer

Each diffusion area of each transistor must be selected as being of n-type or p-type.

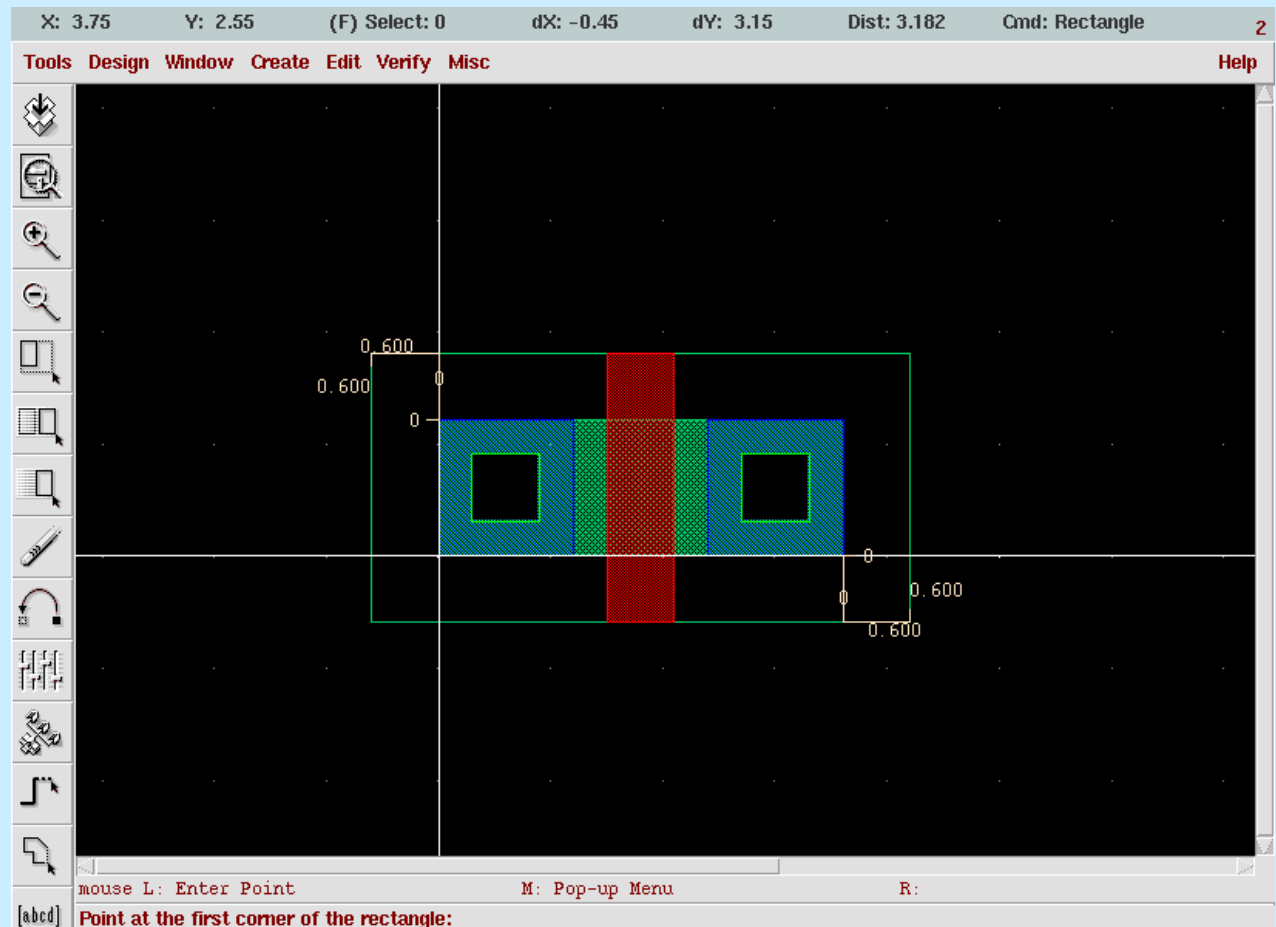
1. Select *nselect* layer from the LSW.



The N-Select Layer

2. Draw a rectangle extending over the active area by 0.6μ (2λ) in all directions.

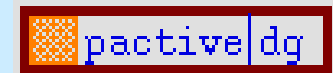
This is it ! Our first transistor is finished, now let us make a few million more of the same :-)



Drawing the P-Diffusion (Active)

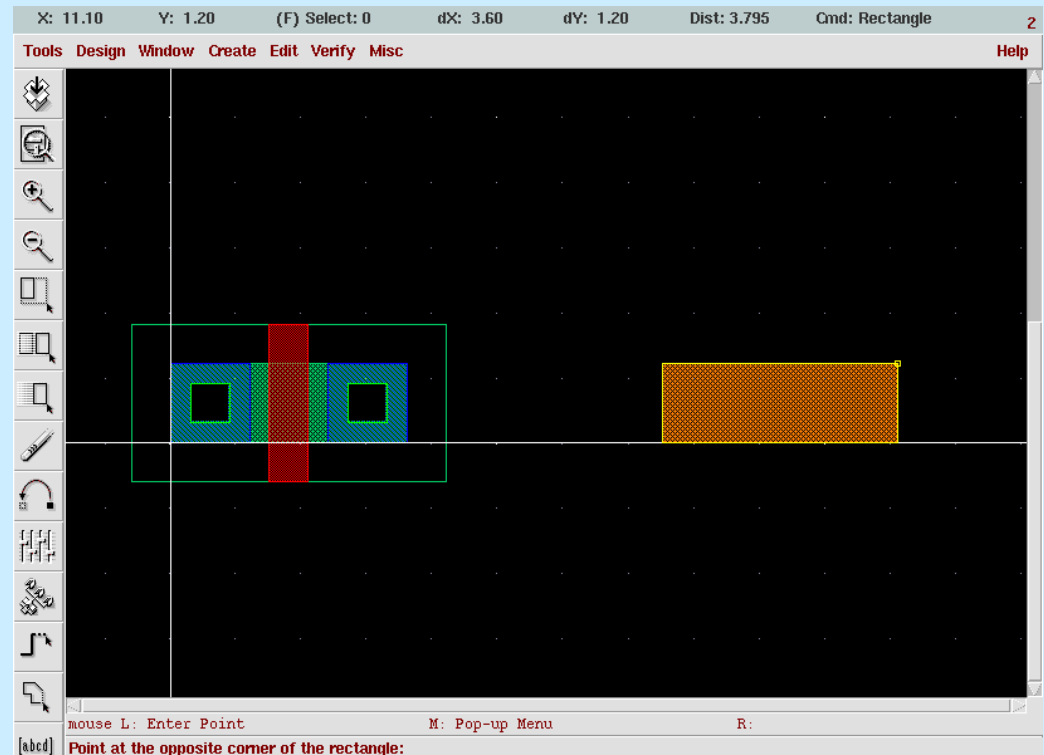
The basic steps involved in drawing the PMOS are the same.

1. Select *pactive* layer from the LSW



2. Draw a rectangle ►
3.6 μ by 1.2 μ

Note that the PMOS transistor will also be surrounded by the N-well region.



Transistor Features

These three steps are identical to the ones done for the NMOS.

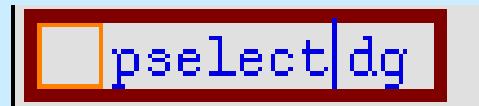
1. Draw the gate poly
2. Place the contacts
3. Cover contacts with Metal-1



The P-Select Layer

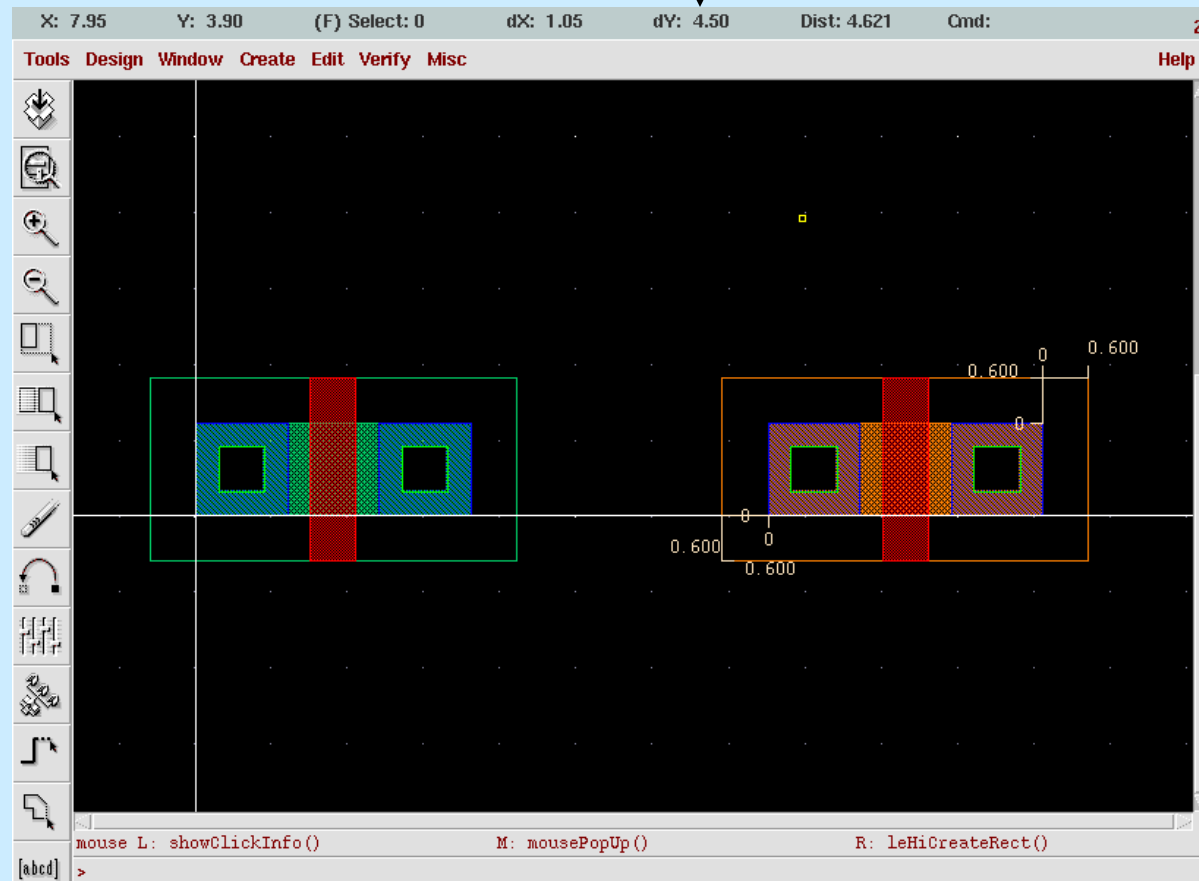
The p-type doping (implantation) window over the active area must be defined using the n-pelect layer.

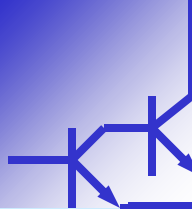
1. Select *pselect* layer from the LSW



The P-Select Layer

2. Draw a rectangle that extends over the active area by 0.6μ (2λ) in all directions.

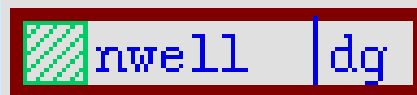




Drawing the N-Well

Note that the drawing sequence of different layers in a mask layout is completely arbitrary, it does not have to follow the actual fabrication sequence.

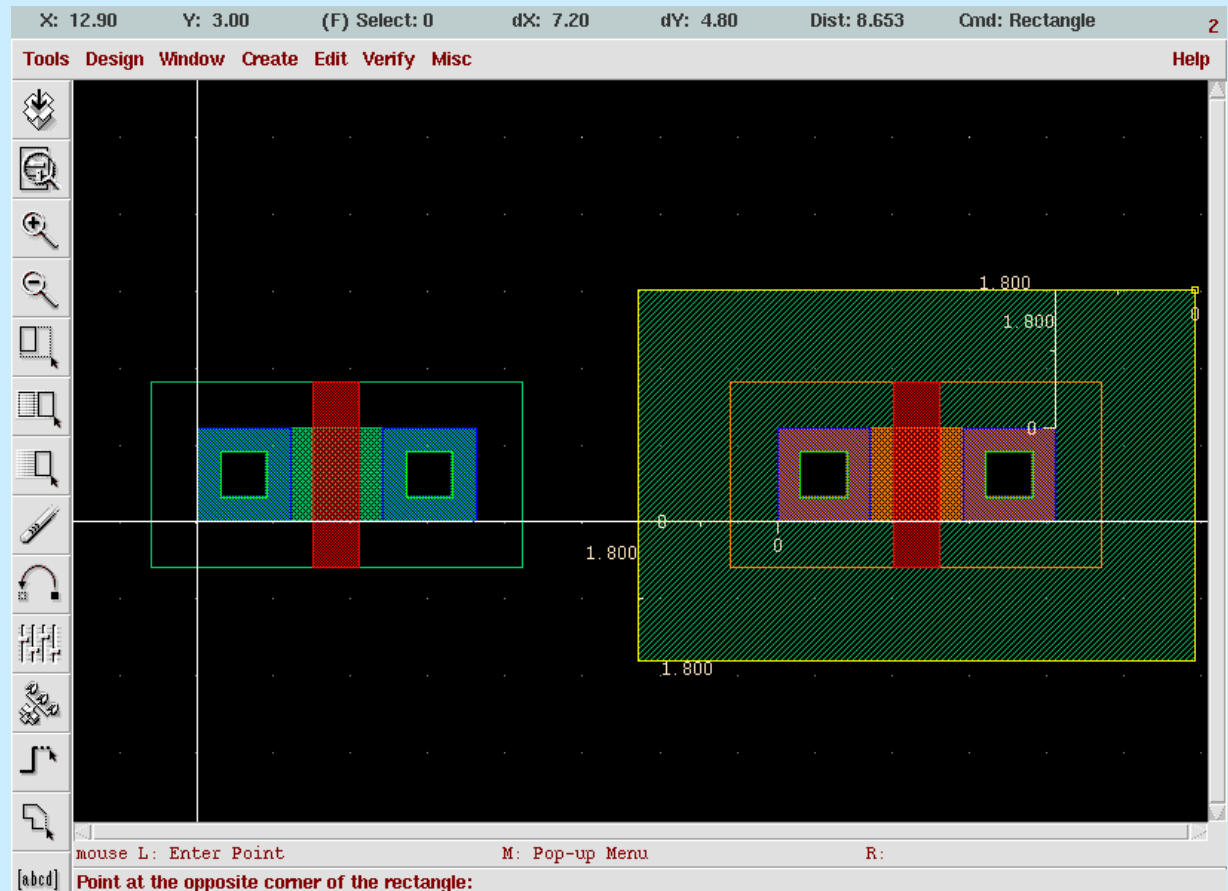
1. Select the *nwell* layer from the LSW

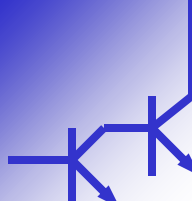


Drawing the N-Well

2. Draw a large n-well rectangle extending over the P-Diffusion

The n-well must extend over the PMOS active area by a large margin, at least 1.8μ



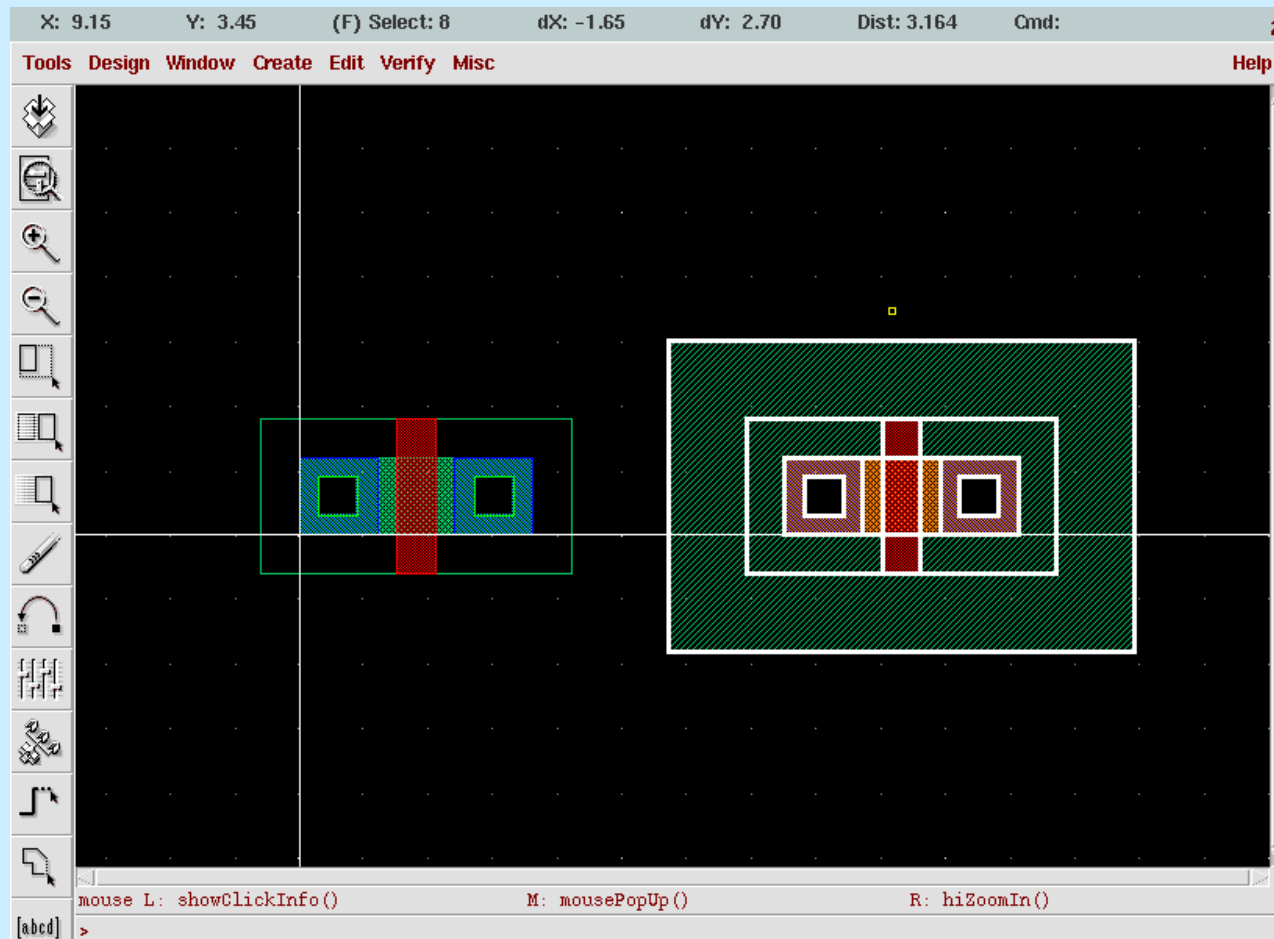


Placing the PMOS and NMOS transistors

Based on our original signal flow diagram, it is more desirable to place the PMOS transistor directly on top of the NMOS transistor- for a more compact layout.

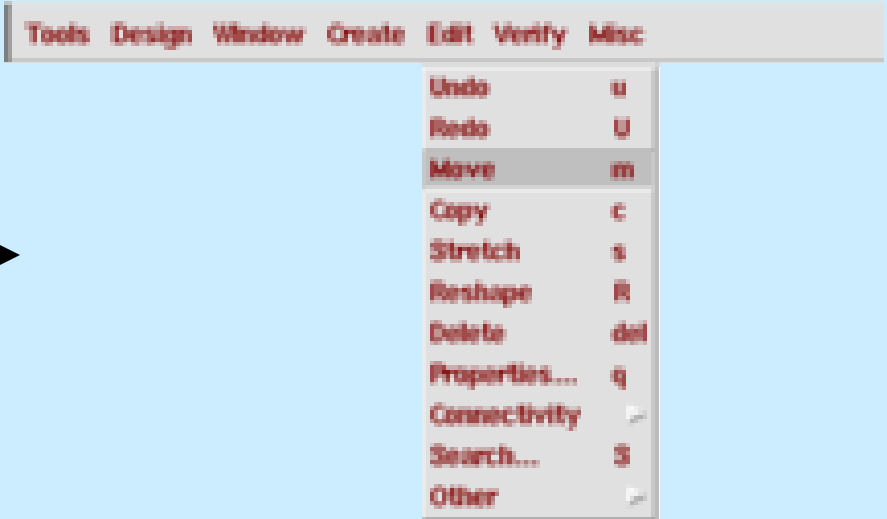
Placing the PMOS and NMOS transistors

1. Select the PMOS transistor



Placing the PMOS and NMOS transistors

2. From the menu *Edit* select the option *Move*



A window will pop-up:

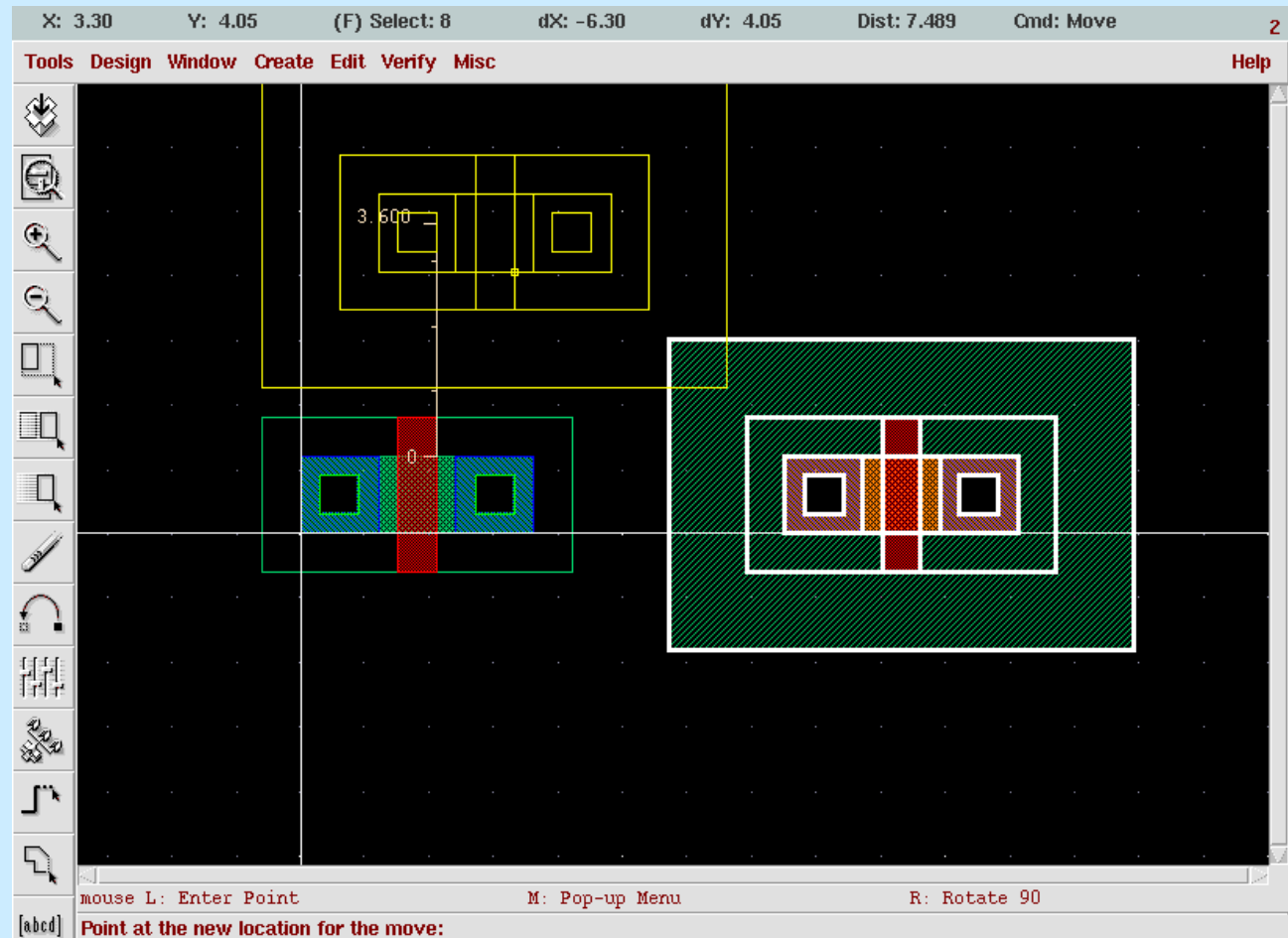


We have to change the *Snap Mode* option to *Anyangle* so that we can move the transistor freely.

Placing the PMOS and NMOS transistors

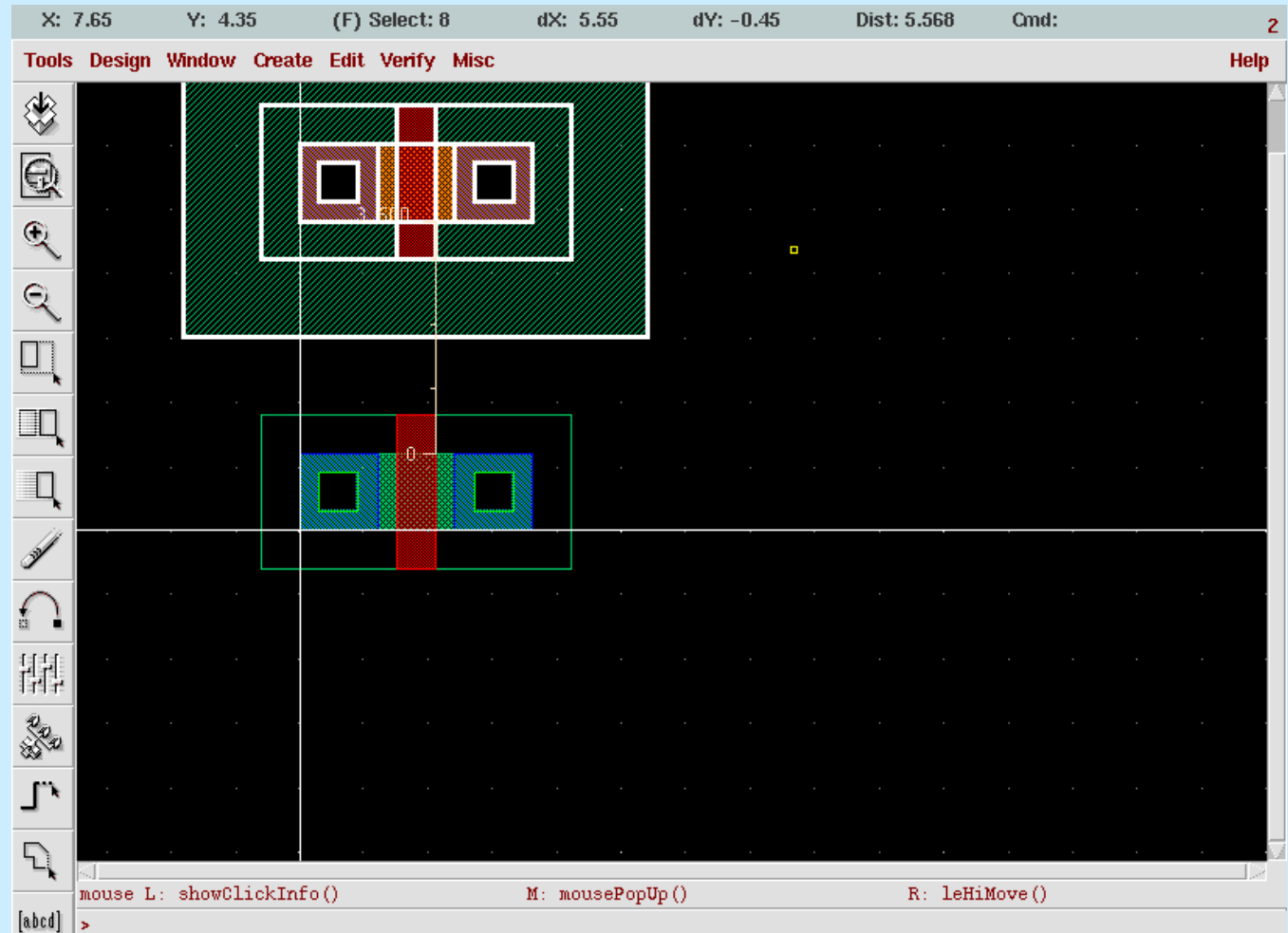
3. The reference point Pick

After we have picked the reference point, the outline of the shape will appear attached to the cursor and we will be able to move the shape around.



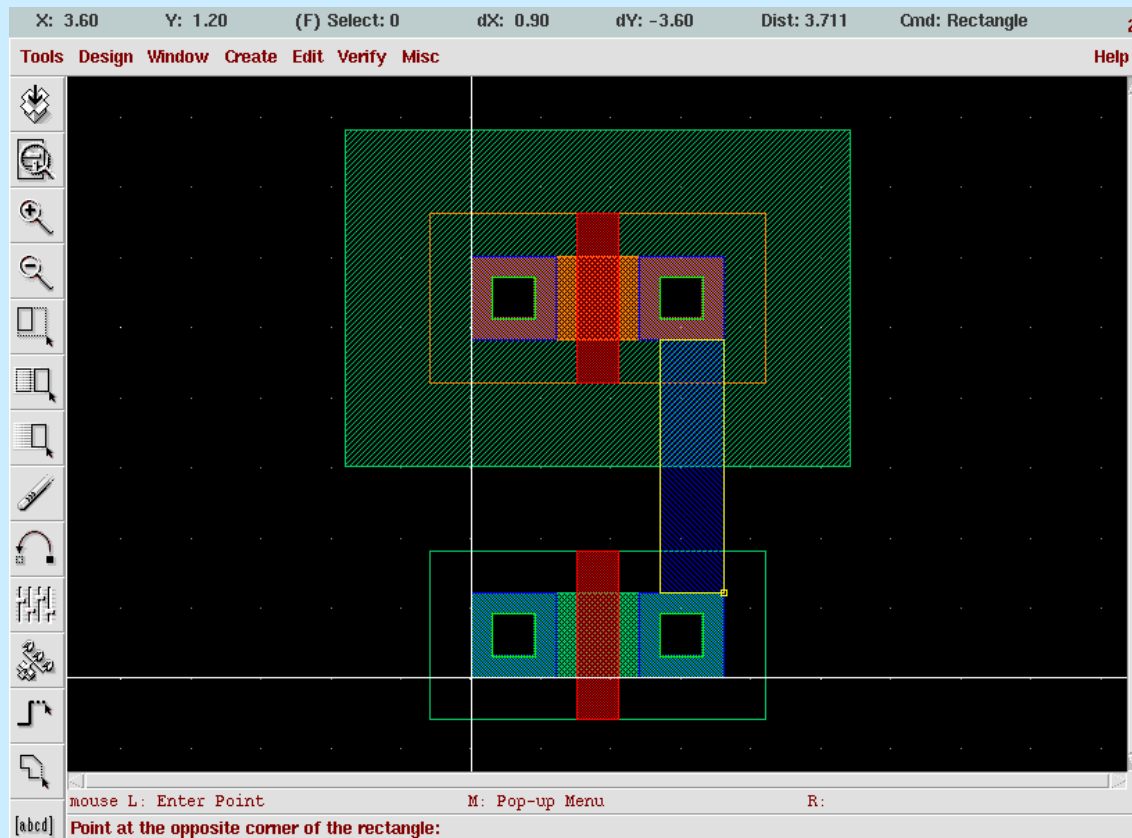
Placing the PMOS and NMOS transistors

4. Place the transistor



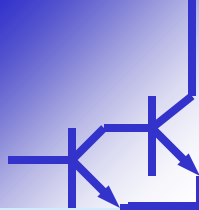
Connecting the Output

1. Draw a Metal-1 rectangle between NMOS and PMOS drain region contacts



- The minimum Metal-1 width is 0.9μ (3λ), thus narrower than the Metal-1 covering the contacts.

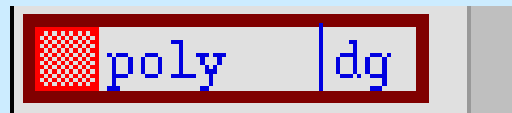
- The transistors are completely symmetric, the source and drain regions are interchangeable.



Connecting the Input

Connect the gates of both transistors to form the input.

1. Select *poly* layer from the LSW



Connecting the Input

2. From the *Create* menu select *Path*



Tools Design Window Create Edit Verify Misc

Rectangle	r
Polygon	P
Path	p
Label...	l
Instance...	i
Pin...	^p
Contact...	o
Device...	
Conics	

The path options box will pop up:

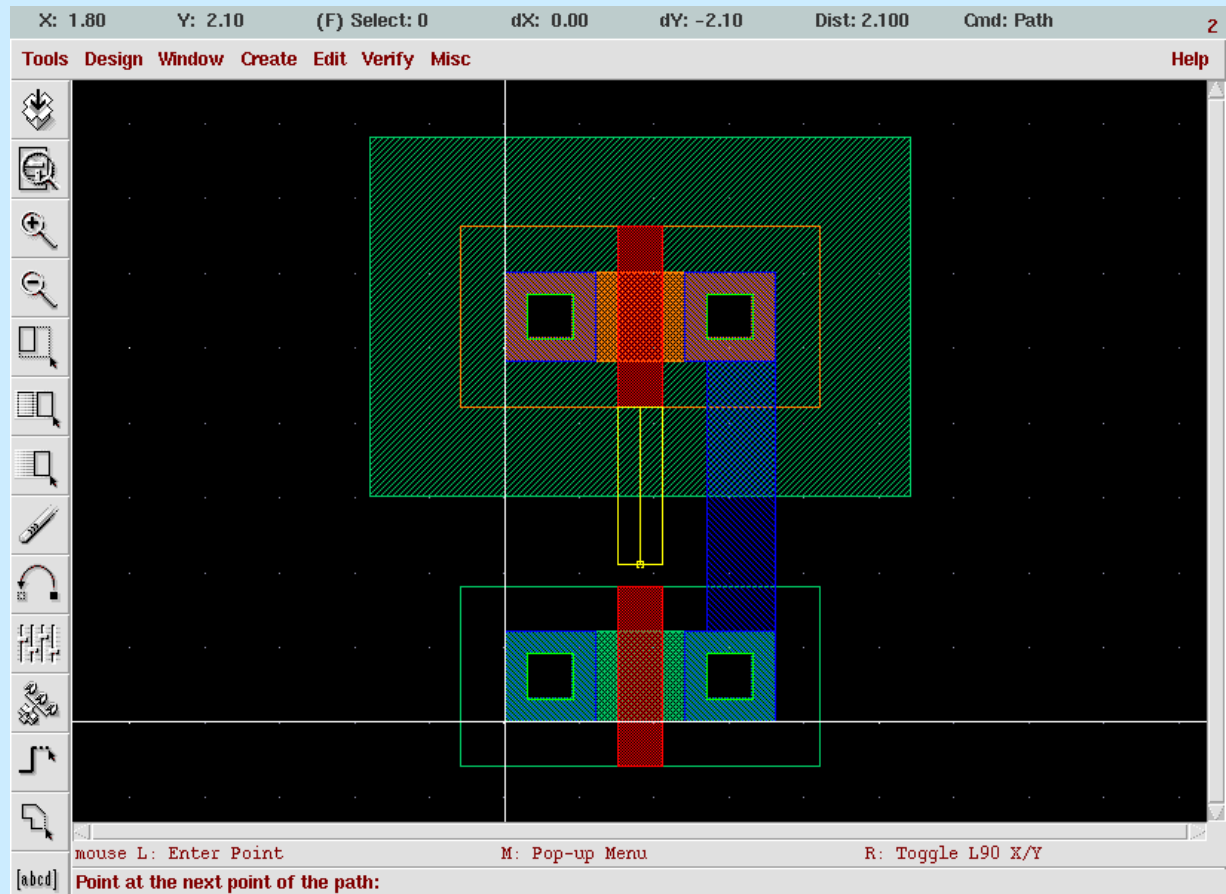
Hide	Cancel	Defaults	Help
Mode		☐ Guided ☒ Manual	Change To Layer
Width	0.6	poly	dg
Fixed Width	☐		
Offset	0	Contact Justification	
Justification	center	☐ ☐ ☐	
End Type	flush	☐ ☒ ☐	
Begin Extension	0	☐ ☐ ☐	
End Extension	0	Snap Mode orthogonal	

In the *path* mode you can draw lines with the selected layer. The width of the drawn line can be adjusted, the default is the minimum width of the selected layer.

Connecting the Input

3. Start path

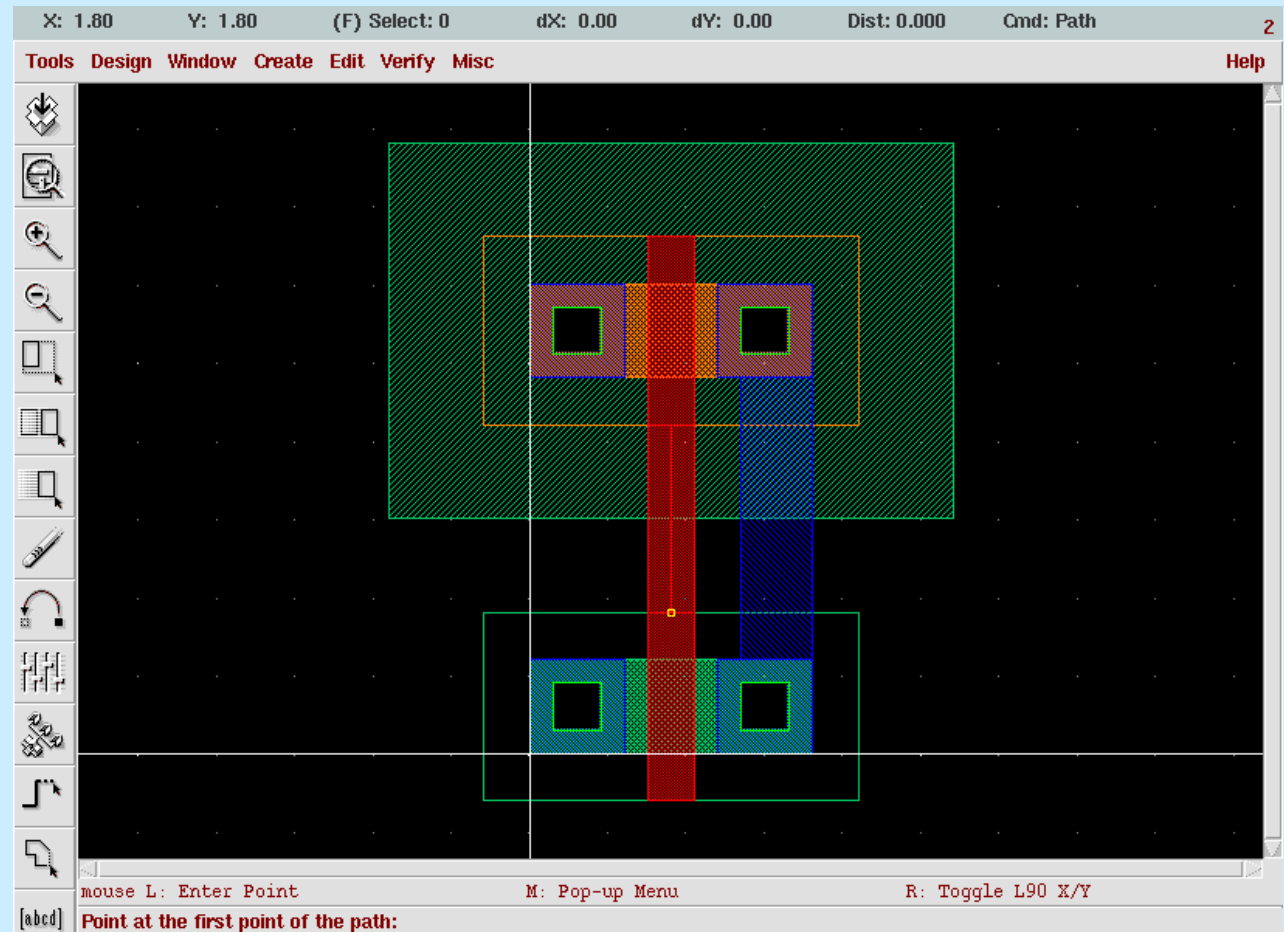
- Click on the middle of the PMOS poly extension a ghost line appear
- Move this ghost line to the NMOS poly extension.

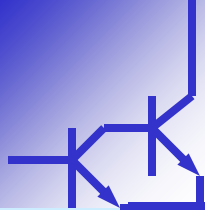


Connecting the Input

4. Double click to finish path

A single click will finish a line segment and let you continue drawing, a double click will finish the path.





Making a Metal-1 Connection for the Input

Now we have to make a connection from the poly layer to the Metal-1 layer.

This connection can be done:

- manually by drawing a poly contact layer between Metal-1 and poly,
- using the *path* command to automatically add the contacts.

Making a Metal-1 Connection for the Input

1. Starting from the poly line connecting the gates, start drawing a horizontal poly path

2. On the *Path Options* dialog box, click on *Change To Layer* and switch to *Metal1*

Hide Cancel Defaults Help

Mode ☐ Guided ☒ Manual

Width Change To Layer  metall dg

Fixed Width ☐

Offset

Justification center

End Type flush

Begin Extension

End Extension

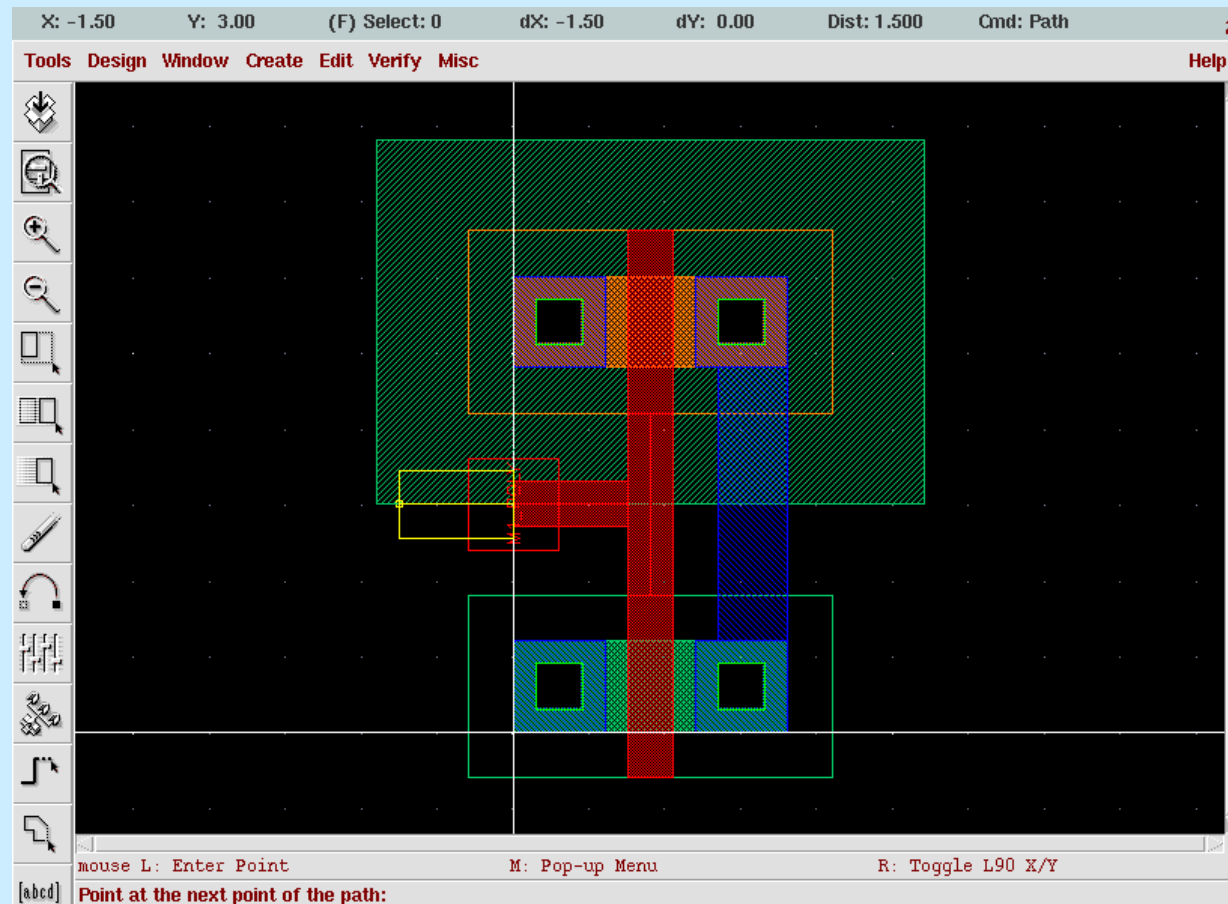
Snap Mode orthogonal

Contact Justification

☐	☐	☐
☐	☒	☐
☐	☐	☐

Making a Metal-1 Connection for the Input

This will automatically add a contact to the end of the current path.

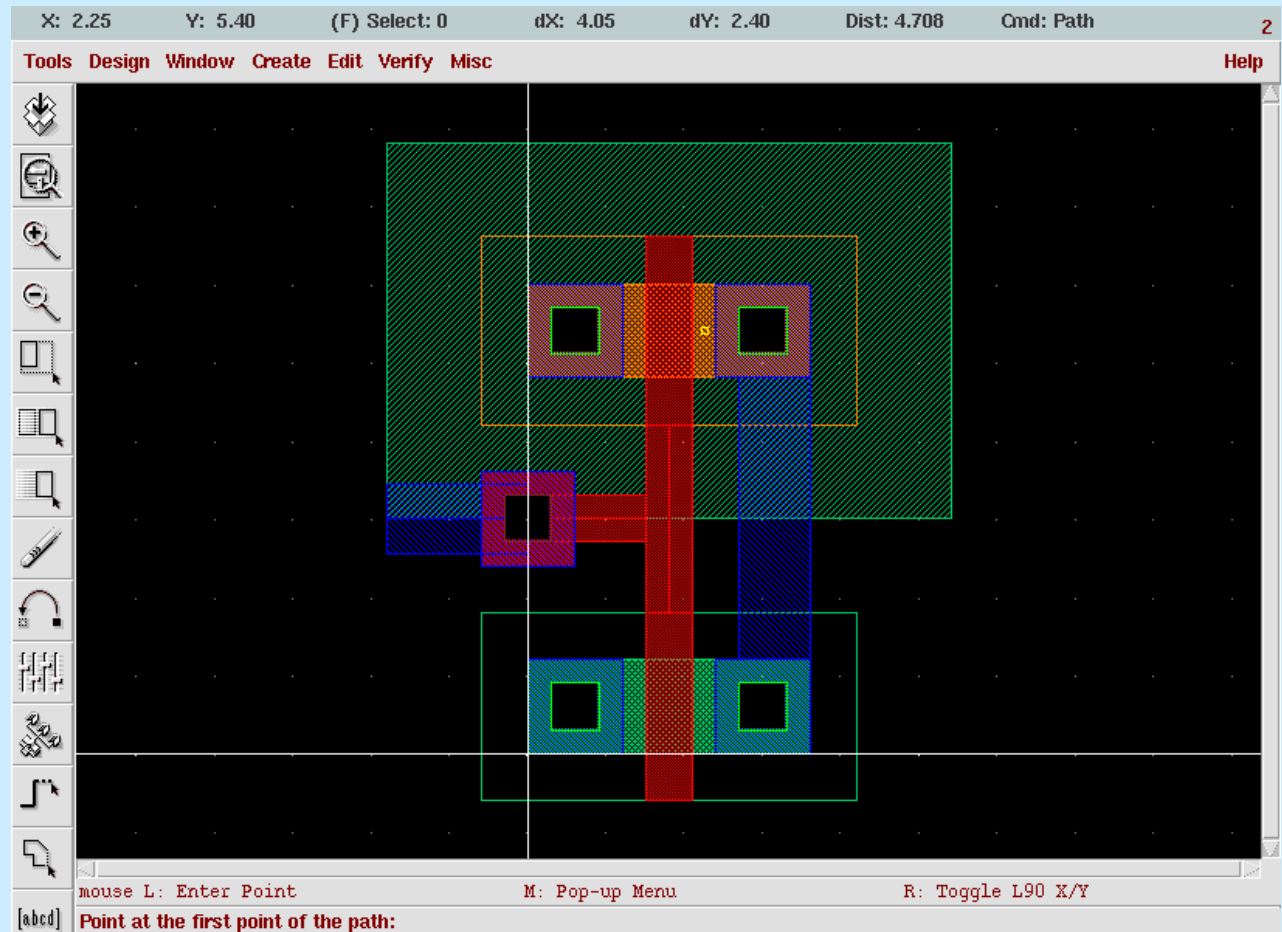


Making a Metal-1 Connection for the Input

3. Finish the path (by double clicking)

SHIFT-F to see all levels of hierarchy.

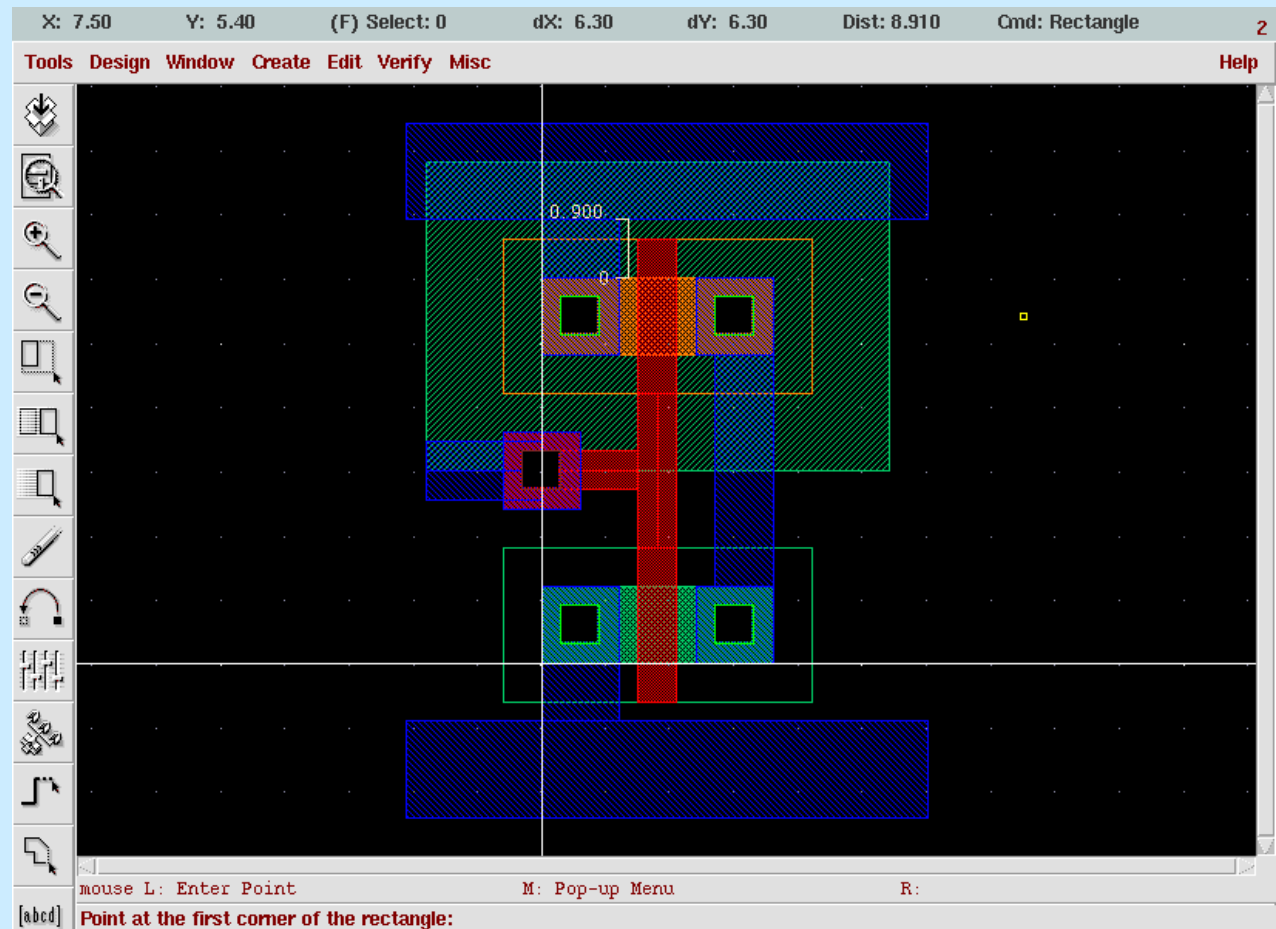
CTRL-F to see a single layer of hierarchy.



Power Rails

Our Signal Flow Graph suggests horizontal power and ground lines in Metal-1.

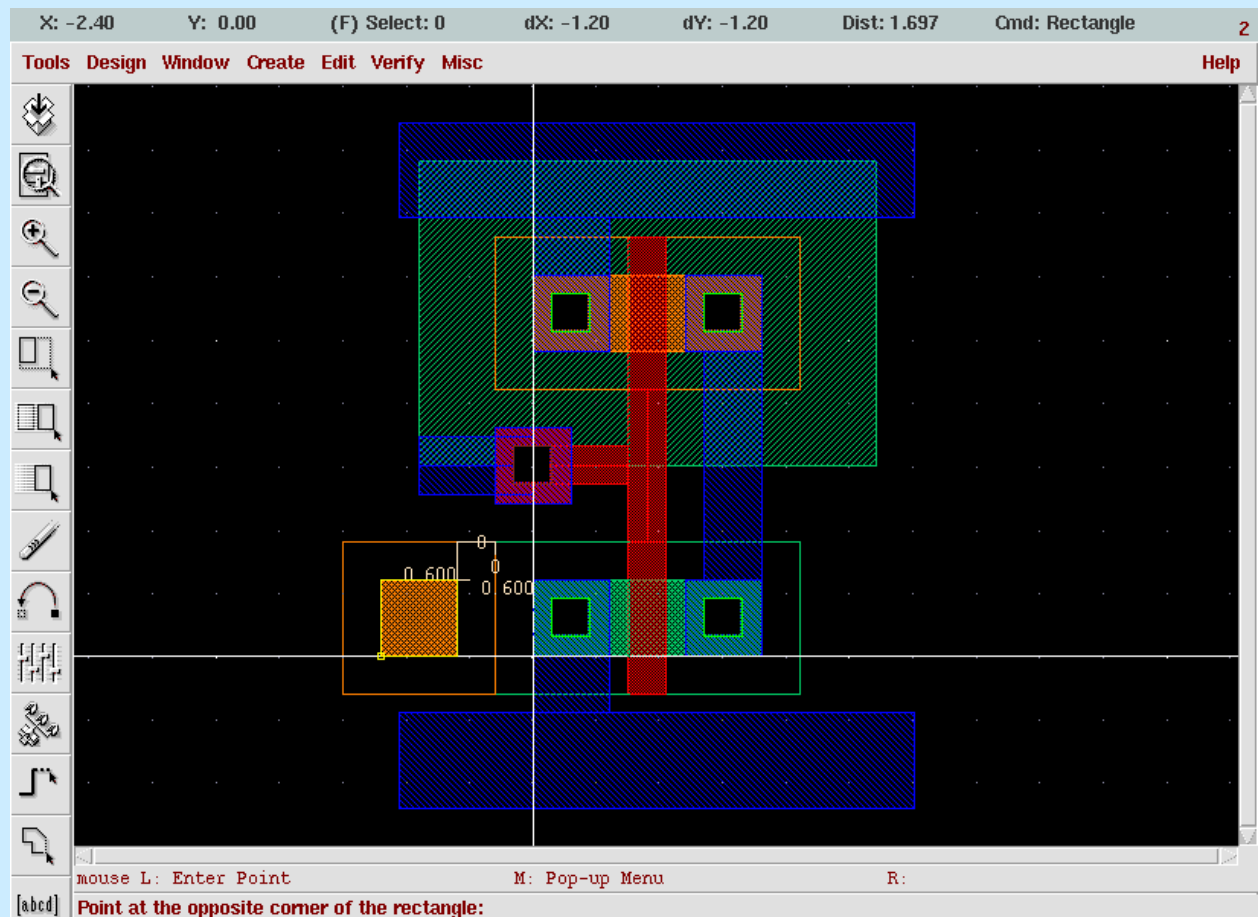
1. Draw the Power Rail in Metal-1 above the PMOS
2. Draw the Ground Rail in Metal-1 below the NMOS



P-Substrate Contact

The substrate on which the transistors are built must be properly biased.

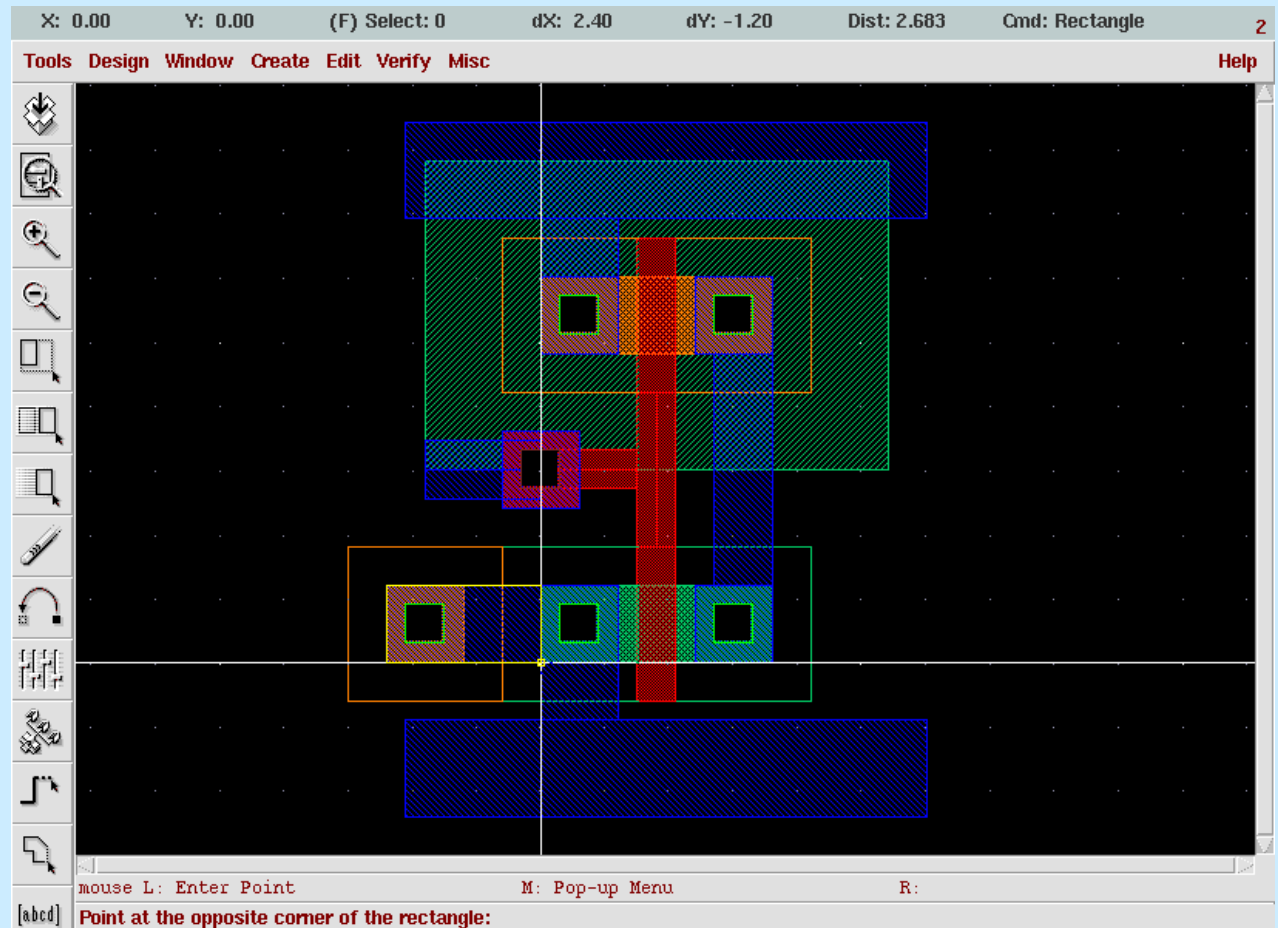
1. Draw a P-select square next to the NMOS transistor.
2. Draw a P-active square inside the P-select area.



P-Substrate Contact

3. Draw the active contact square inside the p-type active area.

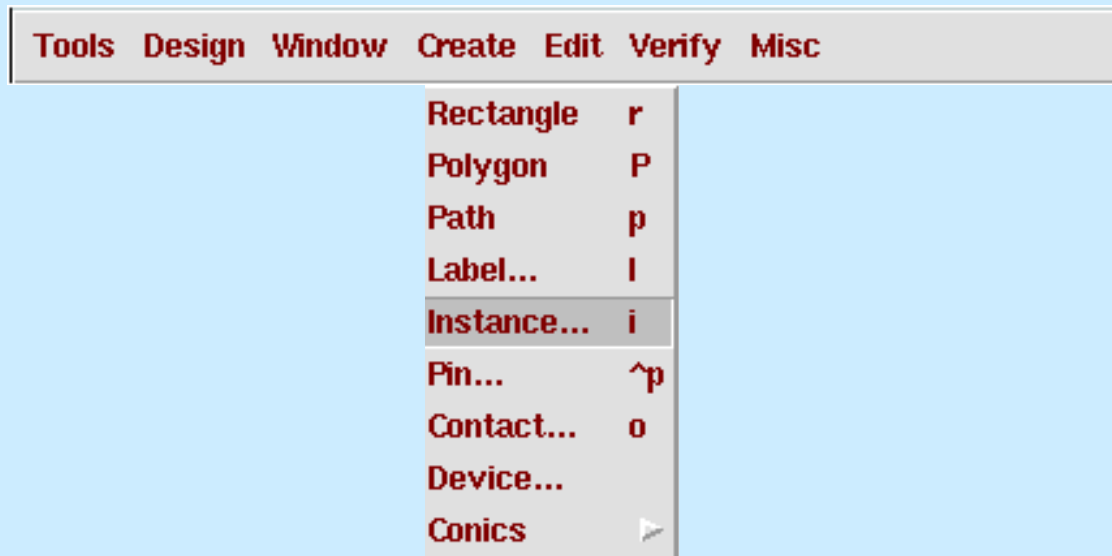
4. Make a metal connection to ground, covering the entire substrate contact.



N-Substrate Contact

The PMOS transistor was placed within the n-well, which has to be biased with the VDD potential.

1. From the menu *Create* select option *Instance*



N-Substrate Contact

The instance options menu will pop-up:

Provide:

- a cell name
- library

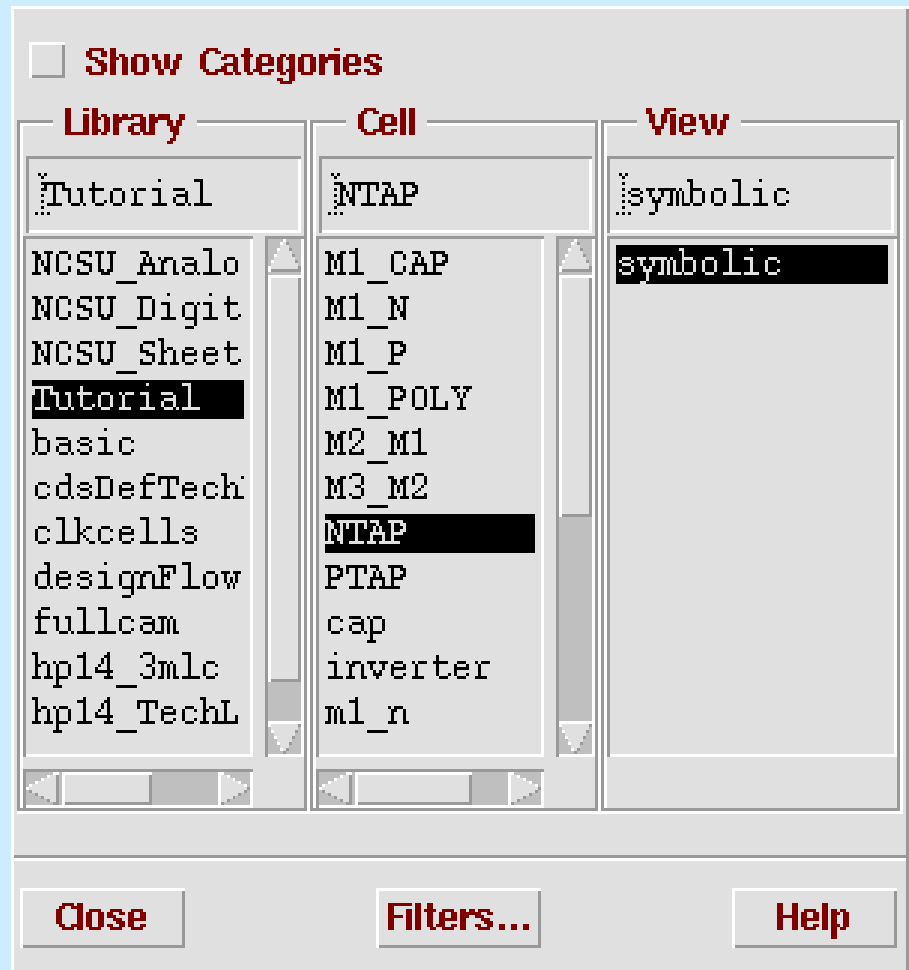
The screenshot shows a dialog box titled "N-Substrate Contact" with a light gray background. At the top, there are four buttons: "Hide", "Cancel", "Defaults", and "Help". The main area contains several input fields and buttons. The "Library" field is set to "Tutorial". The "Cell" field is set to "NTAP", with a "Browse" button to its right. The "View" field is set to "symbolic". The "Names" field is set to "I3". Below these, there are two rows of input fields: "Rows" and "Columns" are both set to "1", and "Delta X" and "Delta Y" are both set to "2.4". To the right of these is a "Mag" field set to "1". Below these fields are three buttons: "Rotate", "Sideways", and "Upsidedown". At the bottom, there are five more input fields: "yPitch" (set to "1.2"), "xPitch" (set to "1.2"), "column" (set to "1"), "row" (set to "1"), and "I" (set to "0.6").

Library	Tutorial		
Cell	NTAP	Browse	
View	symbolic		
Names	I3		
Rows	1	Columns	1
Delta X	2.4	Delta Y	2.4
		Mag	1
Rotate Sideways Upsidedown			
yPitch	1.2		
xPitch	1.2		
column	1		
row	1		
I	0.6		

N-Substrate Contact

Choose the library, cell
and cell view.

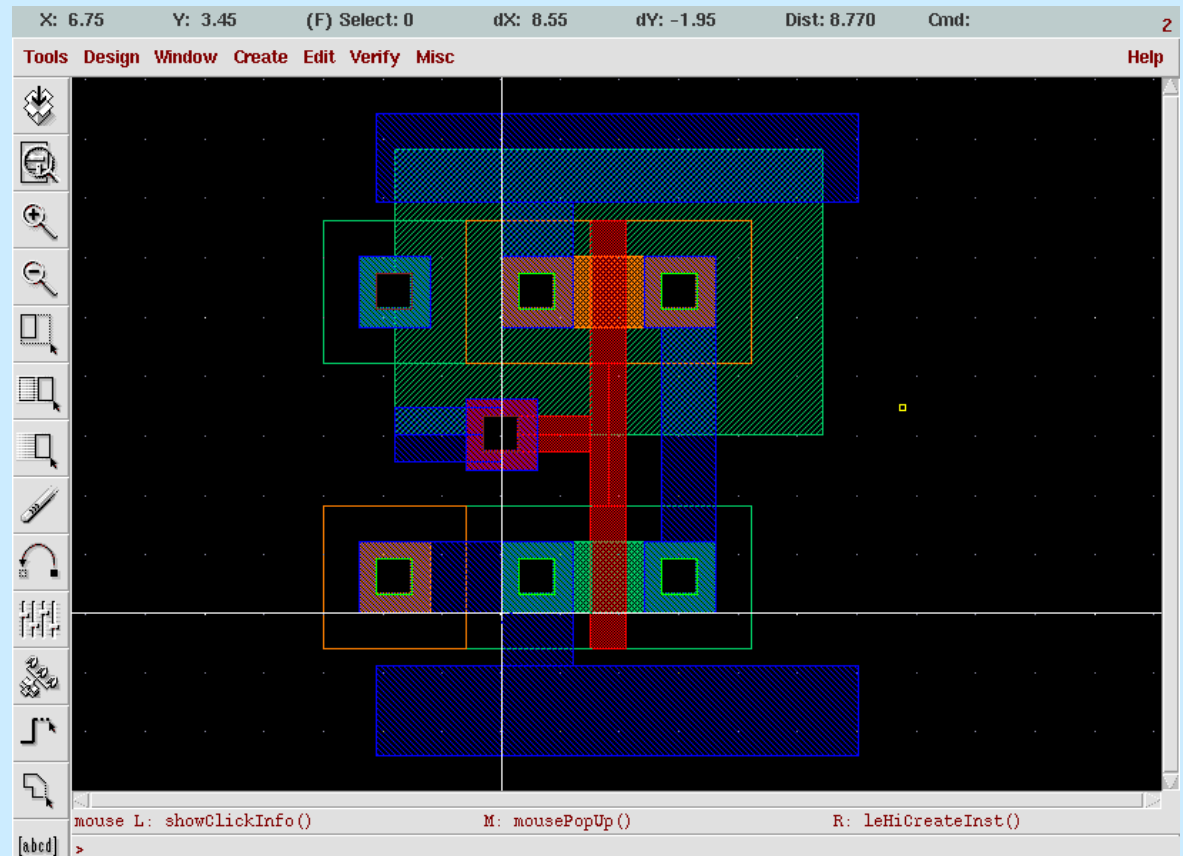
Your selection will be
transferred to the
Instance options menu.



N-Substrate Contact

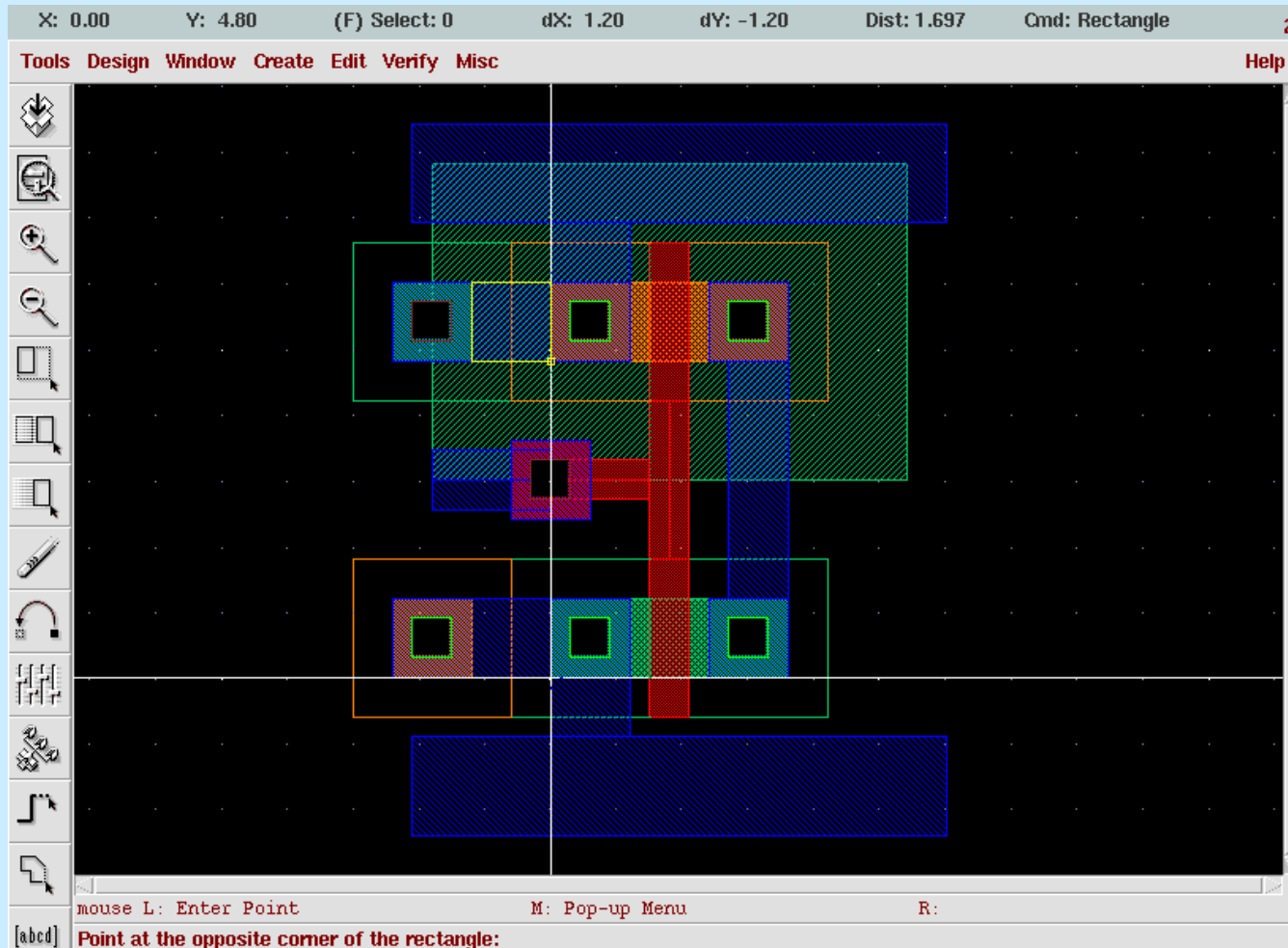
2. Move the instance to the desired location.
3. Place the instance.

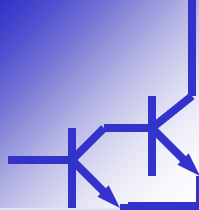
The n-well in this example is not wide enough to accommodate both the PMOS transistor and the contact, which will obviously generate a rule violation. This will have to be dealt with in the next step.



N-Substrate Contact

4. Make the power connection.





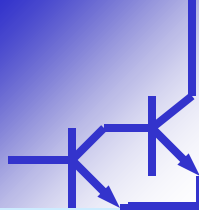
Enclosing the substrate contact

Enlarge the n-well, so that it also covers the substrate contact.

- draw an adjoining rectangle using the n-well layer or
- modify the existing rectangle

1. Press *F4* on the keyboard to toggle selection mode.

The information bar will start displaying "(P) Select" (P for partial) instead of "(F) Select" (F for Full).



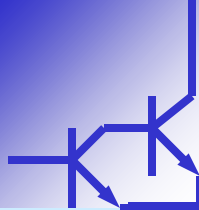
Enclosing the substrate contact

2. Move cursor over the left edge of the n-well.

3. Click once to select the edge.

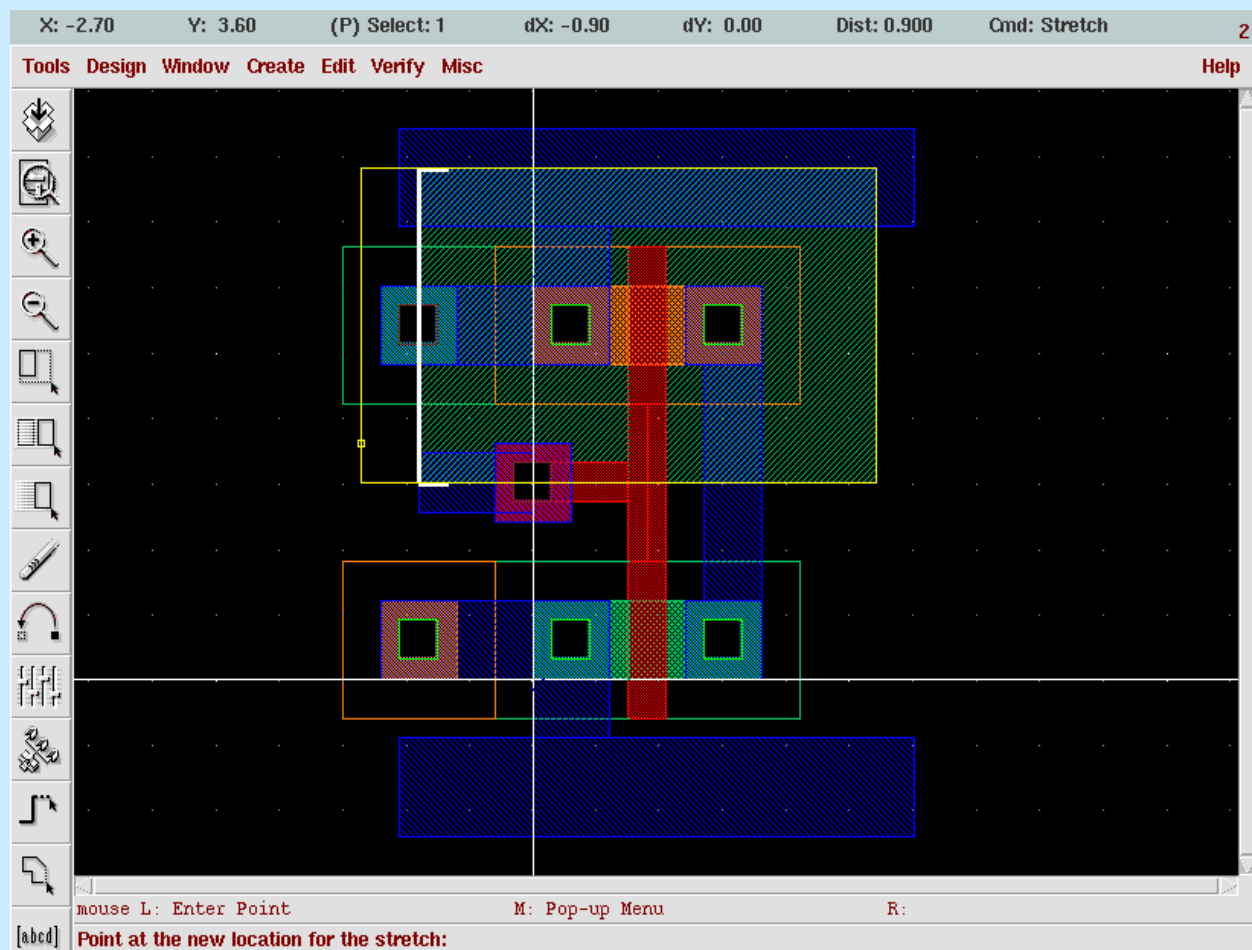
4. Move mouse over the selected edge (without pressing any mouse buttons).

Cursor changes shape when you are close to the edge.

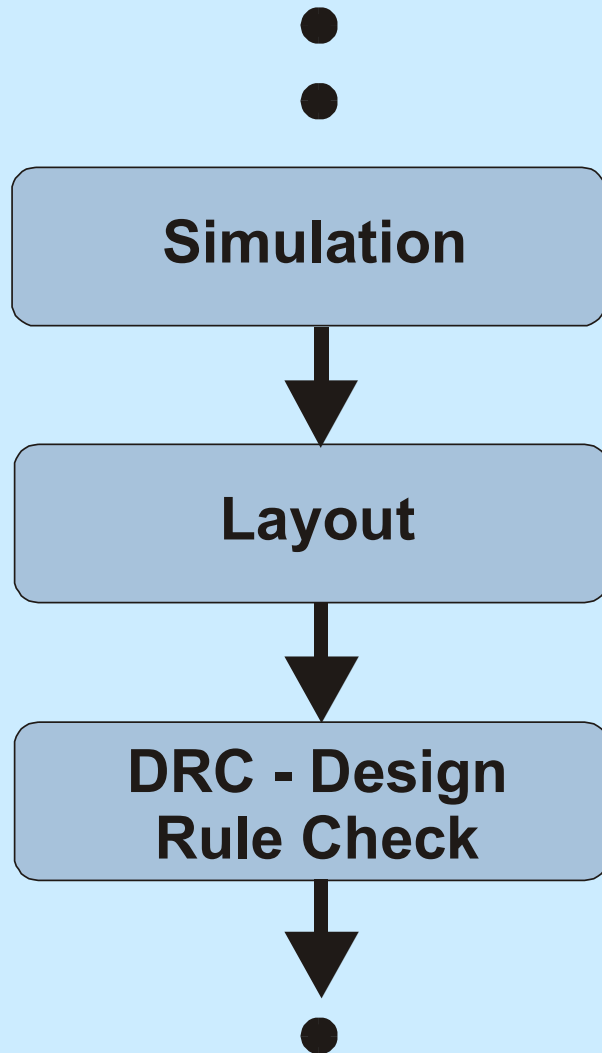


Enclosing the substrate contact

5. Press and hold left mouse button when cursor changes above the selected edge.



Design Rule Check (DRC)



- The created mask layout must conform to a complex set of design rules, in order to ensure a lower probability of fabrication defects.
- A tool built into the Layout Editor, called Design Rule Checker, is used to detect any design rule violations during and after the mask layout design.

Design Rule Checking

1. From the menu *Verify* select option *DRC*

This will pop-up the
DRC options dialog ►
box:

OK Cancel Defaults Apply Help

Checking Method ☒ flat ☐ hierarchical ☐ hier w/o optimization

Checking Limit ☒ full ☐ incremental ☐ by area

Coordinate Sel by Cursor

Switch Names Set Switches

Run-Specific Command File ☐

Inclusion Limit

Join Nets With Same Name ☐

Echo Commands ☒

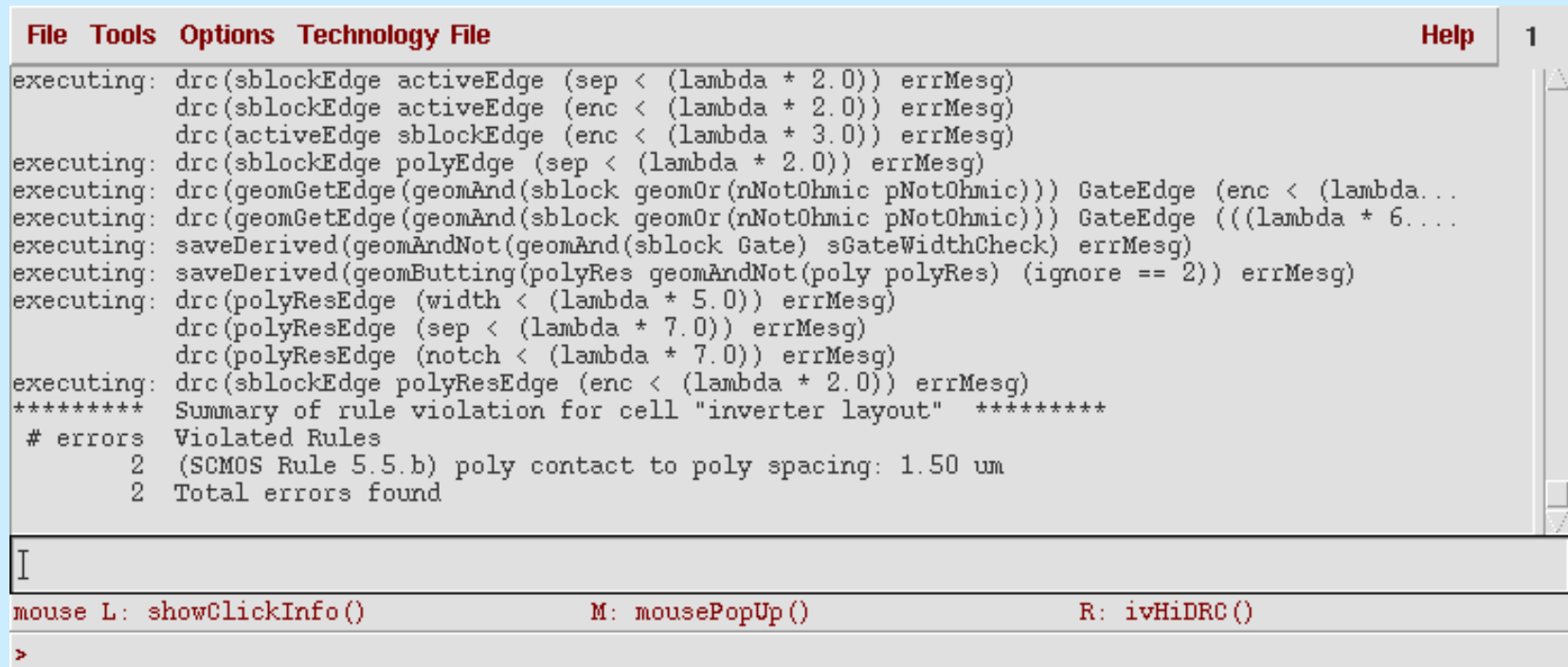
Rules File

Rules Library ☒

Machine ☒ local ☐ remote Machine

Design Rule Checking

2. Start DRC



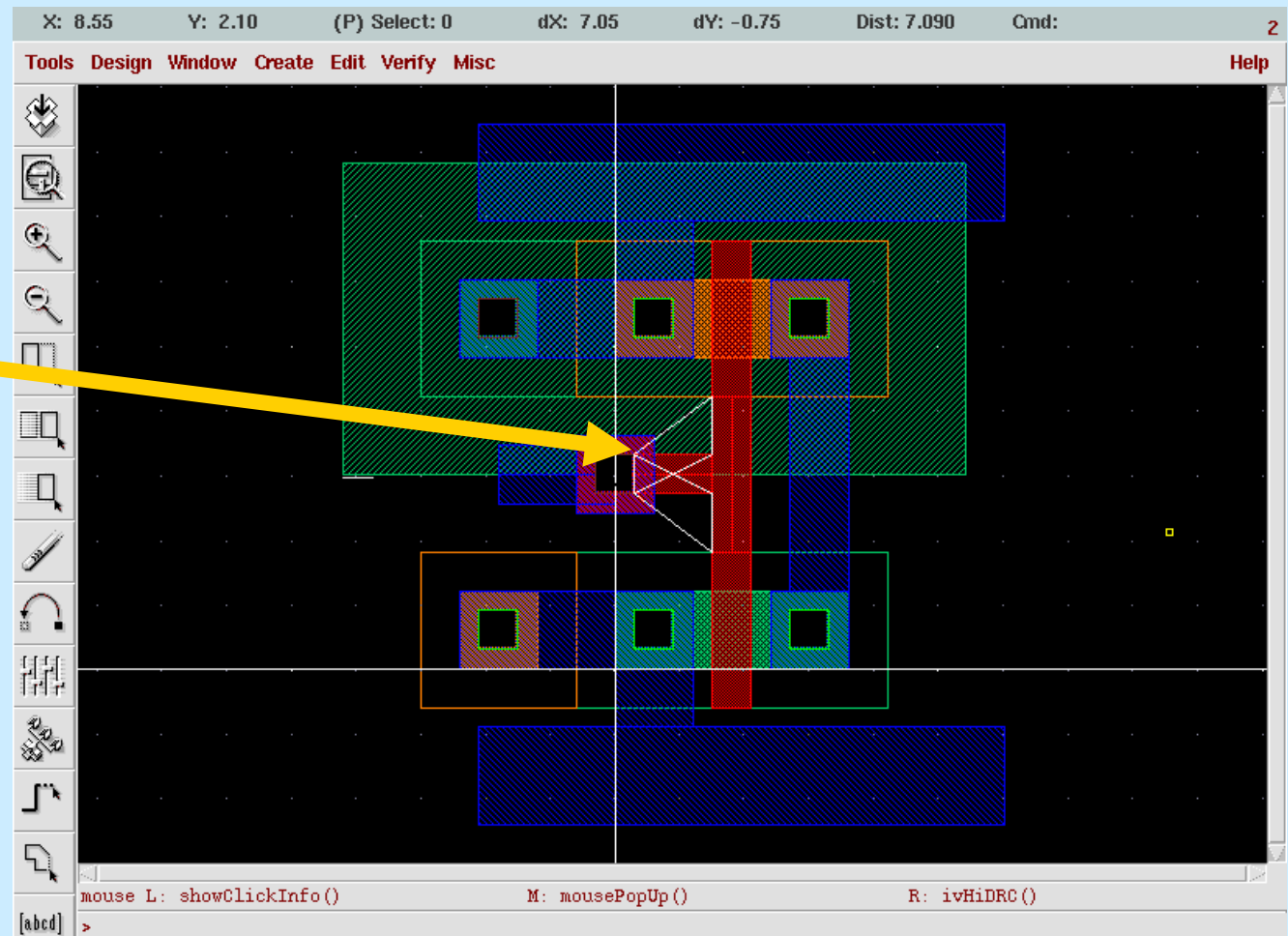
```
File Tools Options Technology File Help 1
executing: drc(sblockEdge activeEdge (sep < (lambda * 2.0)) errMesg)
           drc(sblockEdge activeEdge (enc < (lambda * 2.0)) errMesg)
           drc(activeEdge sblockEdge (enc < (lambda * 3.0)) errMesg)
executing: drc(sblockEdge polyEdge (sep < (lambda * 2.0)) errMesg)
executing: drc(geomGetEdge(geomAnd(sblock geomOr(nNotOhmic pNotOhmic))) GateEdge (enc < (lambda...
executing: drc(geomGetEdge(geomAnd(sblock geomOr(nNotOhmic pNotOhmic))) GateEdge (((lambda * 6...
executing: saveDerived(geomAndNot(geomAnd(sblock Gate) sGateWidthCheck) errMesg)
executing: saveDerived(geomButting(polyRes geomAndNot(poly polyRes) (ignore == 2)) errMesg)
executing: drc(polyResEdge (width < (lambda * 5.0)) errMesg)
           drc(polyResEdge (sep < (lambda * 7.0)) errMesg)
           drc(polyResEdge (notch < (lambda * 7.0)) errMesg)
executing: drc(sblockEdge polyResEdge (enc < (lambda * 2.0)) errMesg)
***** Summary of rule violation for cell "inverter layout" *****
# errors  Violated Rules
      2   (SCMOS Rule 5.5.b) poly contact to poly spacing: 1.50 um
      2   Total errors found

I
mouse L: showClickInfo()           M: mousePopUp()           R: ivHiDRC()
>
```

DRC results and progress will be displayed in the CIW.

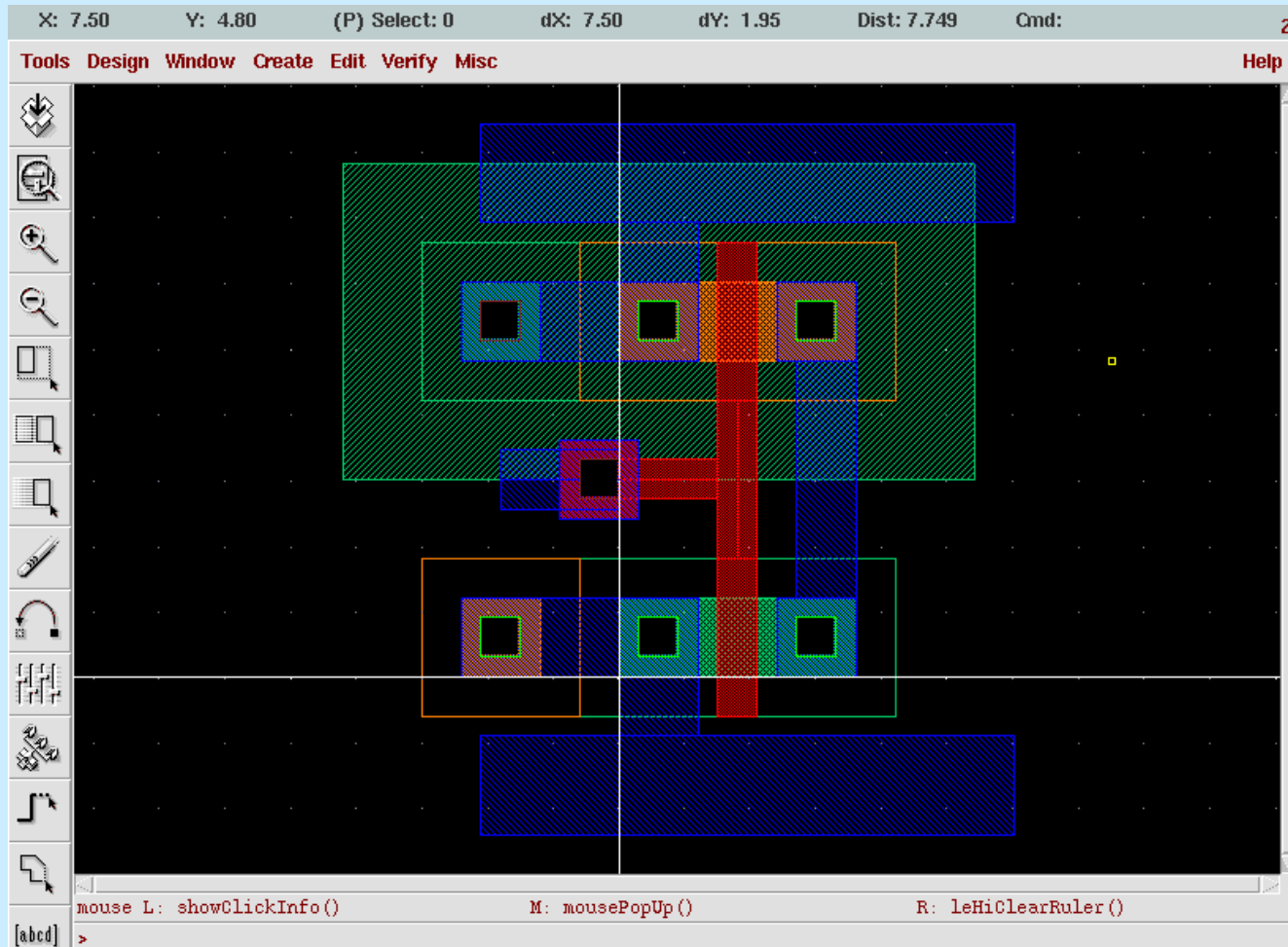
Design Rule Checking

The errors are highlighted on the layout.

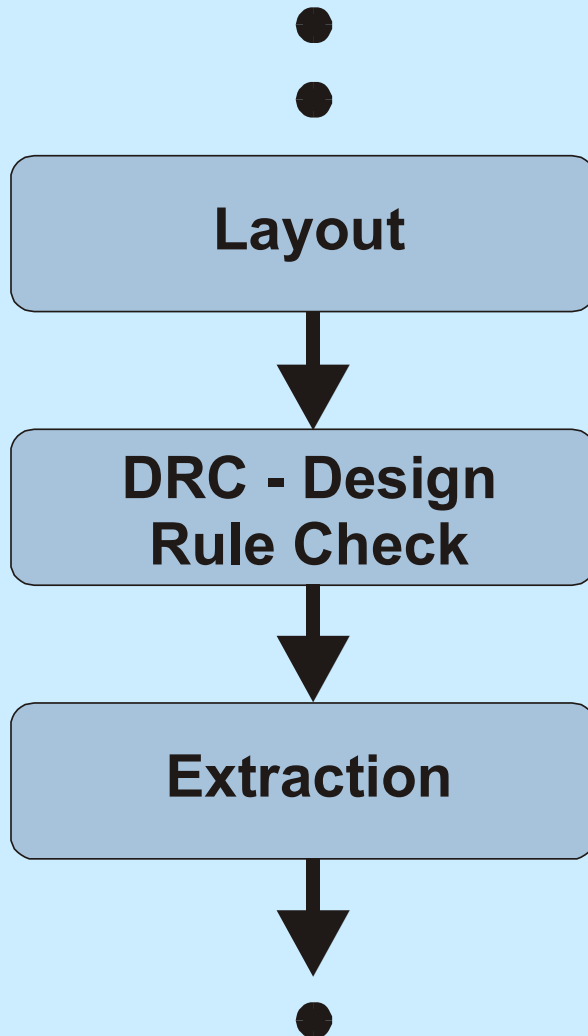


Final Layout

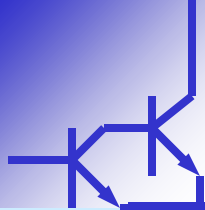
This is the completed layout of the CMOS inverter.



Circuit Extraction



- The mask layout only contains physical data. (In fact it just contains coordinates of rectangles drawn in different layers).
- The extraction process identifies the devices and generates a netlist associated with the layout.



Extracting from the Layout

Before extraction make sure that the design does not contain any DRC errors.

1. From the *Verify* menu select the option *Extract*

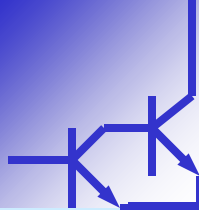


Extracting from the Layout

To enable the extraction of parasitic devices, a selection parameter called a switch has to be specified.

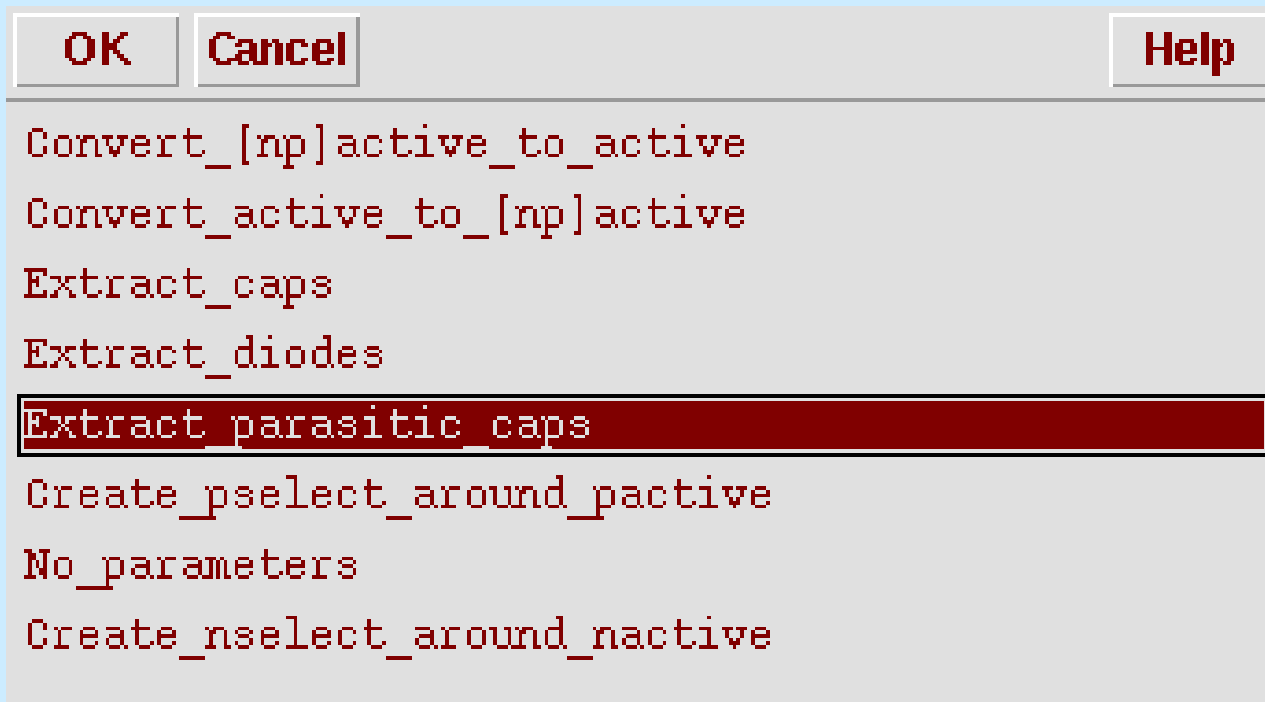
The dialog box contains the following fields and controls:

- Buttons:** OK, Cancel, Defaults, Apply, Help.
- Extract Method:** ☒ flat, ☐ macro cell, ☐ full hier, ☐ incremental hier.
- Join Nets With Same Name:** ☐ **Echo Command:** ☒
- Switch Names:** **Set Switches** (button)
- Run-Specific Command File:** ☐
- Inclusion Limit:**
- View Names:** **Extracted** **Excell**
- Rules File:**
- Rules Library:** ☒
- Machine:** ☒ local, ☐ remote **Machine**



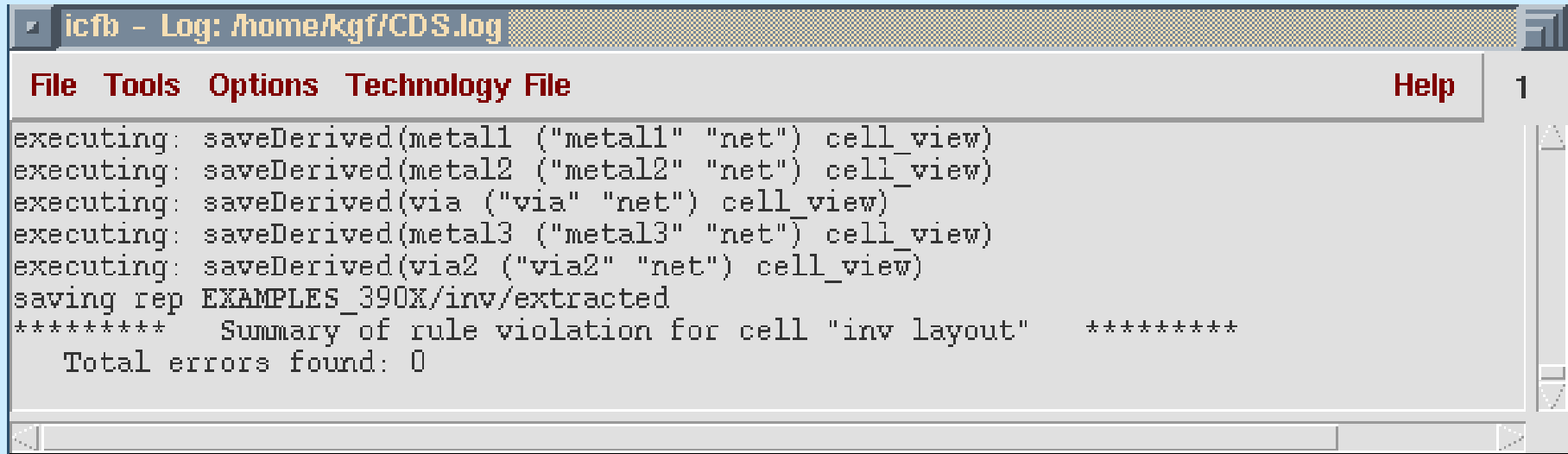
Extracting from the Layout

The list of switches



Extracting from the Layout

Check the Command Interpreter Window (the main window when you start Cadence) for errors after extraction.

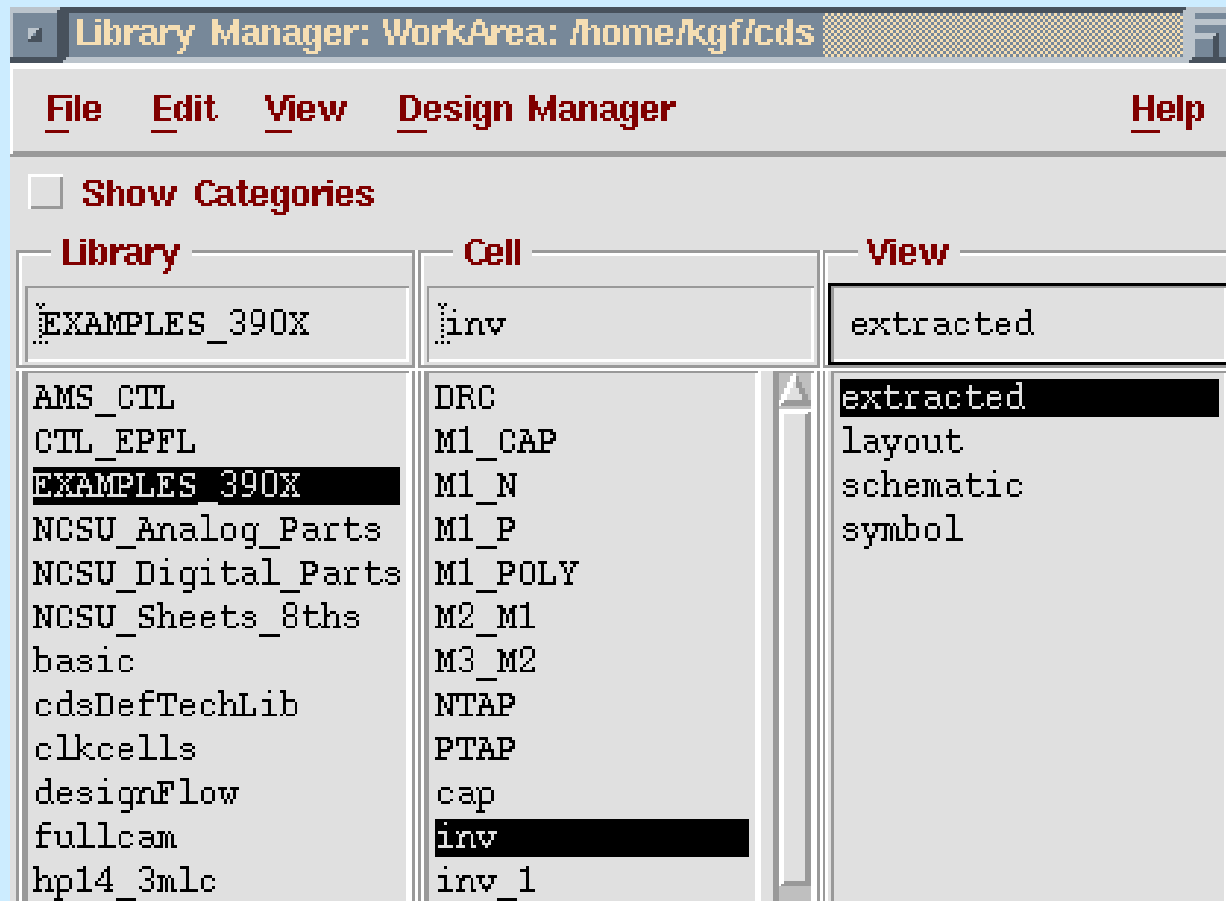
A screenshot of the Cadence Command Interpreter Window. The title bar reads 'icfb - Log: /home/kgf/CDS.log'. The menu bar includes 'File', 'Tools', 'Options', 'Technology', 'File', and 'Help'. The main text area shows the following output:

```
executing: saveDerived(metal1 ("metal1" "net") cell_view)
executing: saveDerived(metal2 ("metal2" "net") cell_view)
executing: saveDerived(via ("via" "net") cell_view)
executing: saveDerived(metal3 ("metal3" "net") cell_view)
executing: saveDerived(via2 ("via2" "net") cell_view)
saving rep EXAMPLES_390X/inv/extracted
***** Summary of rule violation for cell "inv layout" *****
Total errors found: 0
```

Following a successful extraction you will see a new cell view called *extracted* for your cell in the library manager.

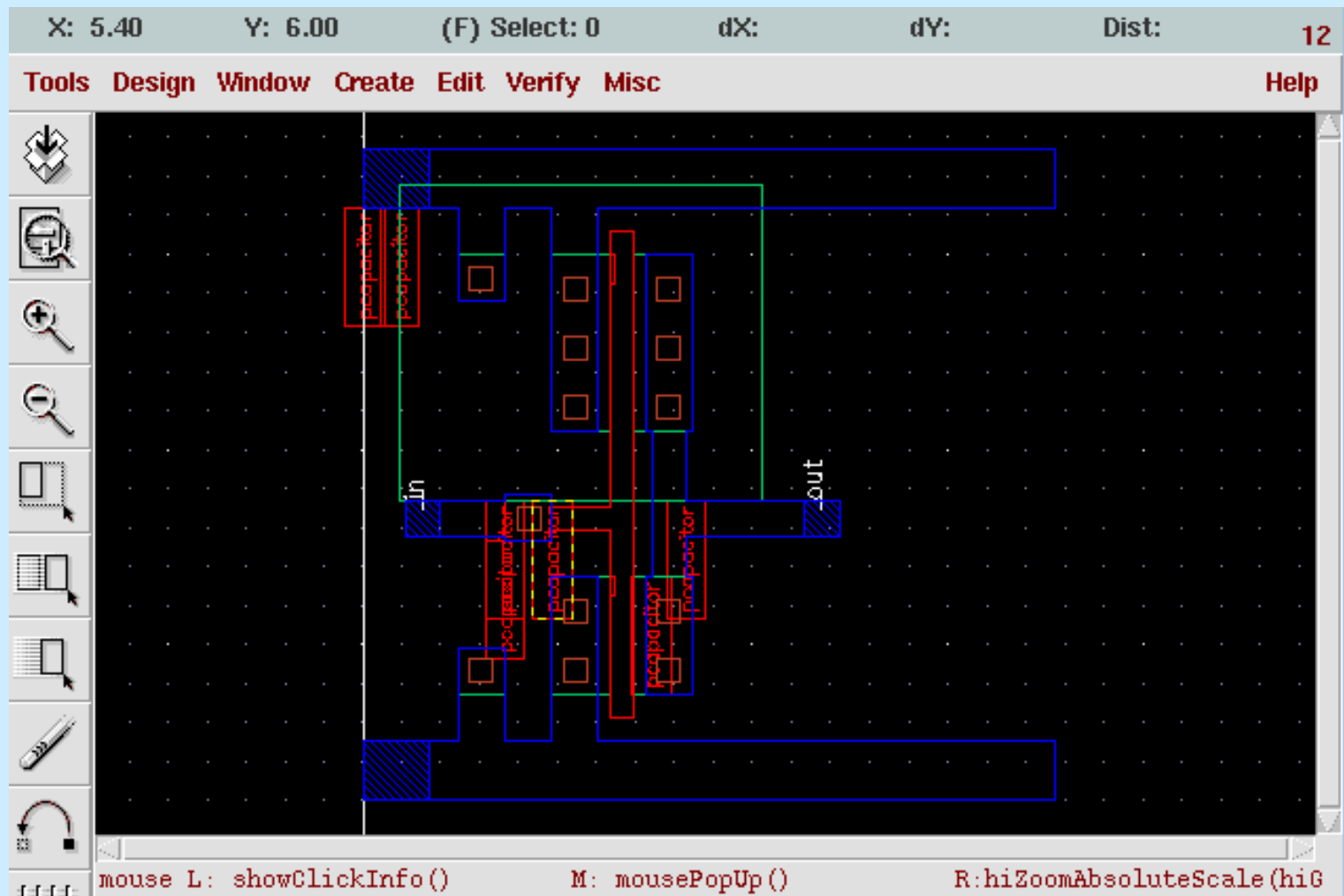
The Extracted Cell View

A new cellview (called *extracted*) is generated in your library.



The Extracted Cell View

Load the
cellview.

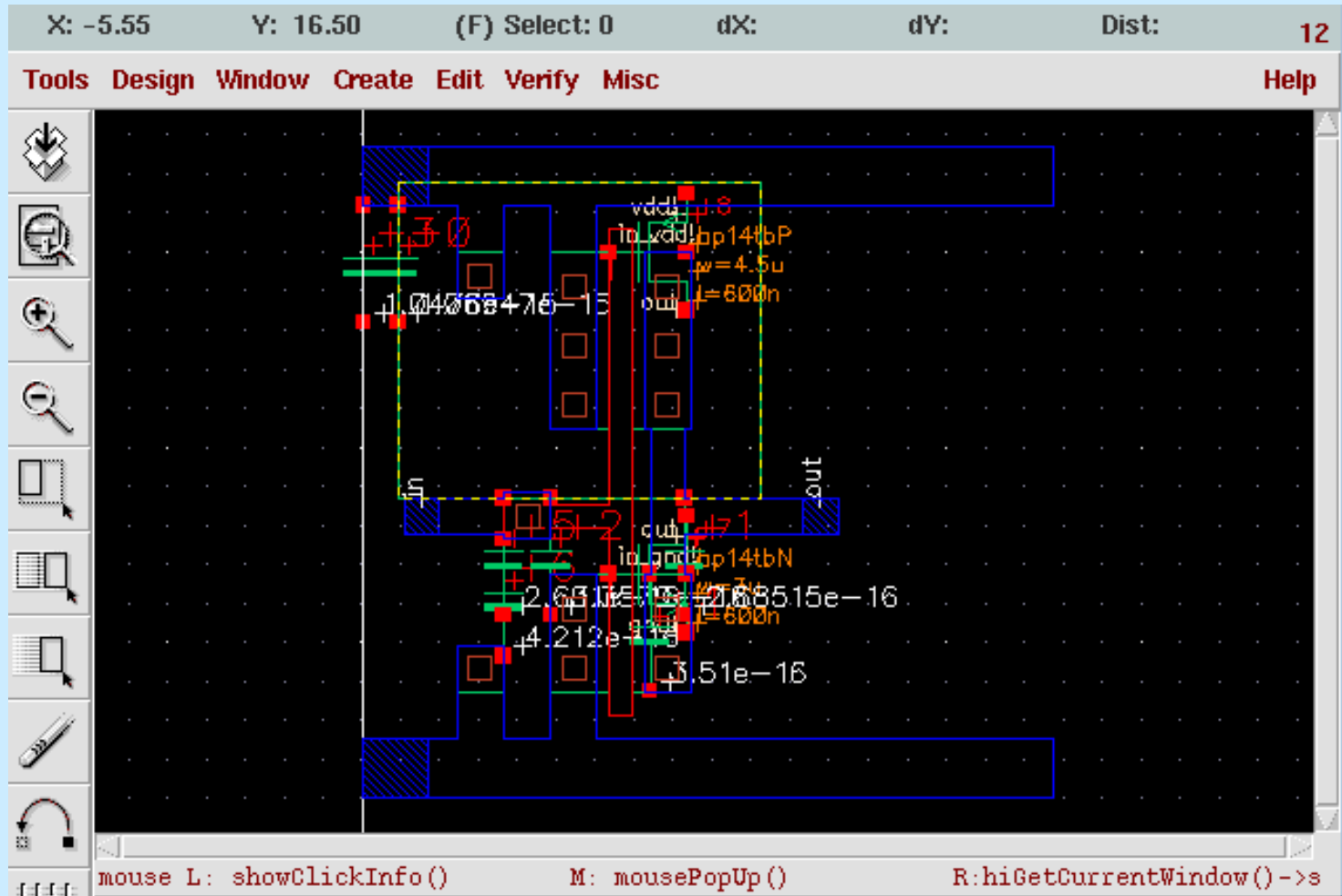


Notice that only the I/O pins appear as solid blocks and all other shapes appear as outlines.

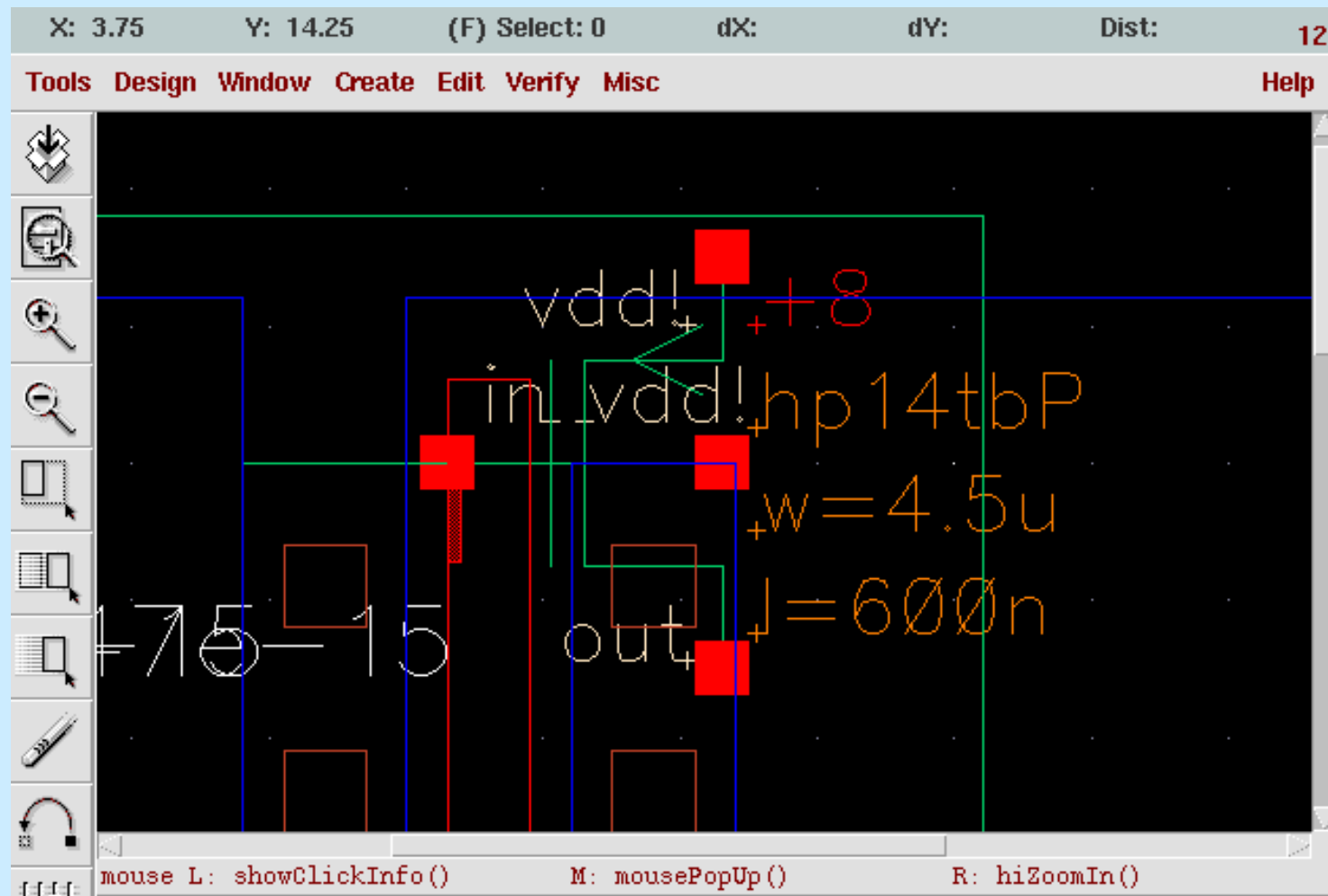
The Extracted Cell View

The red rectangles indicate that there are a number of instances within this hierarchy.

Press
Shift-F to
see all of
the
hierarchy.

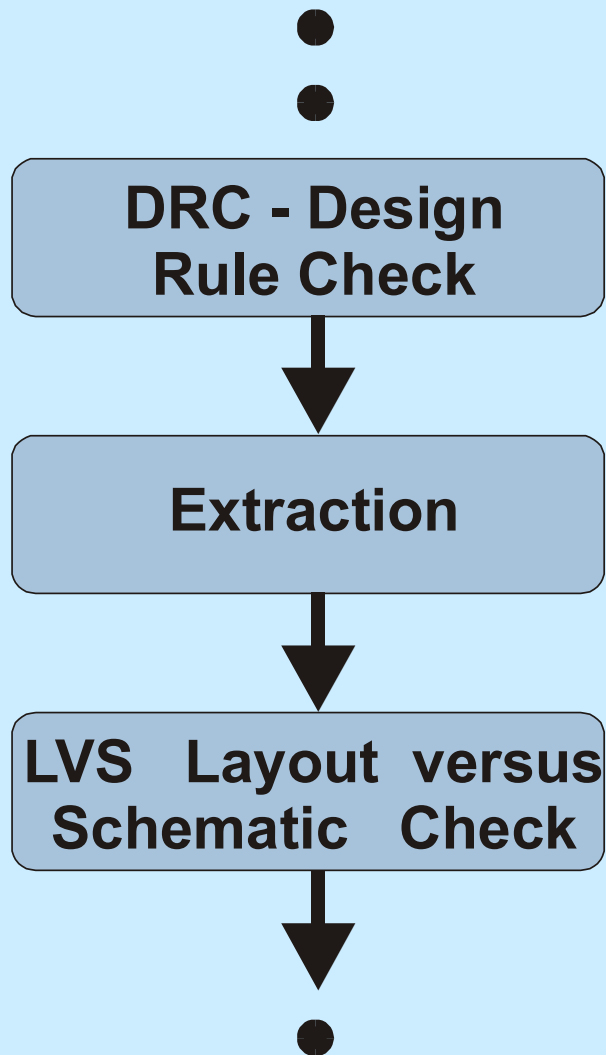


The Extracted Cell View



Notice a number of elements, mainly capacitors.
They are parasitic capacitances.

Layout versus Schematic Check

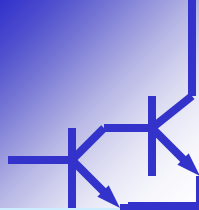


- Compares the original network with the one extracted from the mask layout

- Proves that the two networks are indeed equivalent

- Provides an additional level of confidence for the integrity of the design

- Ensures that the mask layout is a correct realization of the intended circuit topology



Layout versus Schematic Check

1. From the *Verify* menu select the option *LVS*.

Tools Design Window Create Edit Verify Misc

DRC...

Extract...

SCA...

ERC...

LVS...

Probe...

Markers ▶

If you had previously run a LVS check, this would pop-up a small warning box. Make sure that the option *Form Contents* is selected in this box.



OK

Cancel

The selected LVS Run directory does not match the Run Form.

Use



Form Contents



Run Directory Contents

Differences:

Extracted Library Name: wpi9801

Extracted Cell Name: SREG_TEST

Layout versus Schematic Check

Although there are a number of options for LVS, the default options will be enough for basic operations, select *Run* to start the comparison.

Commands Help 13

Run Directory LVS Browse

Create Netlist ☒ schematic ☒ extracted

Library EXAMPLES_390X EXAMPLES_390X

Cell inv inv

View schematic extracted

Browse Sel by Cursor Browse Sel by Cursor

Rules File divaLVS.rul Browse

Rules Library ☒ EXAMPLES_390X

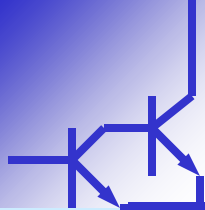
LVS Options ☒ Rewiring ☐ Device Fixing
☐ Create Cross Reference ☒ Terminals

Correspondence File ☐ lvs_corr_file Create

Priority Q Run local

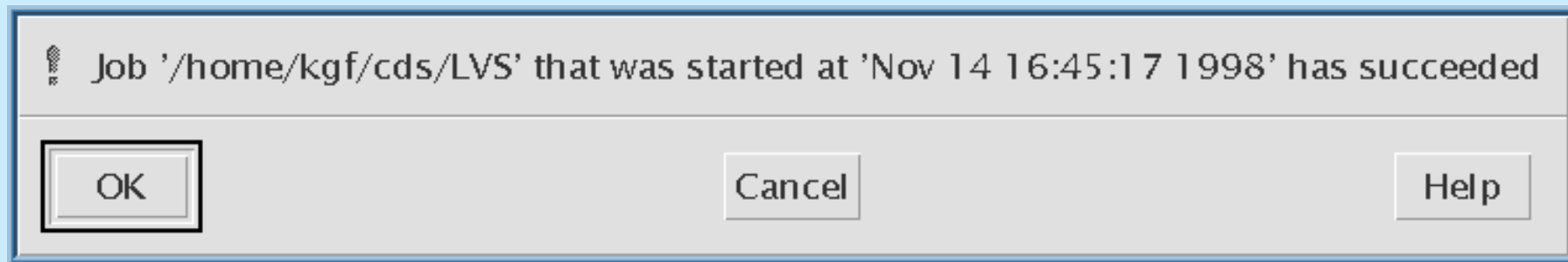
Run Output Error Display Monitor Info

Backannotate Parasitic Probe Build Analog Build Mixed



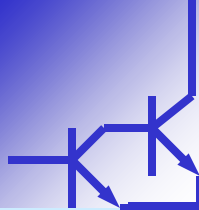
Layout versus Schematic Check

Even for a very small design the LVS run can take some time (minutes).



The *succeeded* message box

The above message box, indicates that the LVS program has finished comparing the netlists, **NOT THAT THE CIRCUITS MATCH**. It might be the case that the LVS was successful in comparing the netlists and came up with the result that both circuits were different.



Layout versus Schematic Check

To see the actual result of an LVS run you have to examine the output of the LVS run. The *Output* option is right next to the *Run* command

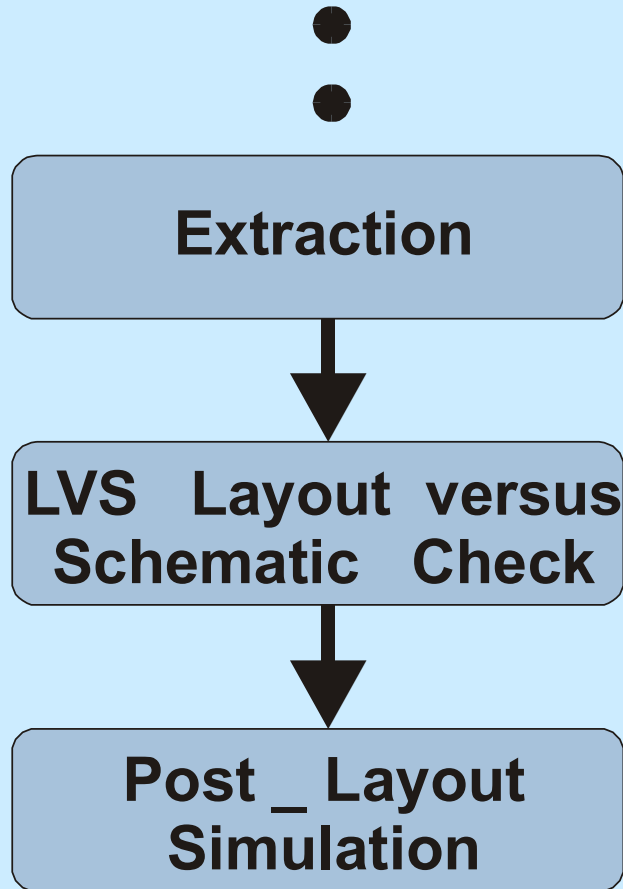
```
Terminal correspondence points
```

```
1      gnd!  
2      in  
3      out  
4      vdd!
```

```
The net-lists match.
```

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	2	2
total	2	2

Post-layout Simulation



Steps of Postlayout Simulation

- Extracting from the Layout
- The Extracted Cell View
- Layout Versus Schematic
- Summary of the Cell Views
- Simulating the Extracted Cell View

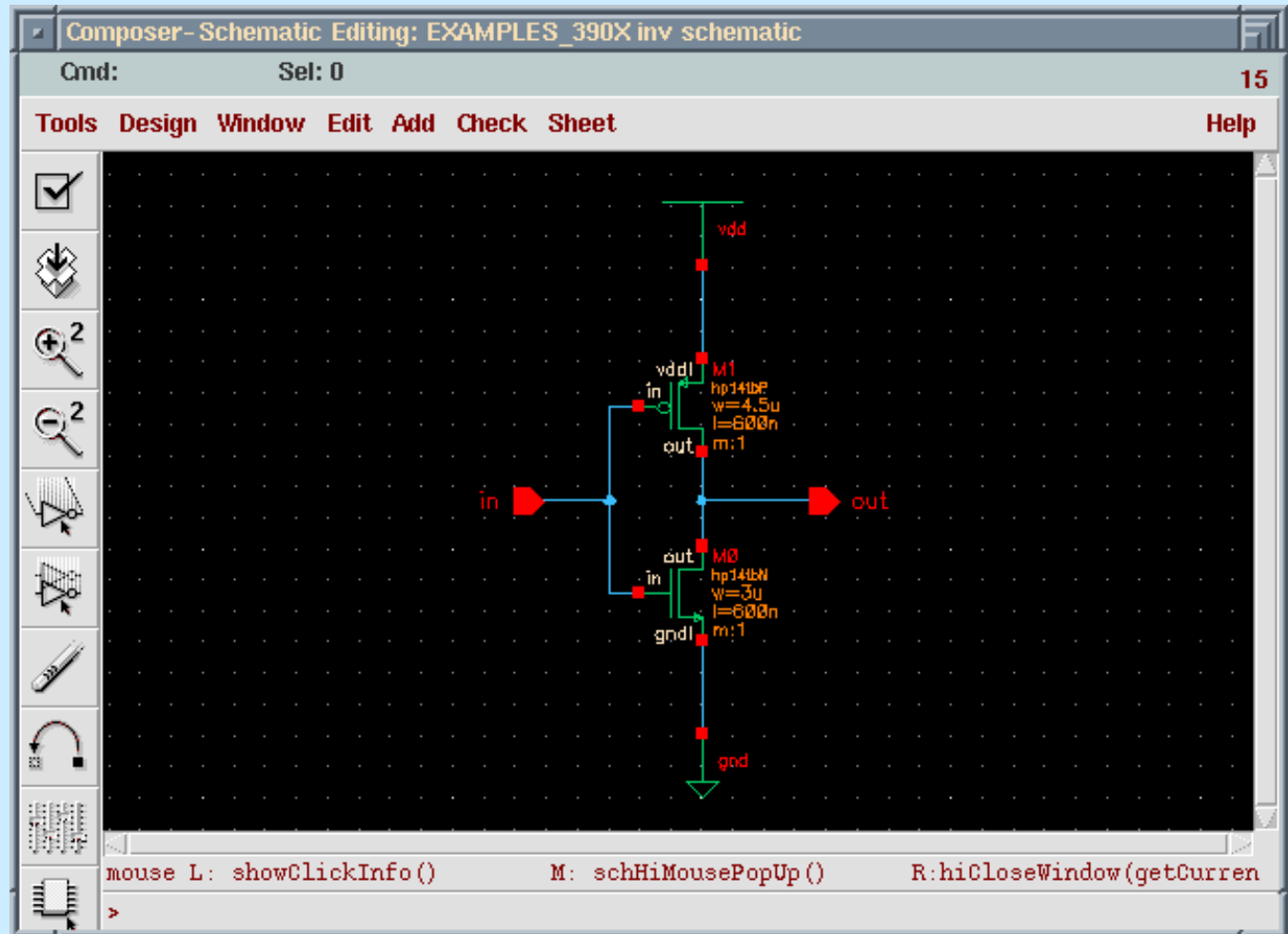
(First three described earlier)

FINISH

Summary of the Cell Views

1. Schematic view

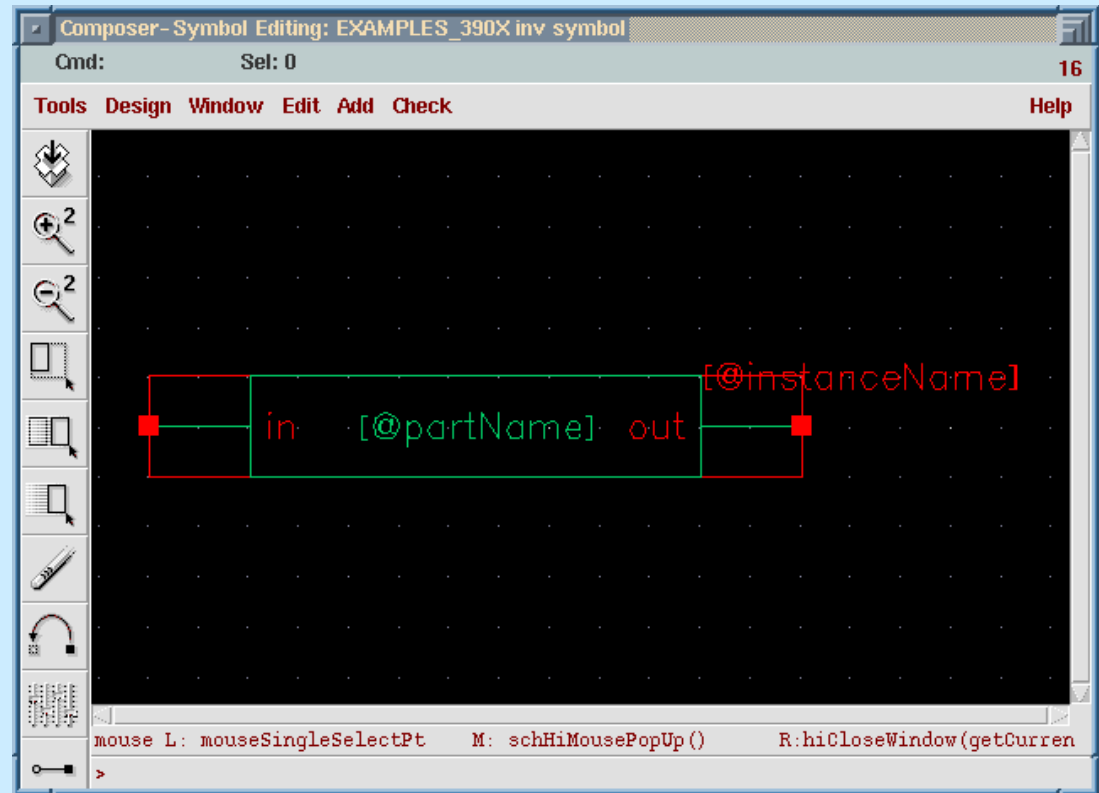
For any design, the schematic should be the first cell view to be created. The schematic will be the basic reference of your circuit.



Summary of the Cell Views

2. Symbol view

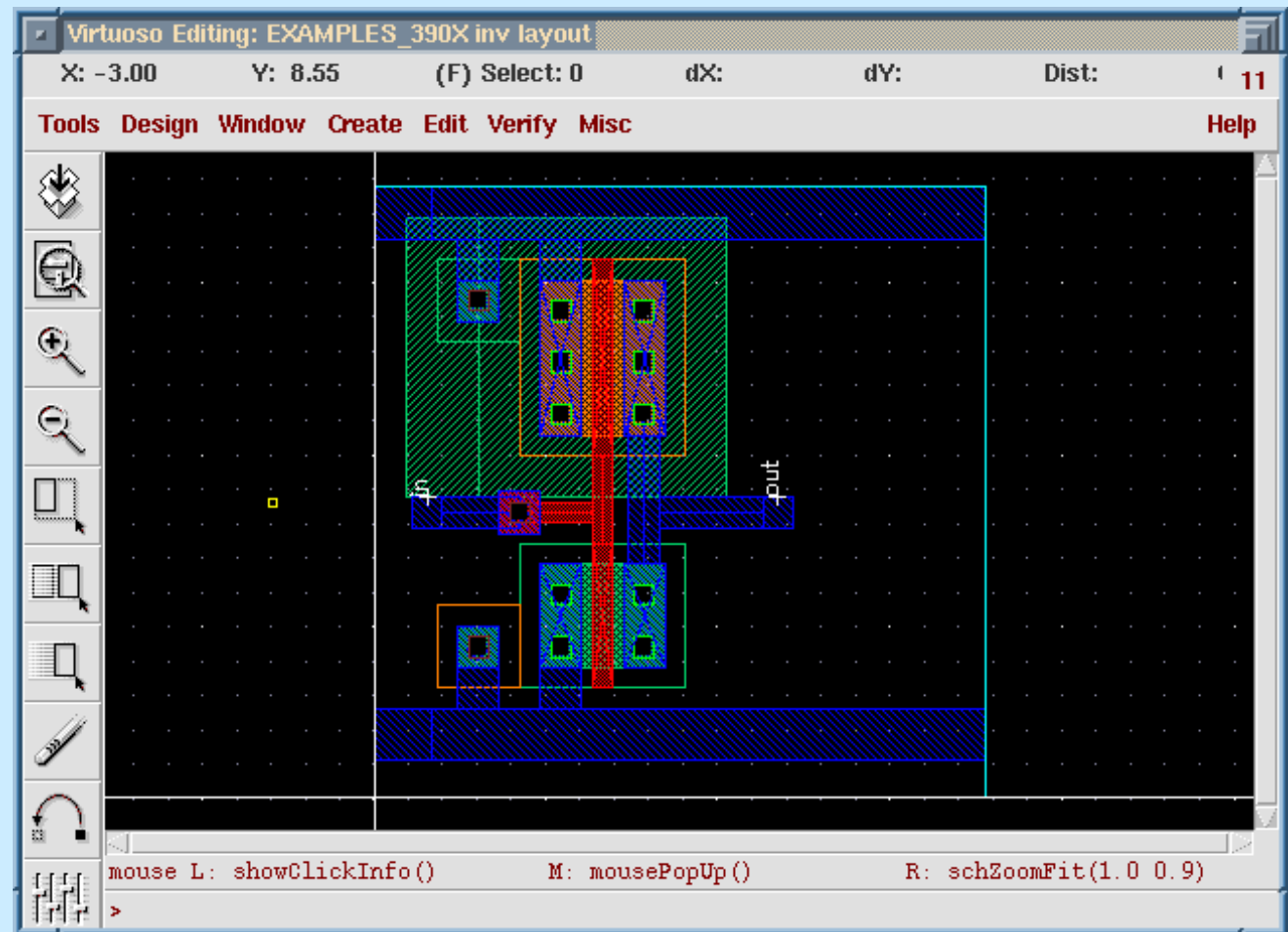
After you are done with the schematic, you will need to simulate your design. The proper way of doing this is to create a separate test schematic and include your circuit as a block. Therefore you will need to create a symbol.



Summary of the Cell Views

3. Layout view

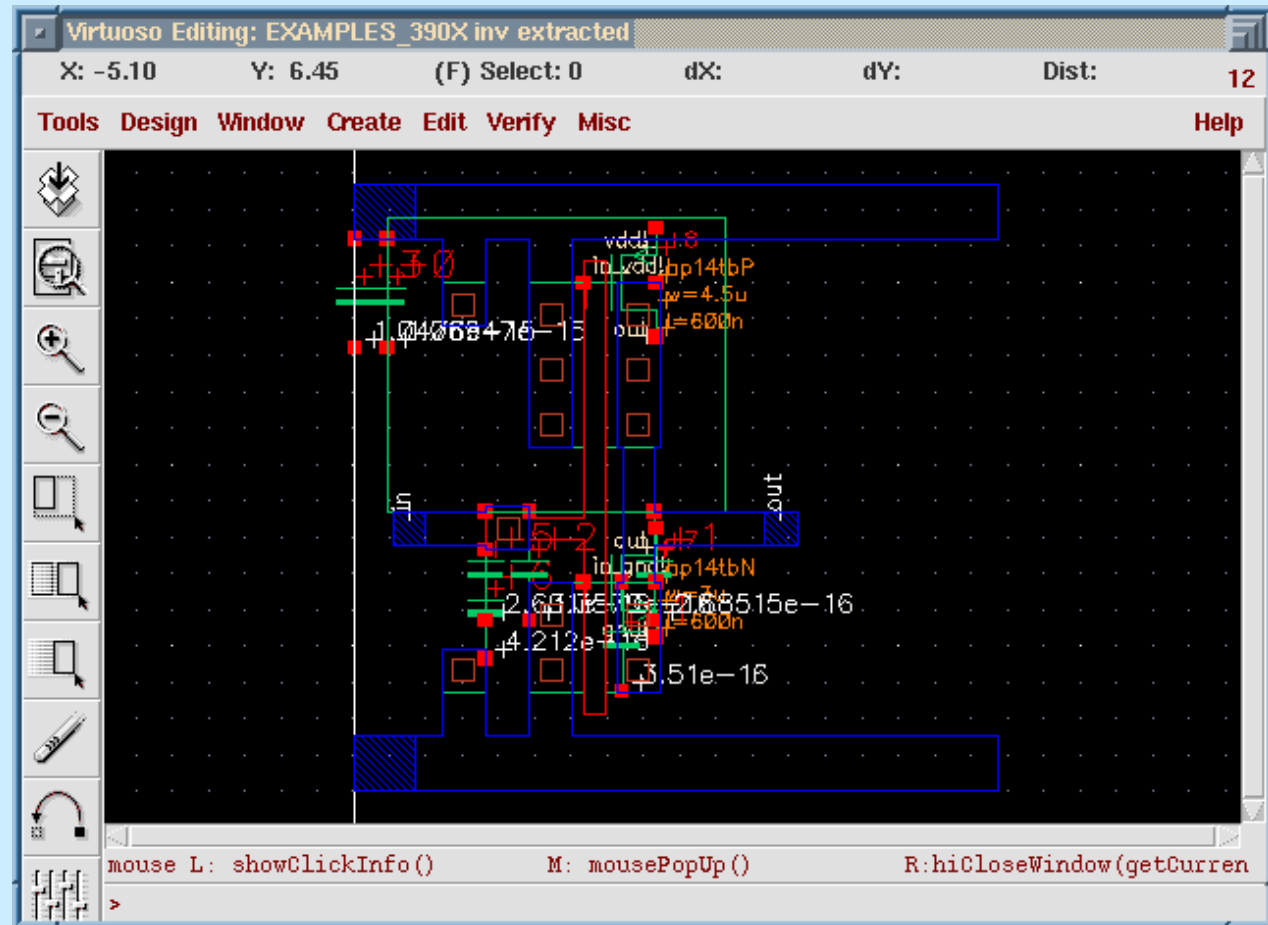
This is the actual layout mask data that will be fabricated.



Summary of the Cell Views

4. Extracted view

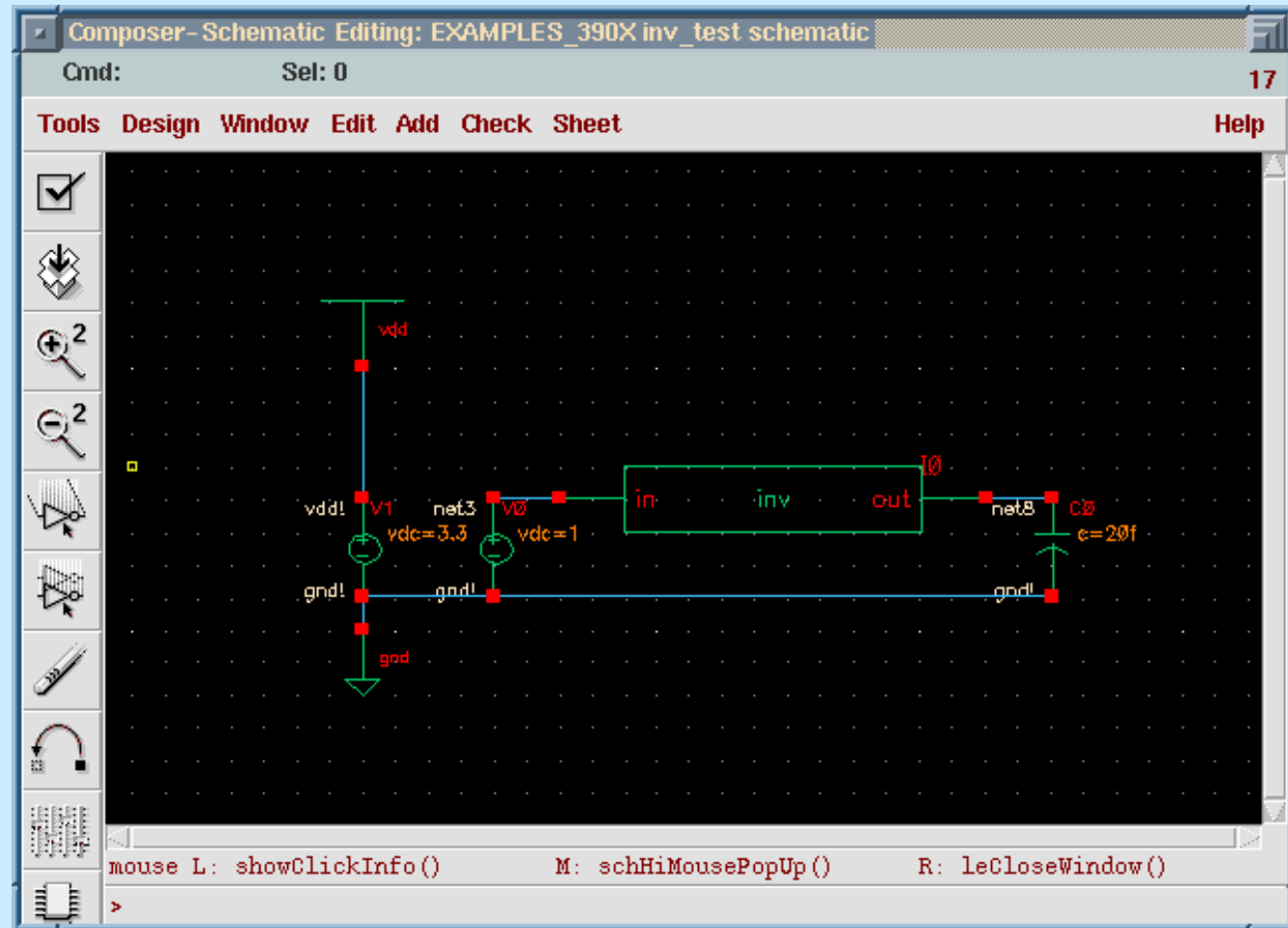
After the layout has been finalized, it is extracted, devices and parasitic elements are identified and a netlist is formed.



Summary of the Cell Views

5. Test Schematic

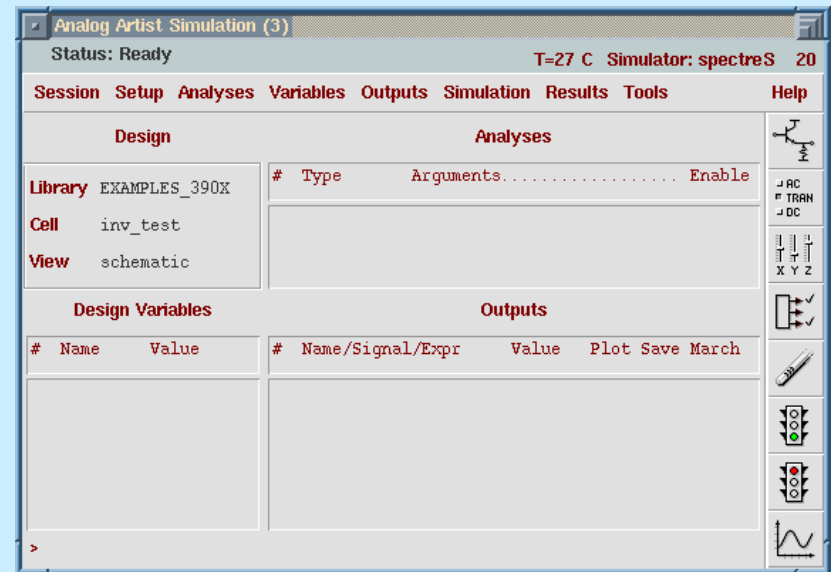
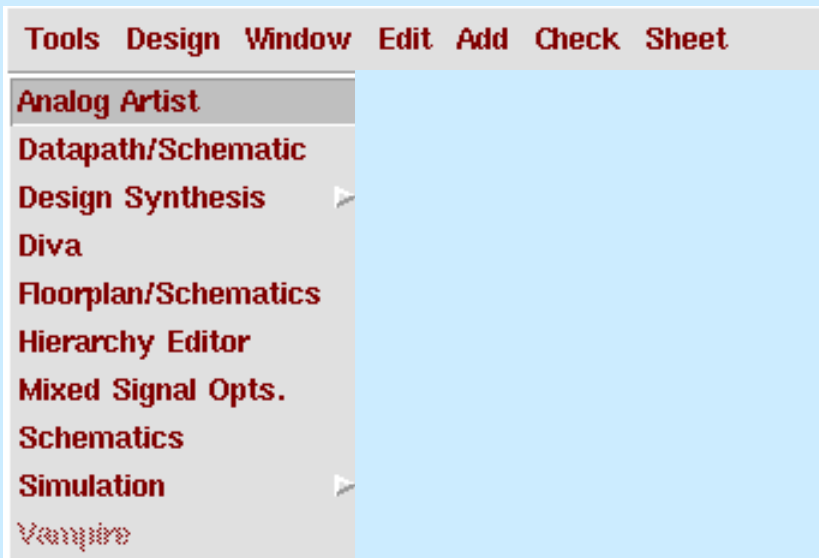
A separate cell is used to as a test bench. This test bench includes sources, loads and the circuit to be tested. The test cell usually consists of a single schematic only.



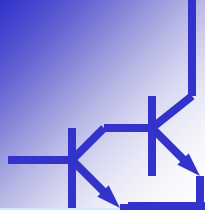
Simulating the Extracted Cell View

Make sure that you are in the test schematic, that you used to simulate your design earlier.

1. Start Analog Artist using *Tools --> Analog Artist*

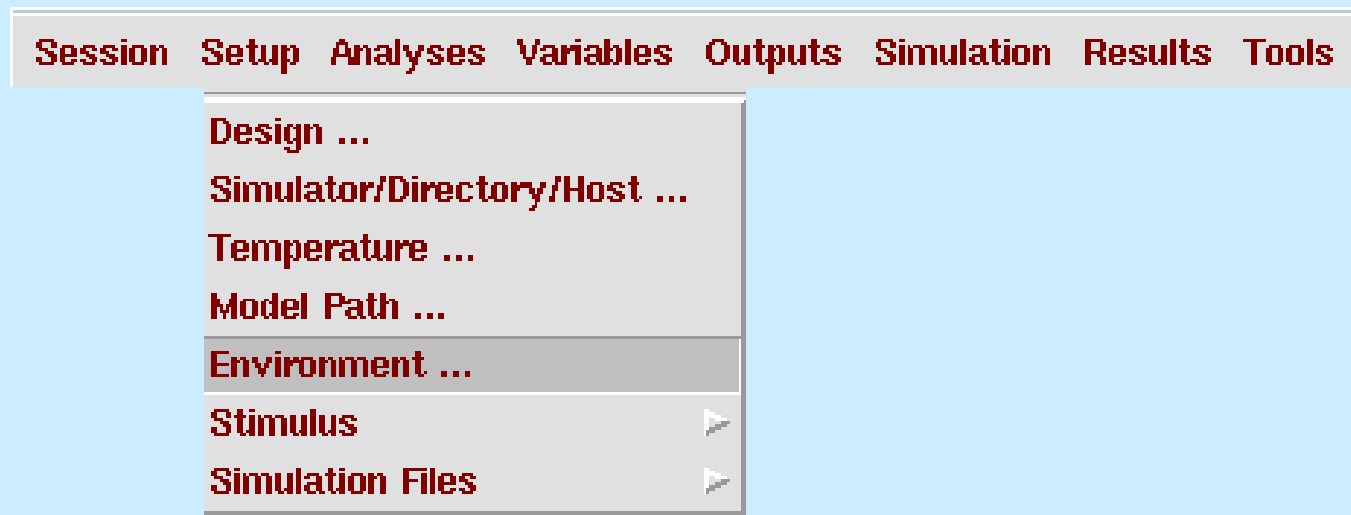


The Analog Artist window will pop-up.



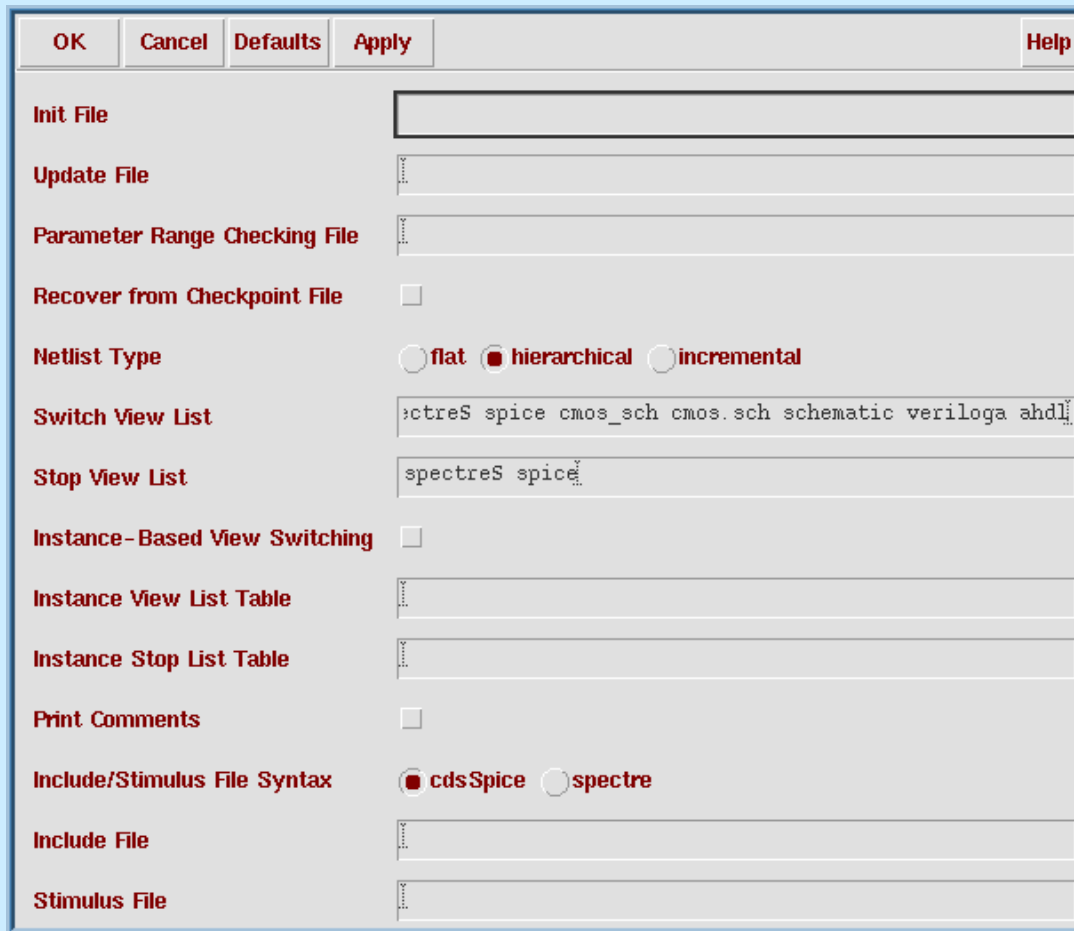
Simulating the Extracted Cell View

2. From the *Setup* menu choose the *Environment* option.



A new dialog box controlling various parameters of Analog Artist will pop-up...

Simulating the Extracted Cell View



OK Cancel Defaults Apply Help

Init File

Update File

Parameter Range Checking File

Recover from Checkpoint File ☐

Netlist Type ☐ flat ☒ hierarchical ☐ incremental

Switch View List spectreS spice cmos_sch cmos.sch schematic veriloga ahdl

Stop View List spectreS spice

Instance-Based View Switching ☐

Instance View List Table

Instance Stop List Table

Print Comments ☐

Include/Stimulus File Syntax ☒ cdsSpice ☐ spectre

Include File

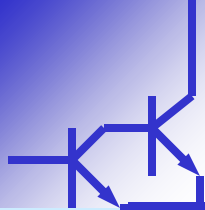
Stimulus File

Alter the line called
the *Switch View List*.

This entry is an
ordered list of cell
views that contain
information that can
be simulated.

Switch View List

spectreS spice cmos_sch cmos.sch extracted schematic



Simulating the Extracted Cell View

3. Choose analyses

Session Setup Analyses Variables Outputs Simulation Results Tools

Choose ...
Delete
Enable
Disable

For example DC analysis

The screenshot shows a dialog box titled "DC Analysis". At the top, there are buttons for "OK", "Cancel", "Defaults", "Apply", and "Help". Below these, the "Analysis" section contains eight radio buttons: "tran", "ac", "sp", "spss", "dc" (which is selected), "xf", "pss", and "noise". The "DC Analysis" section has a checkbox for "Save DC Operating Point" which is currently unchecked. Below this is a "Sweep Variable" section with three checkboxes: "Temperature", "Component Parameter", and "Model Parameter", all of which are unchecked. At the bottom left, the word "Enabled" is displayed. At the bottom right, there is an "Options..." button.

The first step is to determine what parameter will be swept.

Simulating the Extracted Cell View

Choose Component Parameter as the Sweep Variable.

You can select the parameter from the schematic window after you click on *Select Component...*

The screenshot shows a simulation dialog box with the following sections:

- Buttons:** OK, Cancel, Defaults, Apply, Help.
- Analysis:** Radio buttons for tran, ac, sp, spss, dc (selected), xf, pss, and noise.
- DC Analysis:**
 - Save DC Operating Point: ☐
 - Sweep Variable:**
 - ☐ Temperature
 - ☒ Component Parameter
 - ☐ Model Parameter
 - Component Name: (with a "Select Component" button next to it)
 - Parameter Name:
- Sweep Range:**
 - ☒ Start-Stop
 - ☐ Center-Span
 - Start: Stop:
- Sweep Type:**
 - ☐ Linear
 - ☐ Logarithmic
 - ☒ Automatic
- Add Specific Points: ☐
- Enabled: ☒
- Options... button

Simulating the Extracted Cell View

As each component has a number of parameters, you will be given a list of parameters associated with the component you select.

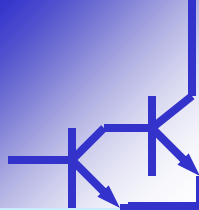
Cmd: Sel: 0 Status: Ready T=27 C Simulator: spectreS 19

Tools Design Window Edit Add Check Sheet Mixed-Signal Help

Parameter dialog box:

dc	vdc	"DC voltage"
mag	acm	"AC magnitude"
phase	acp	"AC phase"
tc1	tc1	"Temperature coefficient"
tc2	tc2	"Temperature coefficient"
tnom	tnom	"Nominal temperature"

info() M: schHiMousePopUp() R: schZoomFit(1.0 0.9)



Simulating the Extracted Cell View

After we have selected the variable we can decide, the range where the variable will change.

This example changes the DC voltage source connected to the input from 0 Volts to 3.3 Volts.

The screenshot shows the 'DC Analysis' dialog box with the following settings:

- Analysis:** ☒ dc, ☐ tran, ☐ ac, ☐ xf, ☐ sp, ☐ pss, ☐ spss, ☐ noise.
- DC Analysis:**
 - Save DC Operating Point:** ☐
 - Sweep Variable:**
 - ☐ Temperature
 - ☒ Component Parameter
 - ☐ Model Parameter
 - Component Name:** /V0
 - Parameter Name:** dc
 - Sweep Range:**
 - ☒ Start-Stop
 - ☐ Center-Span
 - Start:** 0
 - Stop:** 3.3
 - Sweep Type:**
 - ☐ Linear
 - ☐ Logarithmic
 - ☒ Automatic
 - Add Specific Points:** ☐
- Enabled:** ☒
- Options...** button.

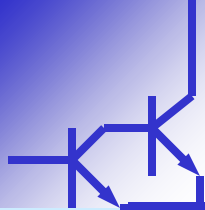
Simulating the Extracted Cell View

The last parameter determines how the sweep will be performed. A linear sweep will increment the value of the sweep variable by a fixed amount.

The example uses a step size of 10 millivolts.

The screenshot shows a simulation dialog box with the following sections:

- Buttons:** OK, Cancel, Defaults, Apply, Help.
- Analysis:** Radio buttons for tran, ac, sp, spss, dc (selected), xf, pss, and noise.
- DC Analysis:**
 - Save DC Operating Point:** A checkbox that is currently unchecked.
 - Sweep Variable:**
 - Radio buttons for Temperature, Component Parameter (selected), and Model Parameter.
 - Component Name:** A text box containing "/V0".
 - Parameter Name:** A text box containing "dc".
 - Select Component:** A button.
 - Sweep Range:**
 - Radio buttons for Start-Stop (selected) and Center-Span.
 - Start:** A text box containing "0".
 - Stop:** A text box containing "3.3".
 - Sweep Type:**
 - Radio buttons for Linear (selected), Logarithmic, and Automatic.
 - Step Size:** A text box containing "10m".
 - Radio buttons for Step Size (selected) and Total Points.
 - Add Specific Points:** A checkbox that is currently unchecked.
- Enabled:** A checkbox that is checked.
- Options...** A button.



Simulating the Extracted Cell View

Choose another analyses

Session Setup Analyses Variables Outputs Simulation Results Tools

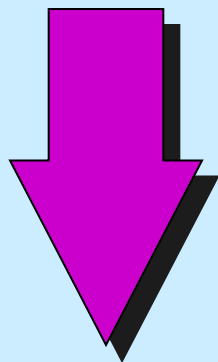
Choose ...

Delete

Enable

Disable

For example tran, noise ect.
till you will be satisfied of
your circuit.



End of Design
SEND to FOUNDRY

OK Cancel Defaults Apply Help

Analysis ☐ tran ☐ ac ☐ sp ☐ spss
☒ dc ☐ xf ☐ pss ☐ noise

DC Analysis

Save DC Operating Point ☐

Sweep Variable

☐ Temperature
☐ Component Parameter
☐ Model Parameter

Enabled Options...