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Study on a Non-Isolated High Step-Up SEPIC-Based DC-DC Converter with Continuous Input Current for Photovoltaic Applications

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ABSTRACT

This paper aims to present, study, and analyze a novel non-isolated high step-up SEPIC-based DC-DC converter for photovoltaic applications. The proposed structure is drafted from the SEPIC converter. A two-winding coupled inductor and an improved voltage multiplier cell are utilized to achieve a high voltage conversion ratio. Moreover, a passive voltage clamp is employed to recycle the stored energy in the leakage inductance of the coupled inductor and reduce the voltage stress on the switch. Hence, a switch with low on-resistance could be used. Since all diodes turn off under ZCS conditions, their reverse recovery problems are alleviated. High efficiency, continuous input current, and low cost and size are the other merits of the presented structure, making it a promising solution for photovoltaic systems. At the end, the proposed converter is compared with several DC-DC structures to prove its advantages over the converters presented before. To verify the performance of the designed topology, a 200-W laboratory prototype is implemented and experimental results are depicted. The Results validate the practicability and functionality of the proposed structure for photovoltaic applications.

I. Introduction

Nowadays, a large proportion of electricity used around the world is generated by burning fossil fuels. However, their sources are limited and over-consumption could lead to severe environmental damages such as air pollution and greenhouse emissions. The aforementioned problems along with the capability of renewable energy sources (RESs) to generate clean electricity have led governments and researchers to increase their contribution to electric production [1], [2].

Thanks to energy policies for supporting low or zero-carbon infrastructures, the deployment of photovoltaic (PV) systems has increased significantly in the last decades. High reliability, low maintenance cost, long life span, environmental friendliness, zero or low emissions, and noise are some unique properties of PV systems [3], [4]. However, the voltage provided by PV panels is relatively low in amplitude. Hence, the interfacing DC-DC converters with high voltage gains are utilized to link PV panels to grid-connected inverters [5]- [7]. The other essential requirement in designing DC-DC converters for PV applications is draining continuous current with minimum ripple. Otherwise, the maximum power point tracking (MPPT) algorithm might not operate efficiently [8], [9]. To this end, authors in [10] and [11] have presented a couple of ripple-free non-isolated DC-DC converters for RES applications. In both presented structures, an inductor is in series with an input voltage source to achieve the minimum input current ripple. However, they suffer from low voltage gain which makes them unsuitable for PV applications.

Generally, DC-DC converters which are employed in PV applications could be categorized in two classes including isolated and non-isolated structures. Isolated configurations are mainly based on multi-winding transformers. However,

utilizing the power transformer reduces the efficiency and increases the converter weight and volume [12], [13]. Compared to isolated structures, non-isolated converters share a common ground between the input source and the load. Moreover, they are not isolated electrically. Non-isolated converters are derived from either conventional structures like buck, boost, and buck-boost converters or developed configurations such as Single-ended primary-inductor converter (SEPIC), Ćuk, and Zeta converters [14], [15].

The power circuit of the SEPIC topology is depicted in Fig. 1. Continuous input current and shared common ground between the input source, the load, and the main switch are outstanding characteristics of the SEPIC structure. However, the voltage gain is still low for PV applications.

In literature, a few techniques have been addressed to enhance voltage gains of DC-DC converters. Switched inductors and capacitors, Z-source and quasi Z-source, voltage lift, and voltage multiplier cells are some of the well-known methods [16]- [19]. Another method that researchers use to increase voltage gains of DC-DC converters is utilizing coupled inductors (CIs). In [20], a SEPIC-based DC-DC structure with a CI is studied. Continuous input current and high voltage gain are significant characteristics of the presented topology. Moreover, the energy stored in the leakage inductance of the CI is recycled by a passive voltage clamp. Authors have presented another CI-based converter in [21]. Output voltage level is boosted by using a CI and a voltage multiplier cell. Since a switch is in series with the input voltage source, the input current is not continuous. Hence, it might not be a practical solution to achieve MPPT in PV applications.

In [22], another high step-up DC-DC converter based on CI and switched inductor is presented. The converter benefits from a high voltage conversion ratio. However, regarding the total numbers of components, achieved voltage gain is not suitable. Moreover, the input current ripple is high which makes it unpromising for PV applications.

According to Fig. 1, the main features of a high gain SEPIC-based DC-DC structure could be summarized as: 1) High voltage gain could be obtained by utilization of a CI, 2) Thanks to the presence of two inductors in SEPIC structure, input inductor could be utilized to guarantee that input current is continuous and the inductor L_2 can be converted to a CI, 3) Due to low current ripple in the primary section of the converter, the root mean square (RMS) value of current that is flowing through the switch is significantly reduced, 4) As the average current of second inductor L_2 is low, the average current of the replaced CI will be low and as a result, a small core could be chosen.

This study is devoted to presenting, studying, and analyzing make it a promising solution for PV systems. High voltage gain is attained by utilizing a CI along with an improved

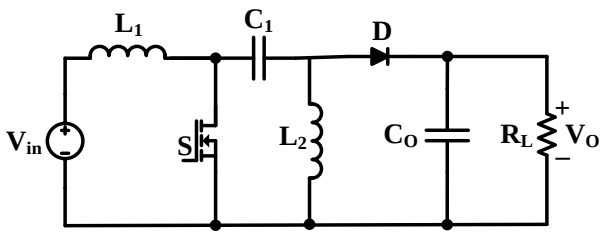

Fig. 1. The Power circuit of the SEPIC structure

voltage multiplier module. Capacitors of the voltage multiplier module are charged by both the primary and secondary sides of CI. Meanwhile, to recycle stored energy in the leakage inductance of the CI, a passive voltage clamp is used. Hence, the voltage across the switch is reduced remarkably, and a low on-resistance (R_{DS-ON}) switch could be utilized. As a result, the structure's cost and conduction power dissipation will be reduced and the efficiency of the proposed converter will be increased. Besides, thanks to the soft switching performance of all diodes at turn-off instant, their reverse recovery problems are eliminated.

II. Operating Principles and Steady State Analysis of the Proposed Converter

Fig. 2 shows the equivalent circuit of the designed high step-up SEPIC-based DC-DC converter. As illustrated in this figure, the presented structure includes a switch S, an input inductor L_{in}, one CI with a turns ratio of n, three capacitors C_1-C_3, an output capacitor C_O, and three diodes D_1-D_3. The capacitor C_2 along with the diode D_1 form the passive voltage clamp. Moreover, an improved voltage multiplier module is employed to enhance the voltage conversion ratio of the presented converter. As depicted in this figure and unlike most conventional DC-DC converters in which the voltage multiplier cell is charged only by the secondary side of the CI, the capacitor C_3 is charged by both primary and secondary windings of the CI.

To simplify the steady-state analysis of the structure, the CI with a turns ratio of $n=N_s/N_p$ is modelled by an ideal transformer that its primary winding is in parallel with magnetizing inductance L_m and in series with the leakage inductance L_k. Moreover, it is assumed that: 1) All capacitors and inductors are large enough without any ripple in their voltages and currents, respectively. 2) All semiconductor components are ideal without parasitic components.

The operating principles of the studied structure in continuous conduction mode (CCM) include five time periods. Current flow paths and main waveforms of operating modes are illustrated in Fig. 3 and Fig. 4, respectively. Operating modes and relative steady-state analysis are explained as follows.

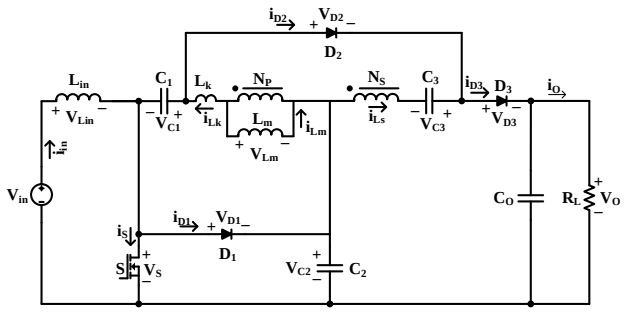

Fig. 2. Equivalent circuit of the presented structure

***Mode I [t_0-t_1]*:** The first mode begins when the switch S is turned on under the ZCS condition at $t=t_0$. Due to the leakage inductance of CI, the diode D_2 is still conducting. While diodes D_1 and D_3 are in off-state. Meanwhile, the input voltage source charges the input inductor L_{in} through the switch S. Since the diode D_3 is biased reversely, the output capacitor C_O supplies energy to the load. Meanwhile, the capacitor C_1 and both sides of the CI charge capacitors C_2 and C_3 through the diode D_2. This mode ends when currents flowing through leakage and magnetizing inductances of CI are equal at $t=t_1$. The following equation could be given for the current flowing through the CI.

$$i_{Lk} = \frac{1}{L_K}\int\left(V_{C2} - V_{C1} + \frac{V_{C3}}{1+n}\right)dt \tag{1}$$

As the voltage across the CI is high and L_k has a low value, the slope of this current is sharp. Hence, the duration of this mode is too short. The relative current-flow path of this mode is depicted in Fig. 3(a).

***Mode II [t_1-t_2]*:** This mode begins when diode D_2 turns off under ZCS condition at $t=t_1$. During this mode, the switch S remains on. Meanwhile, input current increases linearly like mode I. Furthermore, the capacitor C_2 charges both the capacitor C_1 and the CI through the switch S. Energy stored in capacitors C_2 and C_3 along with the CI are transferred to the output capacitor C_O and the load through the diode D_3. This mode ends when the switch S is turned off at $t=t_2$. Fig. 3(b) shows the relative current-flow path. The following equations could be obtained for this mode.

$$v_{Lin} = V_{in} \tag{2}$$

$$v_{Lm} = V_{C1} - V_{C2} \tag{3}$$

$$i_s = i_{in} + i_{Lk} \tag{4}$$

$$n\left(V_{C2} - V_{C1}\right) = V_O - V_{C2} - V_{C3} \tag{5}$$

Mode III [t_2-t_3]: As depicted in Fig. 3(c), the switch S is turned off at the beginning of this mode and the clamp diode D_1 is forward biased simultaneously at $t=t_2$. Consequently, voltage across the switch S is equal with the voltage of capacitor C_2. Moreover, the clamp diode D_1 provides a path to recycle the energy stored in the leakage inductance of the CI. During this mode, the diodes D_2 and D_3 are off and on, respectively. Meanwhile, the energy of input inductor L_{in} is transferred to both the CI and the capacitor C_2. The secondary side of the CI along with the capacitor C_3 supplies energy of the output capacitor C_O and the load. This mode ends when the current which is flowing through secondary side of the CI reaches zero at $t=t_3$. Hence the diode D_3 will turn off under ZCS condition. The following equation could be achieved for the current of the CI.

$$i_{Lk} = \frac{1}{L_K}\int\left(\frac{V_O - V_{C2} - V_{C3}}{n} - V_{C1}\right)dt \tag{6}$$

Since the voltage across the CI is high and L_k has a low value, the slope of this current is sharp. Hence, like mode I, the duration of this mode is too short.

Mode IV [t_3-t_4]: At the beginning of this mode, the diode D_3 is reverse-biased under the ZCS condition. Hence, its reverse recovery problem is eliminated. During this period, diodes D_1 and D_2 are in on-state. Meanwhile, switch S remains off. The energies stored in both input inductor L_{in} and the CI are transferred to capacitors C_2 and C_3. The output capacitor C_O supplies the load. This mode ends when the current which is flowing through the clamp diode D_1 reaches zero at $t=t_4$. Fig. 3(d) shows the relative current-flow path of this mode. The following equations could be formulated for this mode.

$$v_{Lin} = V_{in} - V_{C2} \tag{7}$$

$$v_{Lm} = V_{C1} \tag{8}$$

$$V_{C1} = \frac{V_{C3}}{n+1} \tag{9}$$

Mode V [t_4-t_5]: The last mode begins when clamp diode D_1 is reverse-biased under ZCS condition at $t=t_4$. During this time interval, the switch S and the output diode D_3 are in off-state as well. Meanwhile, the diode D_2 is conducting and energy of both sides of the CI is transferred to the capacitor C_3. Furthermore, the output capacitor C_O supplies the load. The current of input inductor L_{in} declines linearly like in mode IV. Fig. 3(e) shows the relative current-flow path of this mode.

To simplify the steady-state analysis of the proposed structure, short time durations that happen in one complete switching cycle are neglected. Moreover, the voltages of capacitors are presumed to be constant without any ripple.

Employing principle of volt-second balance on inductors in different modes, following equations could be obtained.

$$\left\langle v_{Lin}\right\rangle = 0 \Rightarrow V_{C2} = \frac{V_{in}}{1-D} \tag{10}$$

$$\left\langle v_{Lm}\right\rangle = 0 \Rightarrow V_{C1} = DV_{C2} \Rightarrow V_{C1} = \frac{DV_{in}}{1-D} \tag{11}$$

Where $\langle v_{Lin}\rangle$ and $\langle v_{Lm}\rangle$ are the average voltage values of input inductor L_{in} and magnetizing inductance of the CI in one complete switching cycle, respectively. Substituting (11) into (9), the voltage of capacitor C_3 could be obtained as:

$$V_{C3} = \frac{(n+1)DV_{in}}{1-D} \tag{12}$$

Substituting (10), (11) and (12) into (5), yields to:

$$M_{CCM} = \frac{V_O}{V_{in}} = \frac{n+1+D}{1-D} \tag{13}$$

It's worth mentioning that since the current that is flowing through the CI is low, influence of leakage inductance of the CI on the voltage conversion ratio is low and ignorable [20].

III. Design of Proposed Converter

Determining voltage and current stresses on semiconductors is crucial in designing the converter. According to Fig. 3, voltage stresses on semiconductors could be formulated as:

$$V_{S,peak} = V_{D1,peak} = V_{C2} = \frac{DV_{in}}{1-D} \tag{14}$$

$$V_{D2,peak} = V_{D3,peak} = V_O - V_{C1} = \frac{(n+D)V_{in}}{1-D} \tag{15}$$

Current which is flowing through the capacitor C_1 could be given by:

$$i_{C1} = \begin{cases} I_{Lm} + ni_{D3} & 0 < t \le DT_S \\ i_{D1} - I_{in} & DT_S < t \le T_S \end{cases} \tag{16}$$

By utilizing the principle of amp-second balance on the capacitor C_1, average current of magnetizing inductance of the CI could be calculated as follows.

$$\begin{aligned} &\langle i_{C1} \rangle = 0 \Rightarrow DI_{Lm} + (n+1)I_O - (1-D)I_{in} = 0 \\ &\Rightarrow I_{Lm} = I_O \end{aligned} \tag{17}$$

It could be proved that the average current values of all diodes are equal to the load current I_O. Thus, by neglecting mode III, the duration of mode IV can be achieved as follows.

$$\langle i_{D1} \rangle = I_O \Rightarrow \frac{I_{in} d_4}{2} = I_O \Rightarrow d_4 = \frac{2}{M_{CCM}} \tag{18}$$

Where d_4 is the time length of mode IV. Maximum current values of diodes D_2 and D_3 could be given by:

$$\langle i_{D2} \rangle = I_O \Rightarrow \frac{i_{D3,peak} D}{2} = I_O \Rightarrow i_{D3,peak} = \frac{2I_O}{D} \tag{19}$$

$$\begin{aligned} &\langle i_{D2} \rangle = I_O \Rightarrow \frac{i_{D2,peak}\left(1-D+(1-D-d_4)\right)}{2} = I_O \\ &\Rightarrow i_{D2,peak} = \frac{2I_O}{2(1-D)-d_4} \end{aligned} \tag{20}$$

According to Fig. 3(b), the following equation could be achieved for the current stresses of switch S and diode D_1.

$$i_{D1,peak} = i_{S,peak} = i_{in,peak} + i_{Lm,peak} + ni_{D3,peak} \tag{21}$$

Substituting (17) and (19) into (21), yields to:

$$i_{D1,peak} = i_{S,peak} = \frac{2n+(2-n)D}{D(1-D)} I_O \tag{22}$$

According to [20], operating a converter in discontinuous conduction mode has major drawbacks including slow dynamic response, high current stress of semiconductors, the dependence of the converter on switching frequency, output power, and inductors. Hence, in order to guarantee the CCM

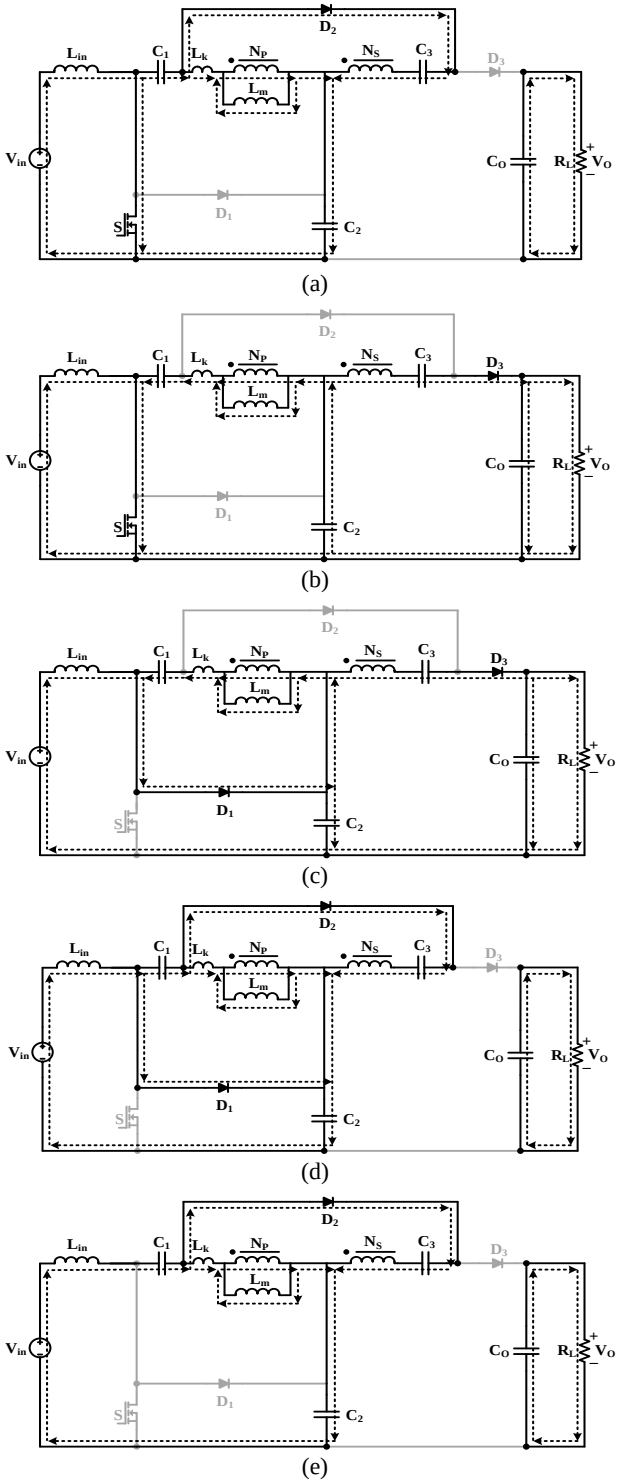

Fig. 3. Current-flow path of operating modes in one switching time interval at CCM operation. (a) Mode I, (b) Mode II, (c) Mode III, (d) Mode IV, (e) Mode V.

operation of the proposed structure, the average current values of inductors L_{in} and L_m have to be more than half of their ripples. Current ripples of inductors could be given by:

$$\Delta i_{in} = \frac{V_{in} D}{L_{in} f_S} \tag{23}$$

$$\Delta i_{Lm} = \frac{(V_{C1} - V_{C2}) D}{L_m f_S} = \frac{V_{in} D}{L_m f_S} \tag{24}$$

To guarantee the CCM operation of the presented structure, the following inequalities have to be satisfied:

$$I_{in} \geq \frac{\Delta i_{in}}{2} \Rightarrow L_{in} \geq \frac{R_L}{2 f_S M_{CCM}} \tag{25}$$

$$I_{Lm} \geq \frac{\Delta i_{Lm}}{2} \Rightarrow L_m \geq \frac{R_L}{2 f_S M_{CCM}} \tag{26}$$

IV. Comparison Study

The proposed converter and some other structures presented before are compared in terms of the type of switching, continuity of input current, number of elements, voltage gain, and voltage stresses on semiconductors in Table 1. Moreover, voltage gains of some structures in Table 1 as a function of duty ratio are depicted in Fig. 5. As shown in this figure, when duty ratio D is less or equal to 0.62, the voltage gain of the designed topology is more than other structures. For duty ratios of more than 0.62, converters presented in [5] and [17] have higher voltage gains. However, hard switching performances of converters in [5] and [17] result in higher switching losses and lower efficiency. Meanwhile, voltage stresses on the switches of both converters are higher than the proposed converter.

In addition to normalized voltage stress on switches and diodes, the other method to evaluate voltage stresses on semiconductors is component stress factor (CSF) analysis. This procedure is similar to component load factor (CLF) analysis. However, they differ in how total and individual component factors are calculated. The CSF method considers the maximum voltage on components of the structure and root mean square (RMS) values of currents flowing through them in a specific set of conditions and output power. Consequently, it gives a quantitative measure of converter performance [23].

To apply CSF analysis, it is assumed that the converters under study have the same resources of silicon, magnetic winding area, and capacitor volume. Hence, CSF analysis consists of three different parts: Semiconductor component stress factor (SCSF), winding component stress factor (WCSF), and capacitor component stress factor (CCSF). These parameters could be formulated as follows [24].

Where N_S, N_W, and N_C symbolize numbers of semiconductors, inductors, and capacitors, respectively. To reduce the complexity of the analysis, it is assumed that: 1) capacitors and inductors are large enough without any ripples in voltages and currents, respectively and 2) there is no power dissipation in components of the converter.

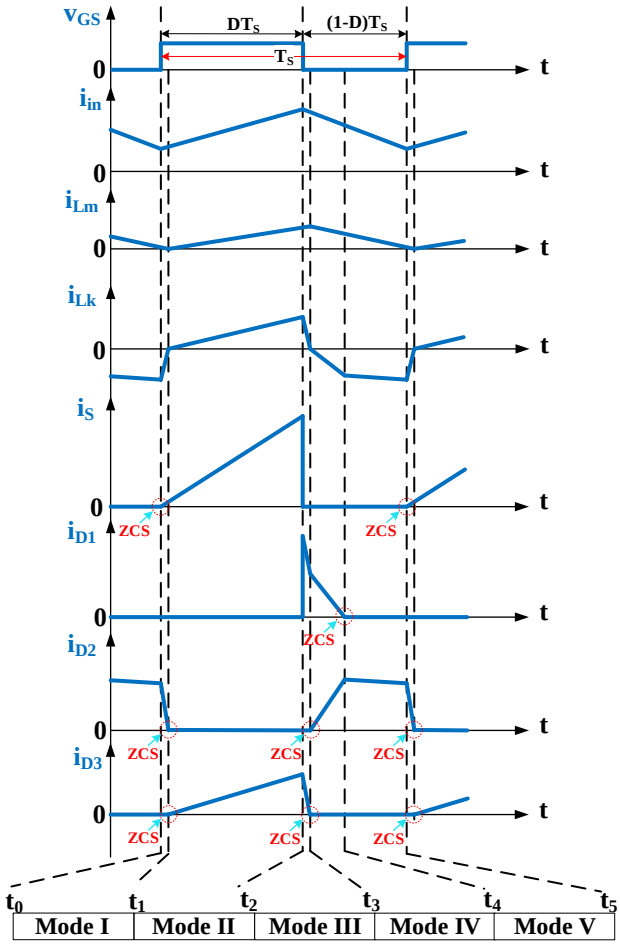

Fig. 4. Typical current waveforms of presented structure at CCM operation

$$SCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{\max}^2 . I_{rms}^2}{P_O^2} \tag{27}$$

$$WCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{\max}^2 . I_{rms}^2}{P_O^2} \tag{28}$$

$$CCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{pk}^2 . I_{rms}^2}{P_O^2} \tag{29}$$

$$SCSF = \sum_{N_s} SCSF_i \tag{30}$$

$$WCSF = \sum_{N_w} WCSF_i \tag{31}$$

$$CCSF = \sum_{N_C} CCSF_i \tag{32}$$

In Fig. 6, the normalized voltage stress on the switch of the presented structure is compared with other structures. As depicted in this figure, voltage stress across the main switch of the presented structure is less than all other topologies. Moreover, only converters presented in [12], [16] and [20] utilize ZCS switching beside the presented structure. Hence, the designed structure will have lower switching losses in

comparison with the converters mentioned in Table 1. In Fig. 7, the total amount of normalized voltage stresses on the diodes of the designed structure and some of the converters in Table 1 are compared. As illustrated in this figure, converters presented in [10], [16] and [17] have lower values than designed topology. However, the converter in [16] utilizes two switches that enhances complexity, cost and volume of the structure. Moreover, converters in [10] and [16] suffer from low voltage conversion ratio using same number of elements.

In Fig. 8, the SCSF of the proposed converter and some of the structures mentioned in Table I are compared. The SCSF of each structure is calculated with the same weighting factor. For simplicity, the weighting coefficient $\Sigma_j W_j$ is assumed to be unit and distributed equally between the semiconductors of each converter. As illustrated in this figure, the designed topology has lower SCSF than the others.

Regarding the comparisons, the presented converter is a promising solution for PV applications. Simple structure, high voltage gain, continuous input current, and soft switching performance of semiconductors are main advantages of the proposed structure. In case higher voltage gains are required, other structures could be utilized. However, higher voltage gains result in an increased number of employed components or higher voltage stresses on semiconductors. Moreover, if the designed converter will operate in duty cycles lower than 0.5, the structure in [19] could be a better solution.

V. Efficiency Analysis

Major parameters in power losses of the converter are related to the switch, diodes, capacitors, and magnetic devices. Supposing that currents of inductors have no ripples, RMS and average values of inductor currents will be equal. In calculating efficiency and power losses of designed structure, short time modes I and III are neglected.

Switch losses include switching and conduction losses. The current of the switch S could be given by:

$$i_S = \frac{i_{S,peak}}{DT_S} \mathrm{t} \quad 0 \le t < DT_S \tag{33}$$

Where T_S is the switching period. Utilizing (33), the RMS value of the switch current could be obtained as:

$$I_{S,rms} = \left(\frac{2n + (2-n)D}{\sqrt{3D}(1-D)} \right) I_O \tag{34}$$

The second element in power loss calculation is the diode. Currents that are flowing through three diodes could be formulated as follows.

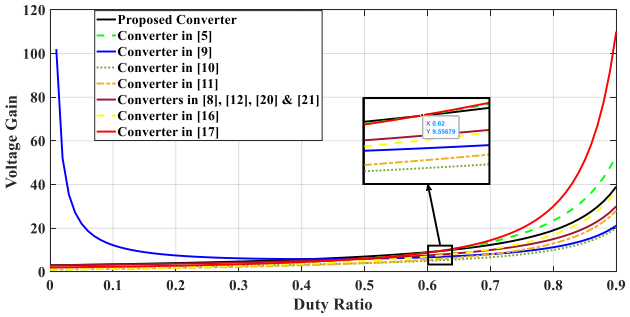

Fig. 5. Voltage conversion ratios of designed converter and topologies in [5], [8-12], [16-17] & [20-21]

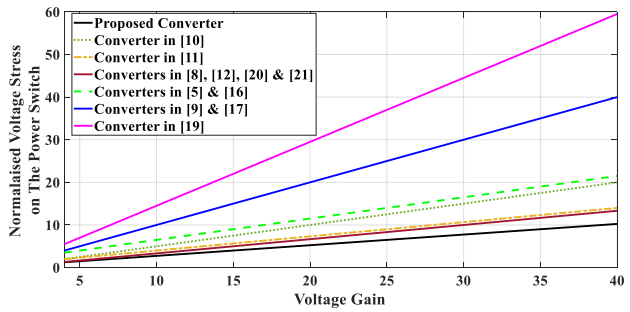

Fig. 6. Voltage stress on the switch of designed converter and topologies in [5], [8-12], [16-17] & [19-21]

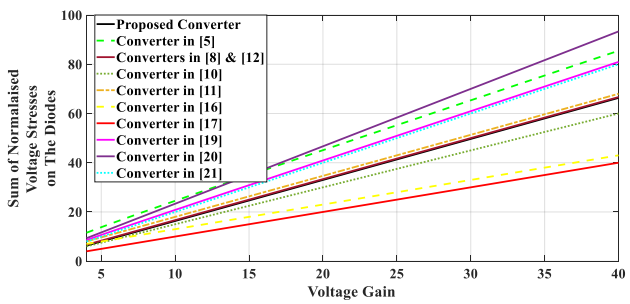

Fig. 7. Total amount of voltage stresses across diodes of the converter and converters in [5], [8-12], [16-17] & [19-21].

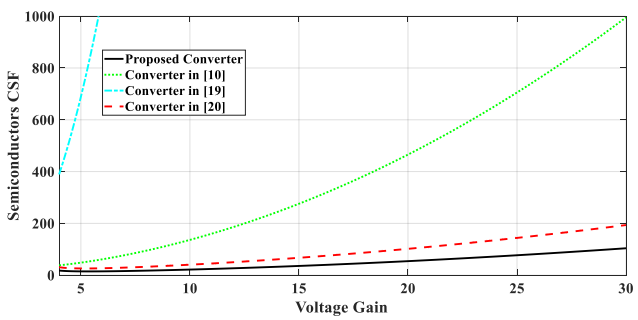

Fig. 8. Semiconductors CSF of proposed converter and structures in [10], [19] & [20]. n=2

TABLE 1 COMPARISON OF PRESENTED STRUCTURE WITH SOME HIGH GAIN DC-DC CONVERTERS PRESENTED BEFORE

Ref.	Number of Components					S.S	Low Input Current Ripple	Voltage Stress on Switch(es)	Voltage Gain	$\sum V_D$
	D	S	C	I/CI	T					
P.C	3	1	4	1/1[2W]	10	YES	YES	$\frac{M+1}{n+2}V_{in}$	$\frac{n+1+D}{1-D}$	$\left(2M-\frac{M+1}{n+1}\right)V_{in}$
[5]	4	1	3	1/1[2W]	10	NO	NO	$\frac{M}{D+1}V_{in}$	$\frac{1+nD}{1-D}(1+D)$	$\frac{4M}{D+1}V_{in}$
[8]	3	1	4	1/1[2W]	10	NO	YES	$\frac{M(n-1)}{2n-1}V_{in}$	$\frac{2n-1}{(n-1)(1-D)}$	$\frac{M(3n-1)}{2n-1}V_{in}$
[9]	3	2	3	2/0	10	NO	NO	MV_{in}	$\frac{1+D}{D(1-D)}$	$\frac{3D+1}{D(1-D)}V_{in}$
[10]	3	1	4	2/0	10	NO	YES	$\frac{M}{2}V_{in}$	$\frac{2}{1-D}$	$1.5MV_{in}$
[11]	2	1	3	1/1[2W]	8	NO	YES	$\frac{n+M}{n+1}V_{in}$	$\frac{nD+1}{1-D}$	$\left(\frac{M+n}{n+1}\right)\left(3+\frac{n(M-1)}{M+n}\right)V_{in}$
[12]	3	1	4	1/1[2W]	10	YES	YES	$\frac{M}{n+1}V_{in}$	$\frac{n+1}{1-D}$	$\frac{M(2n+1)}{n+1}V_I$
[16]	2	2	3	3/0	10	YES	NO	$\frac{M+3}{2}V_{in}$	$\frac{1+3D}{1-D}$	$(M+3)V_{in}$
[17]	3	2	3	2/0	10	NO	YES	$\left(\frac{M(1-D)}{2-D}+M-\frac{1}{1-D}\right)V_{in}$	$\frac{2-D_1}{(1-D_1)(1-D_2)}$	$\left(\frac{2M(1-D)}{2-D}+M-\frac{2}{1-D}\right)V_{in}$
[19]	3	1	3	3/0	10	NO	YES	$\frac{3M-1}{2}V_{in}$	$\frac{1}{1-2D}$	$\left(2M-1+\frac{2M}{M+1}\right)V_{in}$
[20]	3	1	3	0/1[3W]	8	YES	NO	$\frac{M+n_2-n_1}{1+n_2}V_{in}$	$\frac{1+n_1+(n_2-n_1)D}{1-D}$	$\frac{(M+n_2-n_1)(3+n_1+n_2)}{1+n_2}V_{in}$
[21]	3	1	3	0/1[2W]	8	NO	NO	$\frac{M}{n+1}V_{in}$	$\frac{n+1}{1-D}$	$2MV_{in}$

D: Diode, S: Switch, C: Capacitor, I: Inductor, CI: Coupled Inductor, S.S: Soft Switching, P.C: Proposed Converter

$$i_{D1}=i_{D1,peak}\left(1-\frac{t}{d_4T_S}\right)\quad DT_S\le t\le(D+d_4)T_S \tag{35}$$

$$i_{D2}=i_{D2,peak}\begin{cases}\dfrac{t}{d_4T_S} & DT_S\le t<(D+d_4)T_S\\ 1 & (D+d_4)T_S\le t<T_S\end{cases} \tag{36}$$

$$i_{D3}=i_{D3,peak}\left(\frac{t}{DT_S}\right)\quad 0\le t\le DT_S \tag{37}$$

By utilizing (35), (36), and (37), the RMS values of currents flowing through diodes could be achieved as:

$$I_{D1,rms}=\sqrt{\frac{d_4}{3}\left(\frac{2n+(2-n)D}{D(1-D)}\right)}I_O \tag{38}$$

$$I_{D2,rms}=\sqrt{1-D-\frac{4}{3M_{CCM}}\left(\frac{M_{CCM}}{n+D-1}\right)}I_O \tag{39}$$

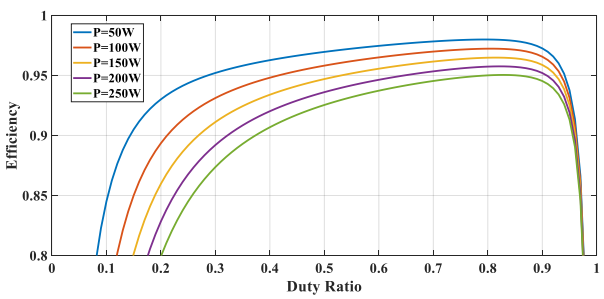

Fig. 9. Efficiency of designed structure versus duty ratio

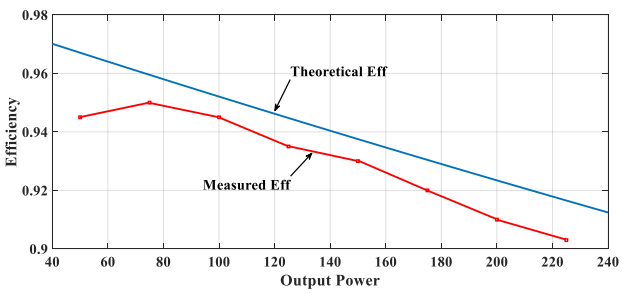

Fig. 10. Theoretical and measured efficiency of presented structure versus output power. n=2, r_C=r_D=10mΩ, r_L=20mΩ, R_{DS_ON}=40mΩ, C_S=600pF, V_F=1V, f_S=30kHz.

$$I_{D3,rms} = \frac{2I_O}{\sqrt{3D}} \tag{40}$$

Assuming that all diodes are similar, power dissipations in diodes could be formulated by:

$$P_D^{loss} = r_D \sum_{k=1}^{3} I_{Dk,rms}^2 + 3V_F I_O \tag{41}$$

Where $I_{Dk,rms}$ represents the RMS value of each diode current, and r_D and V_F are the conduction resistance and voltage drop of each diode, respectively. The RMS values of capacitor and inductor currents could be given by:

$$I_{C1,rms} = I_O \sqrt{\left(\frac{M_{CCM}D+2}{3}\right)\left(\frac{2n+(2-n)D}{D(1-D)}\right)^2 + M_{CCM}^2} \tag{42}$$

$$I_{C2,rms} = I_O \sqrt{\left(\frac{D}{3}\right)\left(\frac{2n+2-nD}{D(1-D)}\right)^2 + M_{CCM}^2} \tag{43}$$

$$I_{C3,rms} = I_O \sqrt{\left(1-D-\frac{4}{3M_{CCM}}\right)\left(\frac{M_{CCM}}{n+D-1}\right)^2 + \frac{4}{3D}} \tag{44}$$

$$I_{CO,rms} = I_O \sqrt{1+\frac{4}{3D}} \tag{45}$$

The RMS values of currents flowing through input inductor L_{in} and CI could be given as follows.

$$I_{Lin,rms} = MI_O \tag{46}$$

$$I_{Lk,rms} = I_O \sqrt{\left(\frac{M_{CCM}D+2}{3}\right)\left(\frac{2n+(2-n)D}{D(1-D)}\right)^2} + I_O \sqrt{\left(1-D-\frac{4}{3M_{CCM}}\right)\left(\frac{M_{CCM}}{n+D-1}\right)^2 + M_{CCM}^2} \tag{47}$$

According to [25], power dissipations in each component and total power losses in the presented converter could be calculated. Regarding [25], the efficiency of the proposed structure could be calculated as follows.

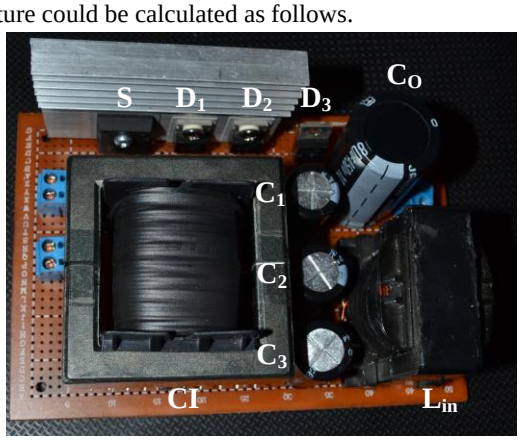

Fig. 11. Experimental prototype of presented structure

$$\eta = \frac{R_L}{2(r_L+r_C)M_{CCM}^2 + \frac{A_1}{3}\left(\frac{2n+(2-n)D}{D(1-D)}\right) + \frac{4}{3D}(r_D+3r_C) + \frac{R_L}{A_2(r_C+r_L+r_D) + \left(1+\frac{3V_F}{V_O}\right)R_L + f_S C_S \left(\frac{DR_L}{n+1+D}\right)^2 + r_C}} \tag{48}$$

Where r_L, r_C, and R_L represent the resistance of each inductor, the ESR of each capacitor, and the output load, respectively. Moreover, A_1 and A_2 are coefficients given by the following.

$$A_1 = D\left(R_{DS\_ON} + 2r_C + r_L\right) + \frac{2}{M_{CCM}}\left(r_D + r_C + r_L\right) \tag{49}$$

$$A_2 = \left(1-D-\frac{4}{3M_{CCM}}\right)\left(\frac{M_{CCM}}{n+D-1}\right)^2 \tag{50}$$

The theoretical efficiency of the designed topology versus duty ratio for some output power is shown in Fig. 9. As shown in this figure, the efficiency of the presented structure is more than 93% for duty ratios of more than 0.5 and output power up to 250 W. As the duty ratio increases, the efficiency of the structure gets higher as well. This trend continues for duty ratios less than 0.84.

In Fig. 10, the measured and calculated efficiency of the presented topology has been depicted. According to this figure, the converter has a maximum efficiency of 95% at the output power of 75 W.

VI. Experimental Results

To confirm the practicability of the proposed converter and theoretical analysis of the presented configuration, a 200-W converter operating at a switching frequency of 30 kHz is implemented. Fig. 11 shows the laboratory prototype of the presented structure. Different components of the converter are illustrated in this figure. Meanwhile, the specifications of the proposed prototype are listed in Table 2. As mentioned in this table, the winding turns ratio of CI is 2. Meanwhile, the duty cycle of the main switch is chosen to be 0.65. Thanks to the low voltage across switch S, a low $R_{DS\text{-}ON}$ MOSFET switch IRFP260 is selected. Furthermore, voltage and current waveforms of components are obtained and illustrated in Fig. 12. Comparing waveforms in Fig. 4 and Fig. 12 proves that the analytical and experimental results are the same. Fig. 12(a)

TABLE 2 CIRCUIT PARAMETERS OF THE PROTOTYPE

Specifications	Values
Input voltage (V_{in})	20 V
Output voltage (V_O)	200 V
Output Power (P_{out})	200 W
Capacitors (C_1-C_3)	47 µF
Output capacitor (C_O)	180 µF
Input inductor (L_{in})	320 µH
Magnetizing inductor of CI (L_m)	100 µH
Turns ratio of CI (n)	2
Switching frequency (f_S)	30 kHz
Power switch (S)	IRFP260
Diodes (D_1-D_3)	MUR1560

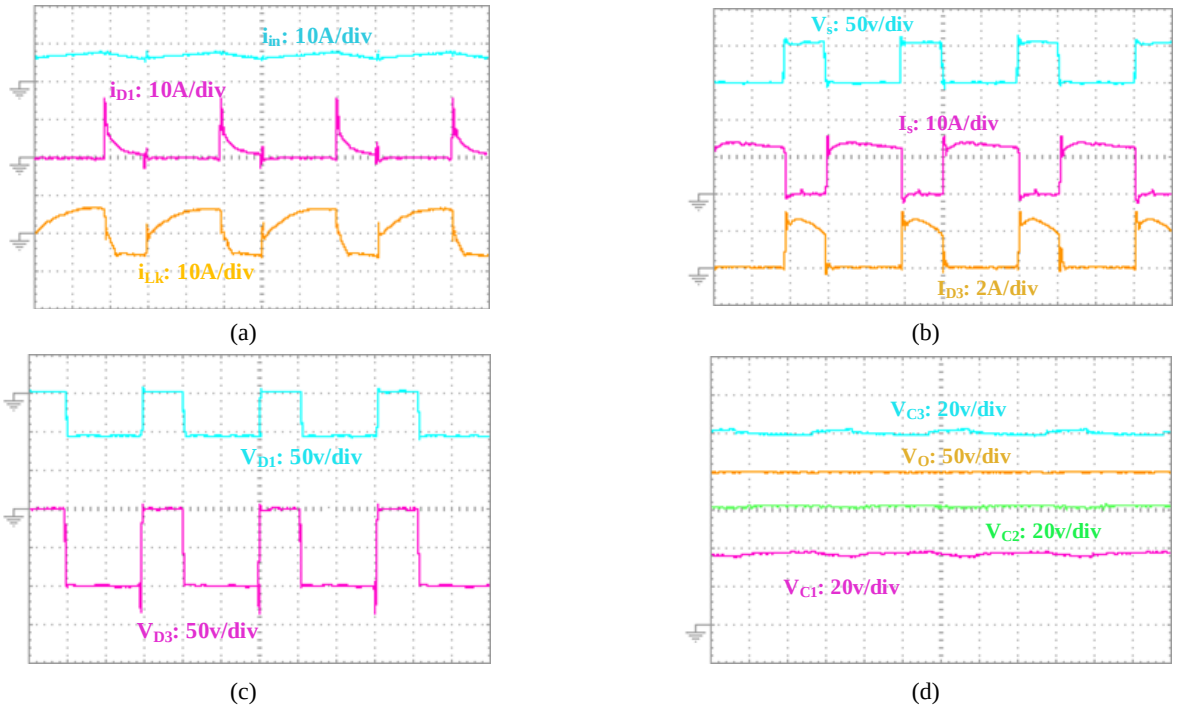

Fig. 12. Experimental result of prototype structure. (a) input current i_{in}, currents of diode D_1 and the primary side of CI, (b) voltage and currents of switch S and diode D_3, (c) voltage of diodes D_1 and D_3, and (d) voltage of capacitors and output voltage V_O.

represents input current and currents flowing through diode D_1 and CI. As depicted in this figure, the input current ripple is relatively low. Hence, the presented converter is a promising solution for PV systems. According to this figure, diode D_1 is turned off under ZCS conditions. Fig. 12(b) shows the voltage across switch S along with switch S and diode D3 currents. According to this figure, the voltage stress of switch S is clamped to the voltage of capacitor C_2. Moreover, it is shown that diode D_3 is turned on and off under ZCS conditions. Fig. 12(c) illustrates voltage stresses on diodes D_1 and D_3. Meanwhile, voltages of capacitors C_1, C_2, C_3 along with output voltage is depicted in Fig. 12(d).

VII. Conclusions

In this paper, a non-isolated high step-up SEPIC-based DC-DC converter has been presented and studied. The proposed converter has outstanding merits such as continuous input current and high voltage conversion ratio that make the structure a promising and functional solution for PV applications. Meanwhile, the stored energy of the leakage inductance of the CI has been recycled by a passive voltage clamp. Hence, power losses of the presented topology and voltage stress on the switch have been reduced. As a result, a switch with low on-resistance ($R_{DS\text{-}ON}$) has been employed. Since all diodes of the presented converter are biased reversely under ZCS conditions, their reverse recovery problems have been eliminated. Moreover, Thanks to the low voltage across switch S, the steady-state analysis of the proposed converter has been discussed and the design procedures of different components have been carried out. Specifications of the presented converter and some other structures presented before have been compared through various methods. The comparison has proved the advantages of the proposed converter over them. Furthermore, the efficiency analysis of the converter has been studied thoroughly and results have been depicted. In the end, experimental results have been added to validate the feasibility of the proposed structure. The results have confirmed the practicability of the proposed converter for PV applications.

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