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GPS synchronized digital current differential protection for transmission lines

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Abstract

This paper describes a newly developed digital current differential protection for transmission lines. The proposed protection is different from existing ones in two aspects: one is using GPS time information to implement synchronized sampling at all terminals of the protected line. Another is the application of new differential algorithm based on fault component instantaneous value. To evaluate the performance of the protection, both the EMTP simulation study on the new algorithm and the dynamic simulation test on the prototype of the protection are conducted. The test results have proved the correctness of the new algorithm and the feasibility of the protection scheme. This paper starts with brief introduction to overall scheme of the protection, then focuses on describing the principles of GPS based synchronized sampling and new differential algorithm. The simulation results are also presented.

Keywords: Current differential protection; Global positioning system; Synchronized sampling; Fault component

1. Introduction

The Global Positioning System (GPS) is a new generation of satellite based navigation, positioning and timing system of USA. The time transferred by GPS is highly synchronized to the Universal Co-ordinated Time (UTC) and can be easily received all over the world by using GPS receiver. Up to now, it has been the most precise and most extensive time synchronization source around the world. With the ability to provide time synchronization to 1 μs accuracy over a wide area as covered by a power system network, GPS has been an interesting subject for power system engineers since the beginning of 1990s. Now GPS has been applied in numbers of areas of power system.

Current differential protection based on Kirchoff's first law is a sample and reliable protective principle for any kinds of transmission lines. Traditional analogue design using metallic pilot wires as communication channel is susceptible to electrical interference and hence becomes less applied. Power line carrier channel tends to be used in phase comparison principle because of its limited bandwidth. Now, the microcomputer based digital current differential protection can overcome most of these problems by using digital communication link. Differing from analogue design, digital differential protection uses sampled current data, not the current waveforms varying with time, to make differential comparison. Thus, some form of synchronization must be provided in order to meet the requirement of the current differential principle. The synchronization ensures that the samples derived from all terminals of the protected line can be time aligned. This is the key technique for implementing this kind of protection.

To solve this sampling time alignment problem, most existing digital differential protections adopt techniques that measure the delay of communication channel and compensate for this delay. These techniques have some drawbacks as described in reference [6]. In fact, the most excellent way is to precisely synchronize the samplings at all terminals with the help of external common timing reference. Today GPS provides us a very good chance to reach the goal.

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As early as 1994, the authors of this paper first proposed the thought to utilize time information provided by GPS to carry out the synchronized sampling mentioned above [4]. After that, through several years of research work, a new type of GPS synchronized digital current differential protection has been developed. To reduce cost, the hardware of the protection is developed on the basis of distance relay. The PCM digital communication technique is adopted to make current data exchange between line terminals. To overcome some problems existing in traditional phasor differential algorithm, a new differential algorithm based on fault component instantaneous value is used for making tripping decision. Taking the advantages of fault component, the algorithm can significantly improve the protection's performance such as sensitivity, operating speed and the ability to tolerate arc resistance. Extensive simulation results have shown these advantages. The goal of this paper is to describe the features of the proposed protection, while the other parts that traditional ones also have are not reported.

2. Overall protection scheme

The overall block diagram of the proposed protection is shown in Fig. 1.

In this protection system, the GPS receivers are installed at each terminal of the line. At each terminal, the main CPU samples the local current signals under the control of synchronized sampling clock. The synchronized samples are processed and encoded according to the communication protocol. The local communication unit then transmits the encoded data (with time tag) to remote terminal and simultaneously receives data from remote terminal via a CCITT standard 64 kbps PCM channel (ether the dedicated fiber optical or multiplexed link). The trip decision is made by the main CPU through calculating and comparison according to the new differential algorithm. This protection is designed to operate in phase segregated mode.

3. Synchronized sampling technique

3.1. GPS receiver and its output signals

The configuration of GPS based synchronized sampling control unit is presented in Fig. 2. The GPS receiver used in this unit is commercial type receiving board with very small size. The receiver can receive signals transmitted from four to eight satellites at any time. Through processing to the received message, the receiver outputs two kinds of time signals. The first is called '1PPS' (one pulse per second) which is synchronized to UTC standard with 1 μs accuracy, and is available anywhere in the world. The second is a serial message, which contains UTC date and time information (year, month, date, hour, min and seconds) corresponding to the front edge of present 1PPS pulse.

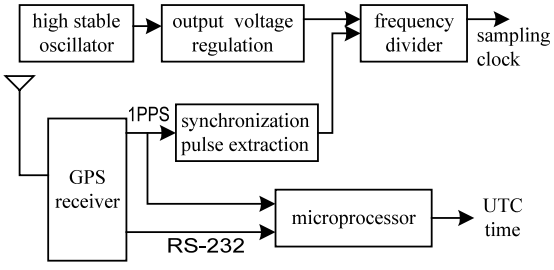


Fig. 2. Synchronized sampling control unit.

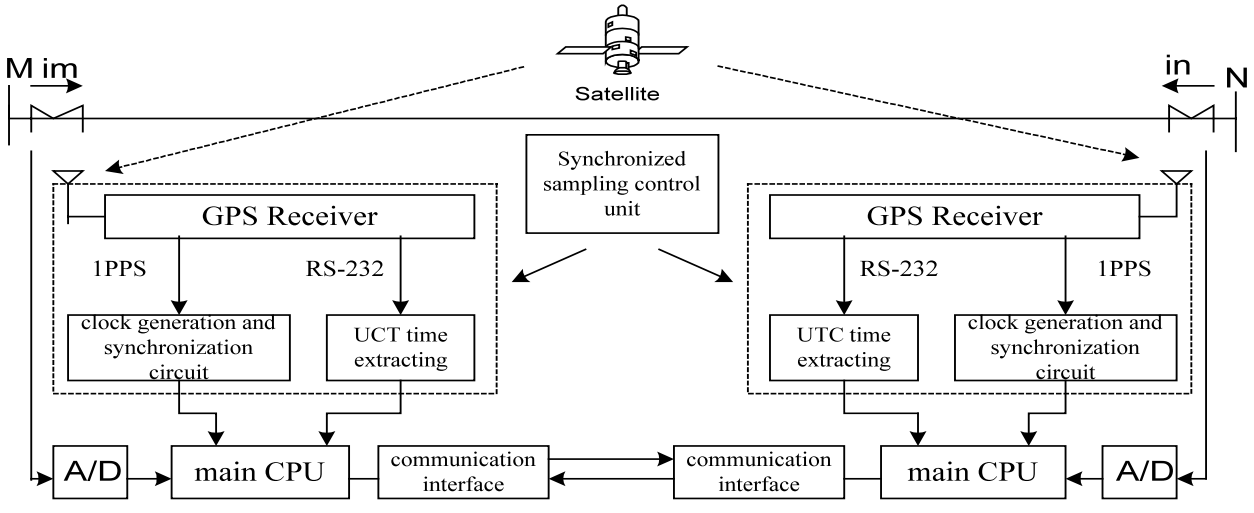


Fig. 1. Block diagram of GPS based current differential protection.

3.2. Implementation of synchronized sampling and test results

As shown in Fig. 2, the local high stable crystal oscillator produces high frequency signal. This signal is transformed into TTL voltage level at first, and then is synchronized one time per second by the rise edges of 1PPS. After that the synchronized signal is divided into lower frequency signal (such as 600 HZ) to be used as local sampling clock. Through above processing, the local sampling clock can keep running with 1 μs accuracy of synchronization to GPS time reference. Since the GPS receivers installed in line terminals are totally identical, the two sampling clocks separated in the line terminals are precisely synchronized by the GPS time reference, no matter how long the protected line is. The maximum error of synchronization is no more than 2 μs (0.036° in phase angle). Under the control of such local sampling clock, synchronized sampling between two terminals can be implemented. In addition, the microprocessor in Fig. 2 is used to extract UTC date and time (corresponding to 1PPS) from the serial message outputted by GPS receiver. The extracted time will be used to set 'time label' to sampled data.

To demonstrate the performance of the proposed synchronization method, a lot of sampling tests are carried out on a physical model of transmission line in power system laboratory. In this paper, three groups of typical sampling data records obtained from M and N terminal relays are given in Table 1. In this case, the sampling rate is 600 Hz, the sampled signal is phase A current. Each group contains 13 samples (one cycle). The full cycle Discrete Fourier Transform (DFT) algorithm is used to extract fundamental frequency component (FFC).

The results shown in Table 1 indicate that the proposed method can provide us with satisfactory accuracy of synchronization. The phase angle error is generally within 0.3°, the magnitude error is within 2%. While in traditional methods, these two kinds of errors are 1–4° and more than 3%, respectively [6].

In addition to the high synchronization accuracy, the most significant advantage of this proposed method is that synchronized sampling is performed independently at local terminal, while the previous communication and related algorithm for synchronization processing are not necessary. Thus the synchronized sampling between line terminals will not affected by any factors related to the communication channel, which make the operation of current differential relay more reliable. This method is suitable for any kind of transmission lines.

4. Protection algorithm

4.1. Problems with phasor differential algorithm

The phasor differential algorithm based on fundamental frequency current signal is widely used in digital current differential protection [1]. Its basic operating criteria is shown in Eqs. (1) and (2).

$$|\dot{I}_m + \dot{I}_n| \geq I_0$$

$$|\dot{I}_m + \dot{I}_n| \geq k(|\dot{I}_m| + |\dot{I}_n|) \quad (1)$$

Table 1
Synchronized sampling test records

Sampling Number	Group 1		Group 2		Group 3	
	Samples (terminal M)	Samples (terminal N)	Samples (terminal M)	Samples (terminal N)	Samples (terminal M)	Samples (terminal N)
1	3.22	3.38	−10.17	−10.16	−2.03	−2.03
2	6.95	7.28	−4.41	−4.23	−8.14	−8.13
3	8.65	8.80	2.20	2.03	−12.21	−12.19
4	7.29	7.62	8.48	8.12	−12.89	−13.04
5	4.07	4.06	12.72	12.53	−9.84	−9.99
6	0.33	0.33	13.40	13.04	−4.07	−4.06
7	−3.56	−3.38	10.17	9.82	2.20	2.54
8	−7.12	−7.11	4.41	4.06	8.31	8.63
9	−8.65	−8.63	−2.20	−2.37	12.55	12.53
10	−7.29	−7.11	−8.48	−8.47	12.89	13.04
11	−3.73	−3.72	−12.72	−12.53	9.33	9.65
12	0.00	0.00	−13.23	−13.04	3.56	3.72
13	3.73	3.89	−9.67	−9.65	−2.71	−2.71
FFC	$8.26^{A} \angle 28.56°$	$8.34^{A} \angle 28.67°$	$13.37^{A} \angle -49.86°$	$13.10^{A} \angle -49.55°$	$12.89^{A} \angle 191.19°$	$13.04^{A} \angle 191.22°$
Phase angle error	0.11°		0.31°		0.03°	
Magnitude error (%)	1.4		2		1.2	

$$|\dot{I}_m + \dot{I}_n| \geq I_0$$
$$|\dot{I}_m + \dot{I}_n| \geq k|\dot{I}_m - \dot{I}_n| \quad (2)$$

where, $\dot{I}_m$, $\dot{I}_n$ is the fundamental frequency current phasors at line terminal M and N, respectively; I_0 is the threshold; K is the restraint coefficient.

Under normal condition, the current phasors involved in the algorithm represent load currents. When a fault occurs, they will be the post-fault fundamental frequency currents including load. Generally, this algorithm can provide adequate sensitivity for internal faults and stability for external faults. But there are two problems existing in the algorithm [5].

1) Under internal fault conditions, the existence of load current as through current will increase the restraint quantity, and hence lower the sensitivity of the protection. This may cause no trip for the case of internal high resistance faults with heavy load in the protected line or with load out of the line.
2) To obtain current phasors used in the algorithm, the full cycle DFT algorithm is often adopted to estimate FFC from local current samples. Therefore, the tripping time for internal faults is generally more than 20 ms (such as LFCB102, GEC measurements and REL-561, ABB), which means the operating speed for this kind of protection is slow.

4.2. New differential algorithm

According to the superposition theorem, the post-fault current (called total current) can be decomposed into normal load current and fault introduced current (called fault component). The fault component can be used in protective relaying due to its interior features.

A new differential algorithm, which is based on fault component instantaneous value, is proposed and adopted in this protection. The phase segregated operating criteria for two terminal lines is given by the formula below:

$$|\Delta i_m + \Delta i_n| \geq k|\Delta i_m - \Delta i_n| + i_0 \quad (3)$$

where: Δi_m, Δi_n is the fault component instantaneous value of current at line terminal M and N, respectively. k is the restraint coefficient (less than 1); i_0 is the threshold.

Letting:

$$i_d = \Delta i_m + \Delta i_n$$

$$i_b = \Delta i_m - \Delta i_n$$

$$i_{op} = |i_d|$$

$$i_{re} = k|i_b| + i_0$$

Eq. (3) becomes:

$$|i_d| \geq k|i_b| + i_0 \quad (4)$$

that is

$$i_{op} \geq i_{re} \quad (5)$$

where i_d is the fault component differential current; i_b is the fault component bias current; i_{op} is the operating quantity; i_{re} is the restraint quantity.

In this criteria, i_0 is set to against the non-zero output (or noise) of the differential current in steady state condition. The principal sources resulting in non-zero output are analogue circuit noise, harmonics generated by the CT, A/D conversion error and the change of system frequency, etc. Item $k|i_b|$ is used to ensure sufficient stability for external faults, especially for the situation of CT saturation caused by external faults. However, the setting for k must also ensure adequate sensitivity for internal faults [2].

Under fault conditions, since the values of both Δi_m and Δi_n are variable with time, the operating quantity and restraint quantity in Eq. (5) do not have fixed relationship in magnitude during transient process. This indicates that it is necessary to make comparison more times by using different samples when Eq. (5) is used to make trip decision. To achieve a high speed response to internal faults and ensure sufficient stability to external faults, a tripping logic is designed as follows:

Suppose sampling rate is 12 points per fundamental frequency cycle, if there are four samples (successive or not) meeting Eq. (5) among the first nine post-fault samples, and the zero-cross times of i_d is not more than 2 during the judgment process, then give the tripping command.

This tripping logic is established according to the following analysis:

4.2.1. The selection for number '4'

Consider a two-terminal line with internal fault on it and do calculation depending on following conditions:

- In Eq. (3), suppose Δi_m and Δi_n contain only FFC represented by $\Delta \dot{I}_m$ and $\Delta \dot{I}_n$, respectively.
- The phase angle difference between $\Delta \dot{I}_m$ and $\Delta \dot{I}_n$ is taken as 25° (the largest possible value).
- The amplitude ratio of $\Delta \dot{I}_m$ and $\Delta \dot{I}_n$ is taken as 0.5, 1 and 1.5, respectively.
- The coefficient k in Eq. (3) is taken as 1, and i_0 is ignored.

Under above unfavorable conditions, the calculation results show that among successive six post-fault samples (half cycle), there are at least four samples which meet Eq. (3).

Suppose Δi_m and Δi_n contain fault induced d.c. components which is represented by Δi_{dcm} and Δi_{dcn},

respectively. Since Δi_{dcm} and Δi_{dcn} have same polarity with internal faults, their existing will make Eq. (3) more easily to be met.

4.2.2. The selection for number '9'

In Eq. (3), since the setting value for i_0 is small, it can not cause obvious effect on relay's sensitivity for general internal faults. But to some high resistance internal faults, the influence will become significant due to the drastic decreasing of fault component. This may cause that the number of samples meeting Eq. (3) during post-fault half cycle is less than 4. In addition, Eq. (3) may not work properly with the samples near zero-cross points of i_d. Therefore, to ensure relay's operation reliability to various internal faults, the time interval for judgement in tripping logic is increased to 3/4 cycle (contain nine samples) from half cycle.

4.2.3. Why consider 'zero-cross times of i_d'

According to the conclusions drawn from transient characteristic analysis for fault component [5], we know that under external fault conditions, the differential current (i_d) is not zero, but a certain amount of high frequency components. This induces two kinds of phenomena:

- During one fundamental frequency cycle, there are more than two zero-cross points in i_d waveform.
- At some instants during first post-fault cycle, the operating quantity (i_{op}) will larger than the restraint quantity (i_{re}).

To ensure relay's stability to external faults, the checking procedure for zero-cross of i_d is included in tripping logic. This procedure can also prevent relay from mis-operation during line energizing.

4.3. Extraction of fault component

There are several methods to extract fault component from post-fault current. This protection adopts following digital filtering algorithm.

$$\Delta i(k) = i(k) - i(k-N) \tag{6}$$

where: $i(k)$ is the present sample; $i(k-N)$ is the sample leading $i(k)$ by N samples; N is the total number of samples in one period of fundamental frequency; k is the sampling serial number, take 1, 2, 3...

Under steady state condition, the output of the filter will keep zero (for fundamental frequency). When a fault occurs, the output will represent the real fault component including d.c. component and various harmonic components during the first post-fault cycle. After that, the output will not reflect the actual fault component and gradually decline and become zero finally. So this extracting algorithm requires that the tripping decision must be made within one period of time (20 ms) after the inception of a fault. This will not affect the tripping logic discussed above.

4.4. Algorithm evaluation

Evaluation for the proposed algorithm is performed using EMTP simulation package. The simulation model is a typical 500 kV system, as shown in Fig. 3. To make a complete evaluation to the algorithm, a variety of fault conditions are simulated. In these simulations, the settings of k and i_0 in Eq. (3) are 0.5 and half of load current, respectively. The CT ratio is taken as 1200/5. The tripping logic is used as operating criteria in this evaluation. Here present some typical simulation results.

4.5. Internal faults responses

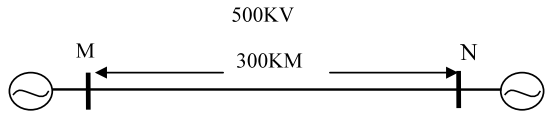
The typical simulation results for internal faults are shown in Figs. 4–6 and Table 2.

Fig. 4 shows a response attained for phase A to earth fault at 100 km from busbar M. From this figure we can see clearly that the operating quantity significantly exceeds the restraint quantity (Fig. 4(c)), which causes the fast tripping response. The tripping time is about 9 ms.

Table 2 indicates that the proposed algorithm has strong ability to tolerate fault resistance. Load current has no effect on this ability due to the using of fault component.

Fig. 5 shows the tripping times for internal faults with same fault type but different locations only have a small change (around 10 ms). This can be explained as follows: when fault location changes, the magnitudes of Δi_m and Δi_n will change, but the phase relationship between them will almost not change due to the features of fault component, which keeps the tripping time stable.

Fig. 6 shows the tripping time for internal fault will increase with the increasing of fault resistance. Following is the reason. With the increasing of fault resistance



System parameters:

Z_m1 =1.05+j43.18Ω Z_n1 = 1.06+44.92Ω

Z_m0 = j29.09Ω Z_n0 = j37.47Ω

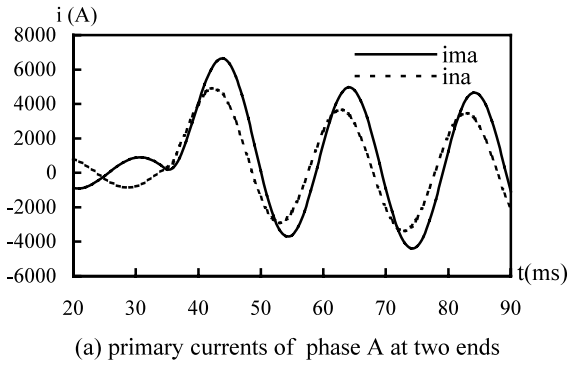
Line parameters:

R1 = 0.0208Ω/km R0 = 0.1148Ω/km

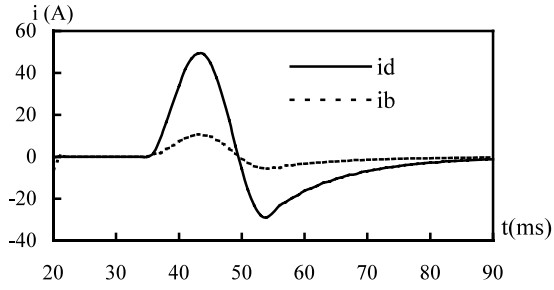
L1 = 0.8984mh/km L0 =2.2886mh/km

C1 = 0.0129μf/km C0 = 0.0052μf/km

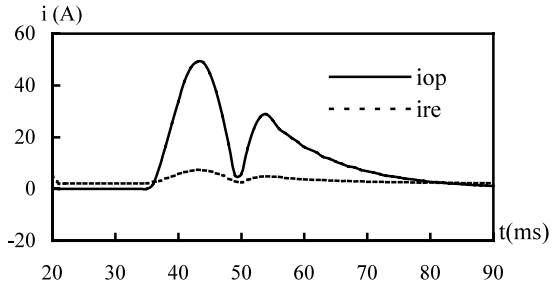
Fig. 3. Model system for algorithm evaluation.



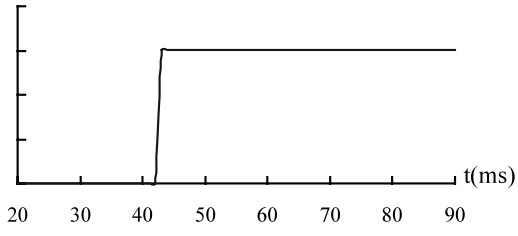
(a) primary currents of phase A at two ends



(b) differential current and bias current



(c) operating quantity and restraint quantity



(d) tripping signal

Fig. 4. Response for phase A to earth fault at 100 km from busbar M.

at fault location, the magnitudes of Δi_m and Δi_n will decrease, which cause the magnitude of i_d to be comparable with load current. At this time, the threshold (i_0) whose setting is part of the load current will play an obvious rule in restraint quantity, and make the restraint quantity exceed the operating quantity within a certain area near zero cross points of i_d. Therefore, to

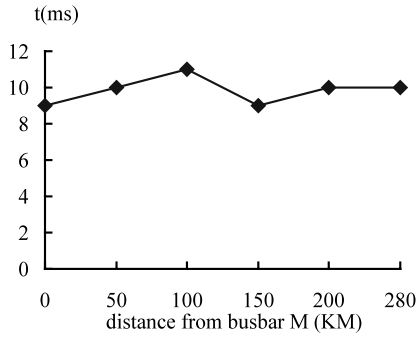


Fig. 5. Tripping time comparison for B–C phase faults ($R_f = 10\ \Omega$) at different positions.

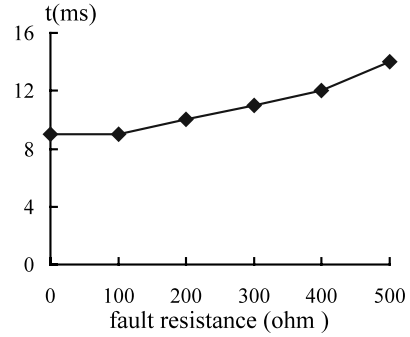


Fig. 6. Tripping time comparison for phase A to earth faults with different fault resistances.

Table 2
Maximum tolerated fault resistances comparison for different loads and different fault inception angles

Fault condition		Phase A to earth fault at 200 km from busbar M		
Primary load current		0	900 A	1700 A
Maximum tolerated fault resistance	$\varphi_{Ua} = 90°$	500 Ω	500 Ω	500 Ω
	$\varphi_{Ua} = 0°$	650 Ω	650 Ω	650 Ω

φ_{Ua}, fault inception angle of phase A voltage

get four samples meeting Eq. (5) will spend longer time than before, which causes the tripping time to be more than half cycle. This result also implies that the threshold is the main factor limiting fault resistance.

Above results indicate that the proposed algorithm can provide high sensitivity, fast tripping speed and strong ability to tolerate fault resistance for internal faults. Load current, fault types and fault location do not affect the performance of the algorithm.

4.6. External faults responses

To investigate the responses to external faults, a large number of external fault conditions are simulated. A

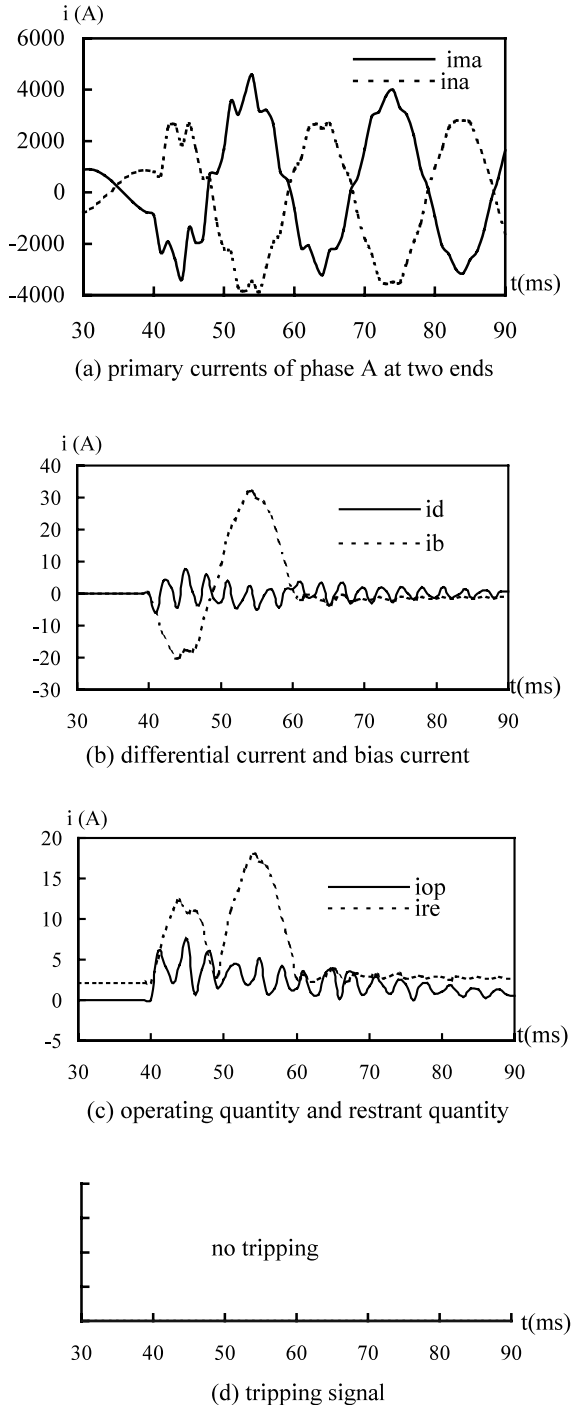


Fig. 7. Response for phase A to earth fault at busbar M.

typical external fault response is given in Fig. 7. From this response we can see two facts:

- The differential current (i_d) is mainly consist of high frequency components (see Fig. 7(b)), which is consistent with theoretical analysis.
- At some sampling points, especially near the zero cross points of i_{re}, Eq. (5) can be met (Fig. 7(c)), but the tripping logic can prevent the relay from tripping.

Above results indicate that the restraint effect of bias current in cooperation with tripping logic can definitely ensure relay's stability under external fault conditions.

4.7. Other simulations

In addition to above simulations, the algorithm is also investigated under some special conditions such as CT saturation, one terminal supply, line energizing, etc. In these situations, the algorithm, incorporating with some specially designed techniques, is able to provide satisfactory protective performance.

5. Dynamic simulation test

To demonstrate the operating performance of the proposed protection, the developed prototype is tested on a 500 kV, 290 km system model in the Dynamic Simulation Laboratory of Tianjin University. A large number of fault types were tested, including internal faults (with low and high resistances), external faults, switch on to healthy line, switch on to fault, etc. The test results are consistent with the EMTP simulation results. The average tripping time is 13 ms (including the operating time of output relay). The maximum tolerated fault resistance for single phase to ground fault is 400 Ω.

6. Reliability

Reliability is one of the basic requirements for designing relays. When GPS is involved in relays, people will ask if the reliability can be assured or if the GPS is reliable. According to the descriptions about GPS's design, maintenance and importance in reference [3], we can say the GPS's reliability is nearly ideal and believable.

In this protection, to provide against eventualities, such as the sudden interruption of GPS signal, the 1PPS signal of GPS receiver is always monitored. When the signal is interrupted or incorrect within a setting time, a special alarm signal will be sent, and the synchronized sampling method will be changed into traditional version.

7. Conclusion

A GPS based digital current differential protection is presented in the paper. In this protection, the problem of synchronized sampling is perfectly solved by using GPS

time information. This novel synchronization method is accurate, reliable and unnecessary for communication between line terminals. The newly proposed differential algorithm based on fault component has the features of high sensitivity, strong ability to tolerate fault resistance and fast operating speed, and hence can be used to substitute for conventional phasor differential algorithm. The EMTP simulation and dynamic simulation test results have shown the high performance of the new protection.

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