Analysis and Experimentation on a New High Power Factor Off-Line LED Driver Based on Interleaved Integrated Buck Flyback Converter

Guirguis Z. Abdelmessih, *Student Member, IEEE*, J. Marcos Alonso, *Senior Member, IEEE*, and Wen-Tien Tsai

***Abstract*—This paper presents a high power factor (PF), low total harmonic distortion (THD) light-emitting diode (LED) driver with dimming capability. In addition, the proposed technique ensures a high PF and low THD at any dimming level. The driver is implemented by using an interleaved capacitor, which is placed between the rectifier and the integrated buck flyback converter (IBFC). In this way, the line current conduction angle is increased, which in return increases the PF and decreases the THD. The operation of the proposed converter ensures that one diode of the conventional IBFC will not conduct, so that it can be removed. Moreover, owing to the continuous power flow, the proposed technique makes a significant reduction of the converter output ripple. The paper presents a prototype of the proposed converter supplying an LED luminaire of 37 V/ 0.67 A. The prototype shows a high PF of 0.997, small THD of 2.5%, output current ripple of 6%, and an efficiency of 80%.**

***Index Terms*—Current shaper, integrated buck-flyback converter, integrated converters, interleaved capacitor, light-emitting diode (LED) drivers, power factor corrector, total harmonic distortion (THD) optimization.**

NOMENCLATURE

v_L	Voltage across the buck inductor.
$v_{\mathrm{AC}_{\mathrm{Bridge}}}$	Voltage across the bridge terminals.
V_B	Bulk capacitor voltage.
V_{int}	Voltage across the interleaved capacitor.
$i_{B_{\mathrm{peak}}}$	Peak value of the buck inductor current.
L_B	Buck inductance.
f_s	Switching frequency.
D	Duty cycle.
$I_{\mathrm{Lm}_{\mathrm{peak}}}$	Peak value of the magnetizing inductance current.
L_m	Magnetizing inductance.
$i_{p_{\mathrm{peak}}}$	Peak value of the flyback primary current delivered to the interleaved winding.
N_i	Number of turns of interleaved winding.
N_p	Number of turns of primary winding.
n_i	Turn ratio of interleaved to primary windings.
$i_{F_{\mathrm{peak}}}$	Peak value of the total flyback current.
R_g	Equivalent resistance of the Buck converter.
$\langle i_g \rangle$	Average line current.
P_g	Average input power.
P_F	Flyback power.
P_{Out}	Output LED power.
V_O	Output voltage.
R	Equivalent resistance of the LED load.
N_s	Number of turns of secondary winding.
n_s	Turn ratio of secondary to primary windings.
T_s	Switching period.
f_{res}	Resonance frequency of the interleaved capacitor and the leakage inductance.
L_{k_i}	Total leakage inductance of the interleaved winding.

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I. INTRODUCTION

SINCE the 1960s when light-emitting-diodes (LEDs) were first developed [1], they have been replacing little by little the conventional sources of light. Nowadays, they have become the most popular lighting source in a wide variety of applications. This has been possible owing to their longer lifetime, as it is usually quoted as 25 000 to 50 000 h, as declared by the LED manufacturers and standard organizations [2]–[4]. In addition, they present a higher efficacy compared to other sources of lighting. As it is stated in [5], incandescent lamp efficacy ranges between 14 and 17 lm/W, fluorescent tubes' around 100 lm/W and high-pressure-sodium lamp's reaches 120 lm/W. However, the new LED generation will have an efficacy up to 250 lm/W even 300 lm/W as stated by [6]. Moreover, LEDs exhibit other outstanding features like small size, fast response, robustness, reliability, and color rendering index [7]–[12]. However, LEDs cannot be connected directly to the mains, due to their low internal impedance, thus they have to be driven through a current controlled supply [1], [5], [13]–[15].

In order to assure the advantages offered by LEDs, an electronic converter to drive the LEDs should adequately be designed to fulfill all required standards. Nowadays, fulfilling the IEC 61000-3-2 Class C [16] concerning the harmonic content of the input current is a must in the case of a luminary load

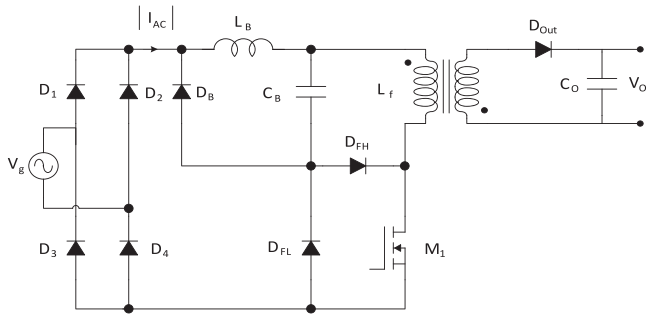

Fig. 1. Integrated Buck-Flyback Converter (IBFC).

[17]. Also, the power factor (PF) should be higher than the minimum value specified by the U.S. Energy Star program [18]. The conventional drivers proposed to fulfill these standards are two-stage LED drivers. The two-stage drivers are composed of a power-factor correction (PFC) stage and a constant-current-controlled dc/dc converter stage [19]. However, although two-stage converters show a significant good operation, they also have some drawbacks. The drawbacks are mainly higher number of components, lower efficiency, and higher number of controlled switches. This increases the converter complexity because additional circuitry is required for the driver, which means larger size and higher cost. In order to overcome these obstacles, many solutions have been proposed based on single-stage converters trying to fulfill the standards [20]. Other solutions keep the two-stage configuration proposing new topologies to aim at increasing the efficiency [21]. Also, a promising solution arises from the integrated converters, which are based on a two-stage topology that makes use of an integrated single switch. Thus, it will ensure lower switching losses and require only one driving circuit. These converters keep the good operation of the two-stage solution, as well as offer some advantages of the single-stage solution [9], [10], [22]–[26].

In this paper, the IBFC shown in Fig. 1 has been selected. This converter presents several good features as follows:

1) Fast output regulation;
2) Low voltage at the buck output;
3) Low current through the main switch.

However, the IBFC shows a limitation in the PF and the total harmonic distortion (THD), showing only good performance at full power. Thus, when dimming is applied so that the converter is not operating at rated power, the performance becomes worse. The proposed interleaved integrated buck-flyback converter (IIBFC) solves this issue as it ensures a good performance within all the operation range. The IIBFC is made by adding a capacitor between the diode bridge and the IBFC converter.

This paper presents a deep analysis and a further study of the IIBFC. The IIBFC is a single switch driver, which ensures an operation fulfilling the standards at any dimming ratio. The driver operates with a nearly unity PF and a significant low THD at any dimming ratio. The analysis proves that one diode of the conventional IBFC will not conduct and can be removed. Thus, the number of components is reduced. Moreover, the driver features isolation between the input and output. The control is simple as it is made using one single integrated circuit (IC). There is no extra sensor needed, so that a simple built-in voltage sensor is enough to regulate the output current from the primary side. Moreover, the driver features a lower ripple compared to the IBFC, which means that a lower capacitance is needed. In return, the driver has a more compact size and lower cost. The main drawback is being the lower efficiency shown by the driver. However, this is due to the fact that this is a low power application, the output power being only 25 W. Moreover, it is a low voltage, high current application, which decreases as well the efficiency. Furthermore, this is a stand-alone power supply. Thus, the efficiency is measured taking into account the control, switch driver, and sensor losses. However, according to the loss analysis on the IBFC made in [27], the efficiency could be increased by redesigning the converter, and without any additional modification of the control circuit. As shown in [27], the efficiency can be increased without adding any extra component, only by redesigning the values of the magnetic component and the turn ratio. This technique increased the efficiency of the IBFC from 82% to 89% [27]. Therefore, by repeating the study on the IIBFC, an improvement could be made so that its efficiency can become comparable to the state-of-the-art driver efficiency. Thus, this method can be adapted to the IIBFC for a further improvement in the efficiency.

This paper is a modified version of [28], as it presents a detailed analysis and a further study of the IIBFC. In the following, the main modifications of this version of the paper are summarized.

1) It gives guidance on how to select the optimal value of the interleaved capacitor.
2) It includes additional simulation results showing the effect of the interleaved capacitance on the flyback current.
3) It explains how the control of the output current can be done from the primary side. This allows the converter to keep the isolation between the input and output, avoiding the use of optocouplers for output current regulation.
4) It gives guidance on how to select a suitable value of the output capacitance.
5) It includes a comprehensive comparison with the up-to-date techniques found in the literature.

The rest of the paper is organized as follows. In Section II, the derivation of the IIBFC is illustrated. Section III shows the operational principles and the analysis of the IIBFC. Section III presents the average model of the IIBFC. The design procedure is illustrated in Section IV. The experimental results, as well as a comprehensive comparison with other up-to-date techniques, are shown in Section V. Finally, the conclusions of this paper are given in Section VI.

II. Derivation of the IIBFC

A. Conventional IBFC

The operation of the IBFC is equivalent to the operation of a buck and a flyback converters working in a cascade mode. The flyback converter function is to deliver the power to the output, while the buck converter duty is to improve the input power factor. The improvement of PF and THD is made by reducing the bulk capacitor voltage (V_B) as much as possible. Fig. 2 illustrates how the voltage level of the bulk capacitor will affect to the PF and THD, taking into account that the buck converter will only conduct when the input voltage is higher than the output voltage. Thus, a conduction angle for the ac main current appears, as illustrated in the bottom plot of Fig. 2. Therefore, decreasing the bulk voltage will increase the conduction angle, and in return, the PF and THD will improve.

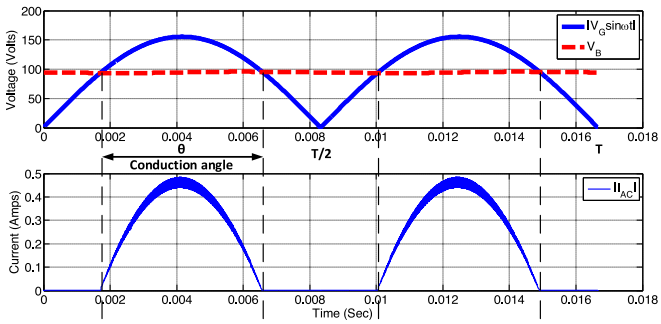

Fig. 2. Top: bridge voltage and bulk capacitor voltage. Bottom: current after the bridge.

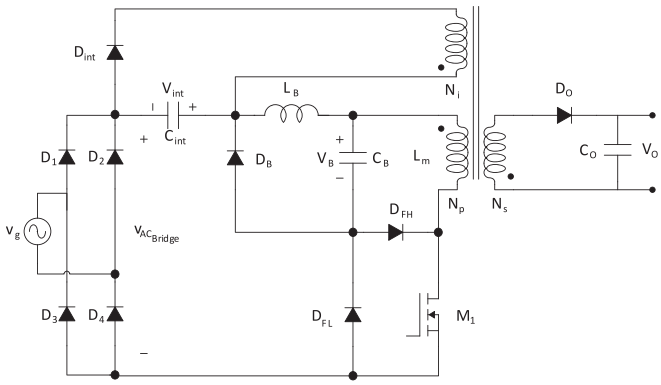

Fig. 3. Interleaved Integrated Buck-Flyback Converter schematic.

Ideally speaking, the more the bulk capacitor voltage is decreased, the more the PF and THD will improve. However, this is limited by two factors. First, if the voltage of the bulk capacitor is decreased, the voltage ratio between the bulk capacitor voltage and line voltage will decrease, and in return the ripple of the bulk capacitor voltage will increase [25]. Moreover, the increasing of the bulk capacitor voltage is done by increasing the buck inductance or by decreasing the magnetizing inductance of the flyback, and both options will be limited by the continuous conduction mode (CCM) limit.

In this type of converters, usually researchers investigate in order to find a tradeoff between fulfilling standards and limiting the size and the cost of the converter.

B. Interleaved IBFC (IIBFC)

The IIBFC shown in Fig. 3 solves all issues found in the conventional IBFC. The idea is simply to add a third winding to the flyback transformer, with the same polarity. This third winding goes to an interleaved capacitor that connects the ac bridge to the buck converter. There is a diode ensuring the direction of the current going to the interleaved capacitor and not in the reverse direction. The idea of the interleaved capacitor has previously been proposed in [29], aiming at a higher PF of a buck converter. When the interleaved capacitor technique is applied to the IBFC, it shows superior advantages, as it ensures a unity PF at any dimming ratio. As previously mentioned, and as shown in Fig. 2, the buck converter only conducts when the input voltage is higher than the bulk capacitor voltage. The presence of an interleaved capacitor makes a modification in the operation of the buck converter. In this case, the buck converter will conduct when the input voltage is higher than the bulk capacitor voltage minus the interleaved capacitor voltage (V_{int}), as the following:

$$v_L = v_{\text{AC}_{\text{Bridge}}} - (V_B - V_{\text{int}})\,. \tag{1}$$

As long as the turn ratio of the primary winding and the interleaved winding equals 1:1, the interleaved voltage will be equal to the bulk capacitor voltage. Therefore, the buck converter will conduct continuously, with a conduction angle of 180°.

III. Operational Principles of the Proposed IIBFC

A. Operation Principle

Since the proposed converter is a single switch converter, there are only two states, ON state and OFF state. However, the discontinuous conduction mode (DCM) operation of the buck and flyback splits the OFF state into three intervals. Figs. 4 and 5 illustrate the equivalent circuits, and the main current waveforms within a high-frequency switching period, respectively.

As aforementioned, each switching period can be split into four intervals, which can be explained as follows. The first interval occurs when the switch M_1 is switched ON, as shown in Fig. 4(a). There are two current loops. The buck converter loop represented by the current coming from the ac main and going into the buck converter. The role of this loop is to charge the buck capacitor, and meanwhile energize the buck inductance. The flyback loop is represented by the current coming from the buck capacitor and going into the transformer to energize the magnetizing inductance and also to deliver energy to the interleave winding. In the second interval, the switch M_1 is switched OFF, as shown in Fig. 4(b). Thus, the energy stored in the magnetizing inductance of the flyback transformer is delivered to the output to supply the LEDs and to charge the output capacitor. Thus, the energy stored in the buck inductance is going to the buck capacitor, through the buck diode. The third interval, shown in Fig. 4(c), is the same as the second interval, but the energy stored in the magnetizing inductance is finished. Thus, there is only current through the buck inductor going to the buck capacitor. The fourth interval, as shown in Fig. 4(d), is when there is no current in the entire converter. However, the current going to the LEDs is continuous in all intervals owing to the presence of the output capacitor.

Concerning the first interval, it is important to explain which of the two flyback diodes, D_{FH} and D_{FL}, will be conducting. Fig. 6 shows a simple magnetic model of the transformer during turn ON, which will be used in the analysis. Concerning the diodes, as shown in Fig. 7, the conduction will be determined according to the value of the flyback current and the buck current. As shown in Fig. 7(a), if the flyback current i_F is higher than the buck current i_B, then D_{FL} will conduct the difference between the two currents, while D_{FH} will not conduct. Fig. 7(b) shows the case where i_B is higher than i_f. In this case, the reverse will occur, D_{FH} will conduct the difference between the two currents, while D_{FL} will not conduct.

Another advantage shown by the IIBFC is the ripple reduction. Fig. 8 shows the simulation results of a comparison between the output voltage and current ripples of the conventional IBFC and the proposed technique. For better comparison, the values of the capacitors used in both converters are the same. As can be seen, the ripple is highly reduced in the proposed IIBFC. The voltage ripple is 5% in the case of the IBFC, and 1% in the case of the

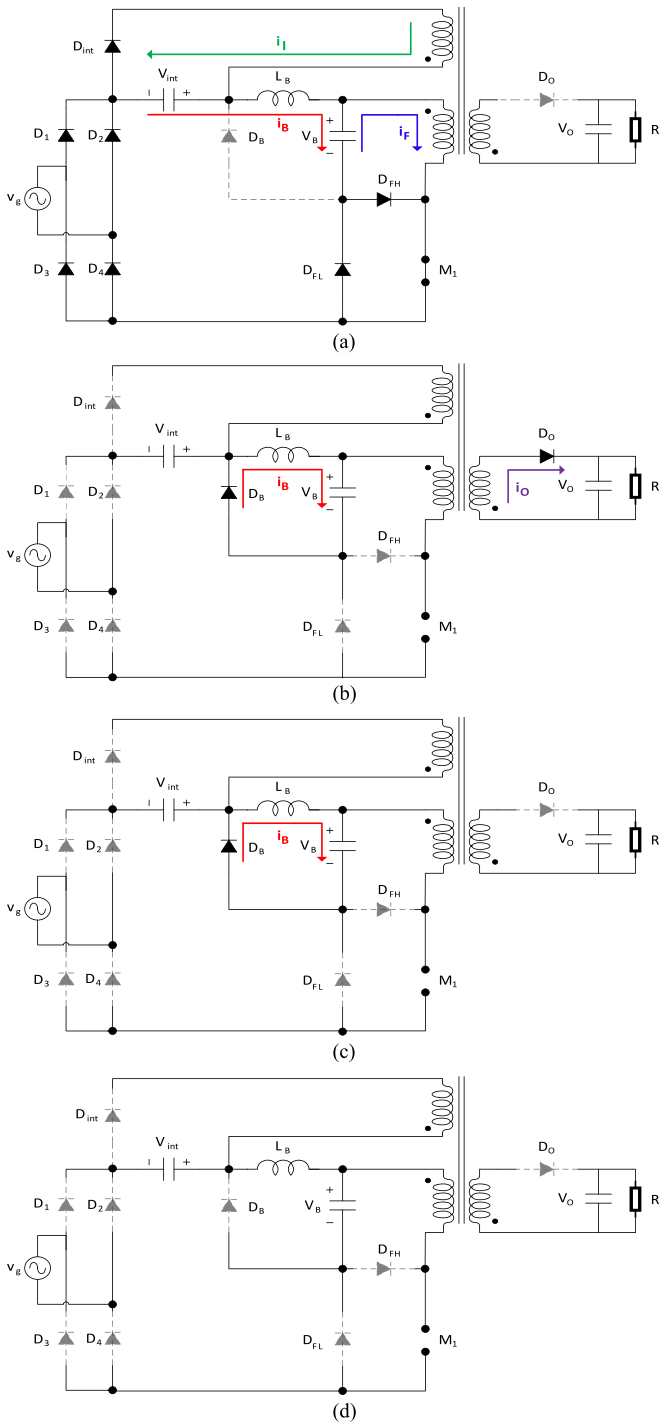

Fig. 4. Equivalent circuits of the IIBFC operating in DCM. (a) Interval I: 0 < t < DTs, (b) Interval II: DTs < t < t1, (c) Interval III: t1 < t < t2, (d) Interval IV: t2 < t < Ts.

IIBFC. The current ripple is 25% in the case of the IBFC, and 5% in the case of the IIBFC.

Fig. 9 shows the simulation results of the output current ripple for the IIBFC using different output capacitances, in order to choose the best capacitor that meets the requirements of a given application. Additionally, Table I shows the simulation results

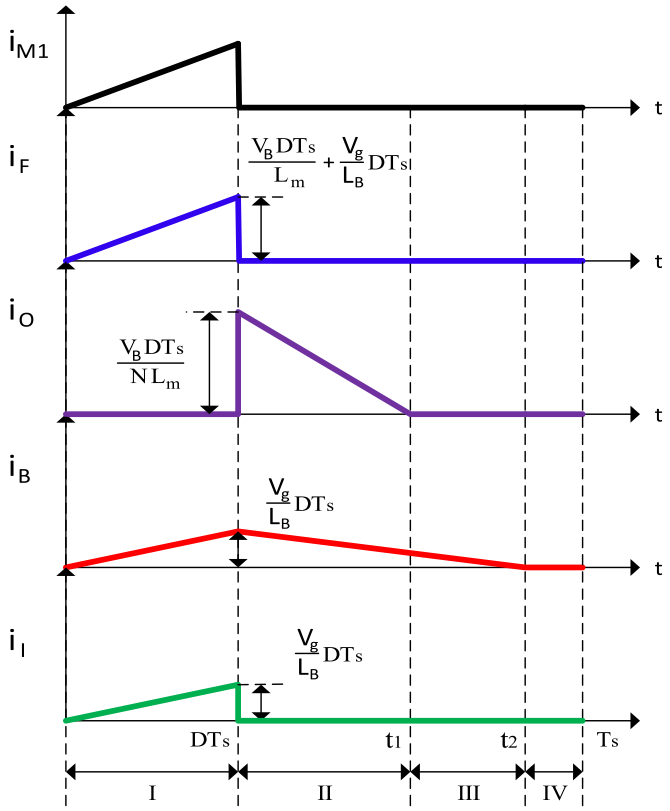

Fig. 5. Main current waveforms of the IIBFC operating in DCM, within a high frequency switching period around the peak line voltage.

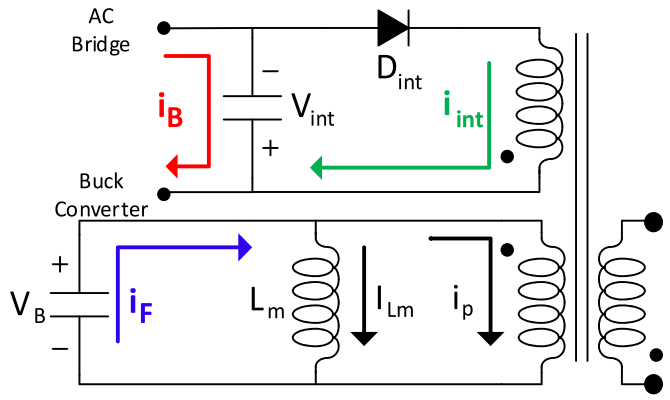

Fig. 6. A simple magnetic model of the flyback transformer and its currents during the turn-ON interval.

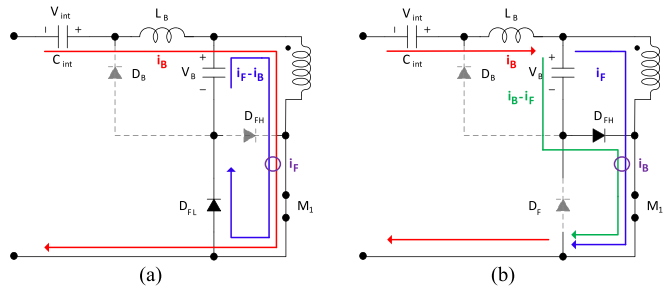

Fig. 7. Operation of the flyback diodes. (a) if $i_F > i_B$, (b) if $i_B > i_F$.

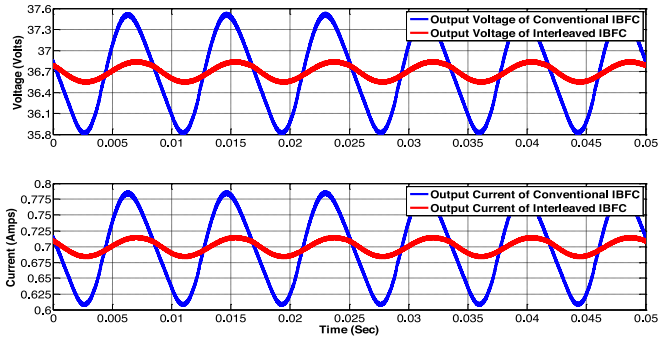

Fig. 8. Output voltage (top) and currents (bottom) of the IBFC (in blue) and the Interleaved IBFC (in red).

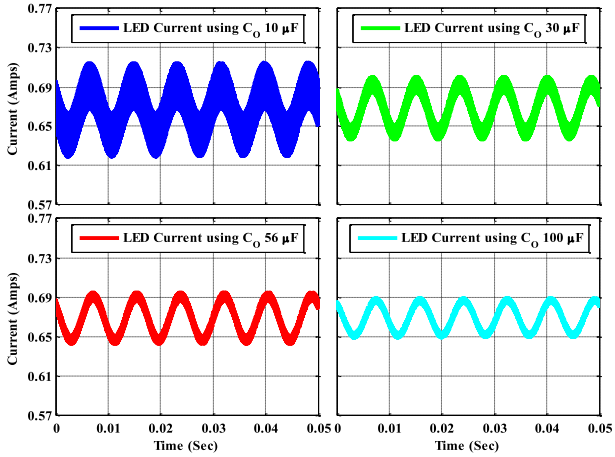

Fig. 9. LED current of the IIBFC with different output capacitances.

TABLE I
SIMULATION RESULTS OF THE IIBFC OUTPUT CURRENT AND VOLTAGE RIPPLES WITH DIFFERENT OUTPUT CAPACITANCES

Capacitor C_O	Output current ripple percentage	Output voltage ripple percentage
10 µF	*14.2%*	*6.5%*
30 µF	*9.5%*	*4.3%*
56 µF	*7.8%*	3.5%
100 µF	5.9%	2.7%

of the ripple percentage of the output current and voltage for different capacitances. As an LED driver, the current ripple is more significant due to the low LED series resistance. However, this table gives an idea of the voltage ripple in case that the application was voltage-ripple oriented and will operate with a pure resistive load.

For this application, an output current ripple of 6% is required. Thus, a big output capacitor of 100 μF is required to keep the ripple below this value. Moreover, the driver is designed in order to supply an LED load, which is characterized by a small dynamic resistance. In other words, a small output voltage variation will lead to a huge variation in the LED current, and in return a huge luminous variation that will hinder the human vision. However, in order to achieve this value of ripple using the conventional IBFC, the capacitance value should be at least 820 μF, which means eight times larger capacitance. The reason of the reduction of the low-frequency ripple is the unbroken conduction of the IIBFC. In other words, the small conduction angle of the conventional IBFC creates a period where the buck converter is not conducting, while the power delivered to the output must be continuous. This phenomena increases the gap between the input power and the output power, which in return increases the ripple. This is not the case of the proposed IIBFC, as the converter is intended to have a conduction angle of 180°.

B. Mathematical Analysis

In the following, the analysis of the currents in the converter is presented. The analysis shows the important design characteristics when both stages, buck and flyback, operate in DCM. For the sake of simplicity, the analysis will consider an ideal converter. An ideal sinusoidal line voltage waveform will also be considered, expressed as $v_g(t) = V_g \sin(2\pi f_l t)$.

In order to determine the operation of the two flyback diodes, D_{FL} and D_{FH}, the peak value of both buck and flyback currents have to be determined. Taking into account (1), and that V_{int} is selected to be equal V_B, the peak value of the buck current is expressed as follows:

$$i_{B_{\text{peak}}} = \frac{D}{f_s L_B} v_{\text{AC}_{\text{Bridge}}} = \frac{DV_g}{f_s L_B} \left|\sin\left(2\pi f_l t\right)\right|. \quad (2)$$

Concerning the flyback current, as in the proposed topology there are two secondary windings, it consists of two terms as shown in Fig. 6. The first term is the current stored in the magnetizing inductance, which will be delivered to the output later during switching OFF, whose peak value is expressed as the following:

$$I_{\text{Lm}_{\text{peak}}} = \frac{V_B D}{f_s L_m}. \quad (3)$$

The second term of the flyback current is the current going to the interleaved capacitor. At steady state, and considering ideal operation without losses, the power going to the interleaved capacitor should be equal to the power extracted from it. Thus, the current going to the interleaved capacitor should be equal to the current of the buck converter during the turn ON interval. Therefore, the peak value of the second term of the flyback current is expressed as the following:

$$i_{p_{\text{peak}}} = \frac{N_i}{N_p} i_{\text{int}_{\text{peak}}} = n_i i_{B_{\text{peak}}} = \frac{n_i DV_g}{f_s L_B} \left|\sin\left(2\pi f_l t\right)\right|. \quad (4)$$

As this design is made in order to set the interleaved voltage to be equal to the bulk voltage, hence the turn ratio n_i is chosen to be 1. In return, the second term of the flyback current will be equal to the buck current, and the peak current of the flyback is determined by the addition of (3) and (4) as the following:

$$i_{F_{\text{peak}}} = \frac{V_B D}{f_s L_m} + \frac{DV_g}{f_s L_B} \left|\sin\left(2\pi f_l t\right)\right|. \quad (5)$$

In this way, the flyback current is continuously greater than the buck current. Thus, as aforementioned, D_{FH} will never conduct and can be removed, as it conducts only if the buck current is higher than the flyback's. Summarizing, the proposed interleaved technique insures a flyback current greater than the buck current and in return D_{FH} is eliminated.

Regarding the operation of the converter, a full DCM has to be ensured. Hence, a study for the boundaries is made in order

to be able to choose the reactive elements. As the buck converter is operated in DCM, the input stage will behave as a resistance for the line. Nevertheless, when an interleaved capacitor is used, the resistance value of the buck converter is not affected, and it is expressed as the following:

$$R_g = \frac{2L_B f_s}{D^2}. \tag{6}$$

Therefore, the value of the average line current is calculated as follows:

$$\langle i_g \rangle = \frac{v_g}{R_g} = \frac{D^2 V_g}{2L_B f_s} \sin(2\pi f_l t). \tag{7}$$

Knowing that both voltage and current waveforms will be sinusoidal, the mean input power is calculated as the following:

$$P_g = \frac{1}{2} V_g \langle i_g \rangle_{\text{peak}} = \frac{1}{2} V_g \frac{D^2 V_g}{2L_B f_s} = \frac{D^2 V_g^2}{4L_B f_s}. \tag{8}$$

Concerning, the flyback power delivered to the output, it is expressed as the following:

$$P_F = V_B \langle i_{\text{Lm}} \rangle = V_B \left(\frac{1}{2} I_{\text{Lm}_{\text{peak}}} D \right). \tag{9}$$

Substituting (3) in (9), the following expression for the power of the flyback delivered to the output is found:

$$P_F = \frac{D^2 V_B^2}{2L_m f_s}. \tag{10}$$

Concerning the output power, it is found using the equivalent resistance of the LED, as the following:

$$P_{\text{Out}} = \frac{V_O^2}{R}. \tag{11}$$

Ideally, the input power will be equal to the flyback power and equal to the output power. Therefore, by equaling the three equations of the power, a relation between the input voltage and the bulk voltage is found, as well as a relation between the bulk voltage and the output voltage, as shown in the following equations:

$$\frac{V_g}{V_B} = \sqrt{\frac{2L_B}{L_m}} \tag{12}$$

$$\frac{V_O}{V_B} = D\sqrt{\frac{R}{2f_s L_m}}. \tag{13}$$

The equations of the powers shown in (8) and (10) represent the two operation constrains. However, still to ensure full DCM mode of operation, additional constrains have to be added, which are the boundaries of the DCM operation. Therefore, t_1 shown in Fig. 5 has to be lower than the switching frequency period for a flyback DCM operation. Same condition has to verify t_2 for a buck DCM operation. The procedure to find those two parameters is to determine two expressions for the peak current, one in terms of the duty cycle and the other one in terms of t_1 for the flyback and t_2 for the buck. The peak value of the magnetizing inductance current expression in terms of duty cycle was found in (3), and it is found also in terms of t_1 as the following:

$$I_{\text{Lm}_{\text{peak}}} = \frac{N_s}{N_p} I_{O\ \text{Peak}} = n_s \frac{V_O}{L_m} (t_1 - DT_s). \tag{14}$$

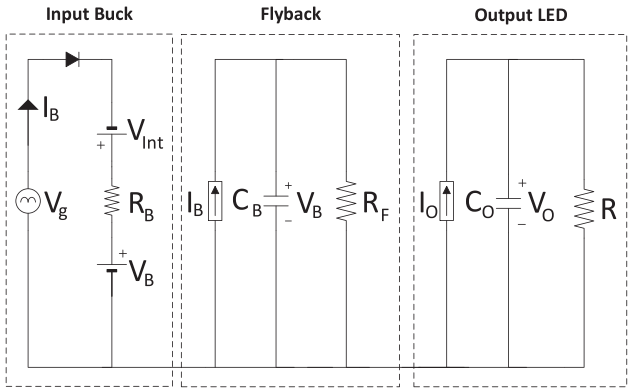

Fig. 10. Average model of the Interleaved Buck Flyback converter.

Matching (3) and (14), the following expression for t_1 is found:

$$t_1 = DT_s \left(\frac{V_B}{n_s V_O} + 1 \right). \tag{15}$$

Likewise for t_2, the peak value of the buck current was found in terms of duty in (2), and also it is found in terms of t_2 as the following:

$$I_{B_{\text{peak}}} = \frac{V_B}{L_B} (t_2 - DT_s). \tag{16}$$

Matching (2) and (16), the following expression for t_2 is found:

$$t_2 = DT_s \left(\frac{v_g}{V_B} + 1 \right). \tag{17}$$

C. Average Model of the IIBFC

For a better illustration of the operation of the IIBFC, an average model has been developed, as illustrated in Fig. 10. The average model is useful to understand the power flow in the converter. Also, it is a faster way to check the magnitude of voltages and currents in all parts without the high-frequency switching effect.

Using the average model with the previously obtained equations, the relation between the buck voltage and the inductor peak current with respect to the buck inductance has been plotted, as shown in Fig. 11. This figure is drawn using the parameters shown in Table II for a switching frequency of 40 kHz and output power of 25.9 W. It is clear that the voltage and the peak of the buck inductor current decrease as the buck inductance increases. However, this is in DCM but after CCM the behavior changes, at first increases, then decreases in small deviations. Besides, increasing the inductance after the CCM area is ineffective, because the operation as well as the PF and THD will be worse. Therefore, the chosen buck inductance will be 900 μH.

IV. Design Procedure of the Laboratory Prototype

A. Power Stage

Using the previously determined equations and the average model illustrated in Fig. 10, a design is made to supply an LED luminaire of 37 V/0.67 A, resulting in 25.9 W of output power. The line voltage is 110 V_{rms} and line frequency is 60 Hz. Seeking

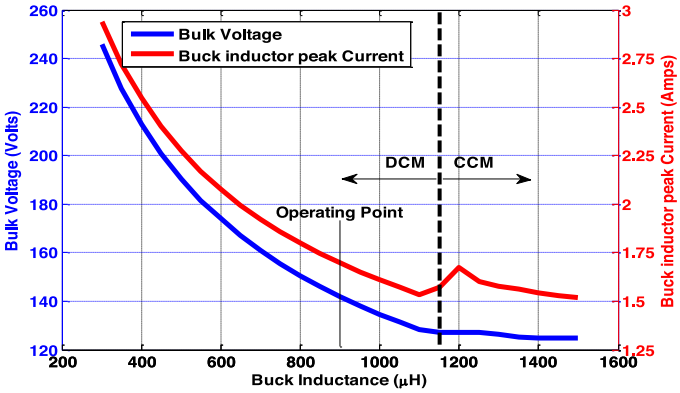

Fig. 11. Bulk capacitor voltage and inductor peak current with respect to the buck inductance.

TABLE II
COMPONENTS OF THE LABORATORY PROTOTYPE

Component	Value
Input Filter Inductor	*2.58 mH*
Input Filter Capacitor	*68 nF*
Buck Inductance	*ER2510/PC44,* $L_B = 900\ \mu H$, N = 60
Flyback Transformer	*PQ2625/3C90,* $L_m = 1.5\ mH$, $N_p = 25\ T$, $N_s = 6\ T$, $N_i = 25\ T$
Bulk Capacitor	47 μF, 250 V
Interleaved Capacitor	2.2 uF, 250 V
Output Capacitor	100 μF, 50 V
M_1	SPA07N60C3
Bridge Diodes	DB156S
D_B & D_{FL}& D_{AUX}	MURS260T3G
D_{OUT}	STPS3150

for a better efficiency, the converter is tested to work under the quasi-resonant technique. The quasi-resonant technique shows better efficiency as it reduces the switching losses. One drawback of this technique is the variable switching frequency operation. Nevertheless, the value of the magnetizing inductance can be designed to keep the switching frequency around a given value without much excursion.

The selected operating switching frequency is to be around 40 kHz, and to ensure this operation, the magnetizing inductance will be chosen to fix t_1 to be equal to 80% of the switching period. This will ensure that the switching frequency will be around 40 kHz.

Concerning the buck inductance value, it will be designed to optimize the operation of the converter. As shown in Fig. 11, this will occur at the boundary operating point between the DCM and CCM, in order to decrease the bulk capacitor voltage and the inductor current as much as possible. Moreover, the best operation in terms of PF and THD is ensured at DCM. Accordingly, t_2 has to be equal to the switching period at the peak input voltage. However, this is in an ideal situation, so a safety margin of 20% is selected in order to ensure DCM operation in the practical implementation. Therefore, as shown by the vertical line in Fig. 11, the operating point is a little before the boundary of DCM and CCM.

Applying this constrains to (15) and (17) related to t_1 and t_2 respectively, the values of the buck inductance, the magnetizing inductance, and the turn ratio are found. Table II shows the parameters of the components used for the laboratory prototype.

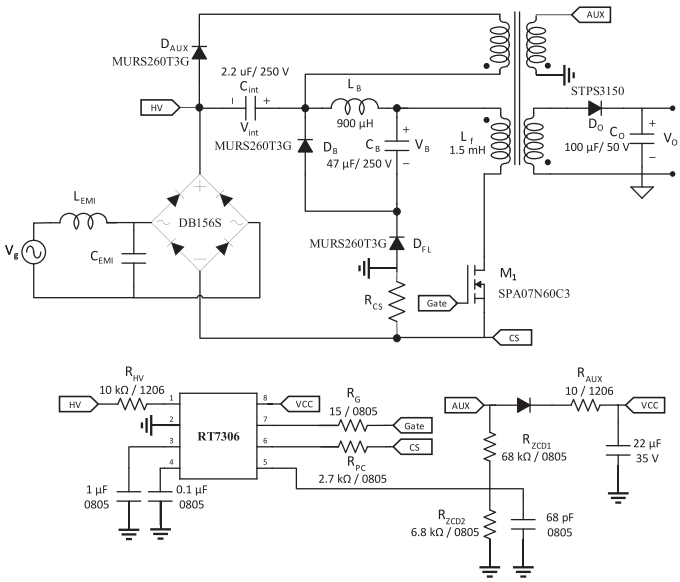

Fig. 12. Schematic diagram of the laboratory prototype.

B. Control Stage

The quasi-resonant technique has previously been presented with the flyback converter and it shows an improvement in the efficiency of the flyback [30]–[32]. The quasi-resonant technique consists in turning ON the switch at the valley value of the voltage across the switch, so that the switching losses are decreased. The same technique will be used here as well with the IIBFC. The IC used for the control is the primary-side LED driver controller RT7306 [33]. As a standalone driver, the power of the IC should come from the driver itself. The control IC has a built-in high-voltage startup system just by connecting it with a high resistance to the converter just after the bridge. Later on, the power is taken from a fourth winding added to the flyback transformer with reversed polarity with respect to the primary winding. The controller IC shows great advantages such as implementing the quasi-resonant technique, constant output current regulation, and dimming capability. Furthermore, the IC shows the great advantage of primary-side control. So the output current is controlled by sensing the peak value of the flyback switch current.

The control is made by adding a series resistance to the flyback switch to obtain a voltage signal to the control IC. The series resistance can be calculated from the equations presented in [33]. However, this control method is not directly applicable to the proposed IIBFC. The reason is that in the proposed topology, the switch is not carrying the current of the flyback, but also the current going to the interleaved capacitor. As aforementioned, and as shown in Fig. 7, the current of the diode D_{FL} is the current of the switch minus the interleaved current. Thus, the current through the diode can be used to get the signal going to the control IC. The placement of the sensing resistance in series with the diode will create a sensing signal, but with negative polarity. In order to create a positive signal so that it complies with the specifications of the control IC, the ground is placed between the resistance and the diode. Fig. 12 shows the detailed schematic diagram of the laboratory prototype, in both aspects power and control.

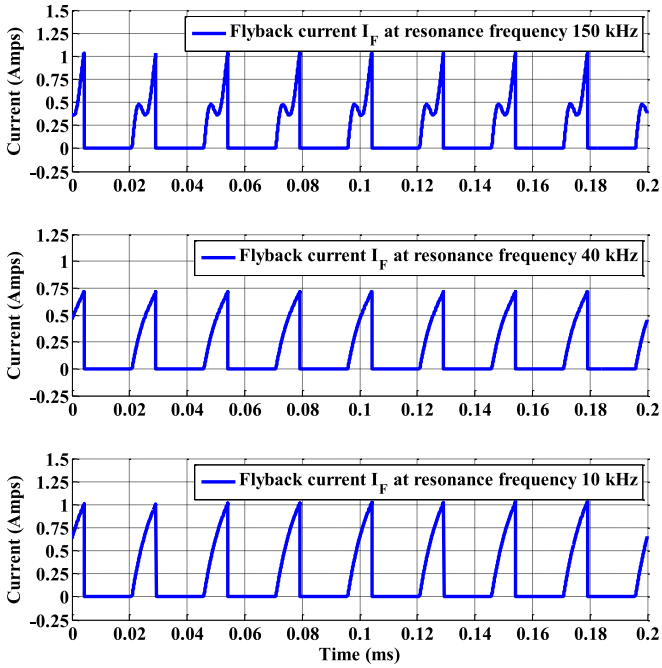

Fig. 13. Flyback current I_F at different resonance frequencies, top: 150 kHz ($C_{\rm int} = 150\ \eta$F), middle: 40 kHz ($C_{\rm int} = 2.2\ \mu$F), and bottom: 10 kHz ($C_{\rm int} = 33\ \mu$F).

The interleaved capacitor affects the shape of the flyback current. In return, it influences the shape of the signal going to the controller IC. This means that the value of the interleaved capacitor has to be selected so that it does not disturb the operation of the converter. Analyzing the behavior of the converter, it is found that the interleaved capacitor with the transformer leakage inductance creates a resonance in the system. The diode added in series with the interleaved capacitor $D_{\rm int}$ protects the system from going to unstable operation. However, this resonance still affects the flyback current and the signal going to the controller IC. The resonance frequency is calculated as the following:

$$f_{\rm res} = \frac{1}{2\pi\sqrt{L_{k_i} C_{\rm int}}}. \tag{18}$$

Using (18), Fig. 13 is drawn showing the flyback current for different resonance frequencies. The plots show resonance frequencies from top to bottom of 150, 40, and 10 kHz.

As shown in Fig. 13 first plot, when the resonance frequency is much higher than the switching frequency, the current will include fluctuations. Moreover, the peak value of the current is not correctly referring to the output current. This means that the controller will not correctly regulate the output LED current. On the other hand, as shown in Fig. 13 third plot, when the resonance frequency is much lower than the switching frequency, there is no fluctuation in the current. However, still the peak value of the current is not correctly referring to the output current. Furthermore, the low resonance frequency requires the usage of a higher capacitance value, which in return increases the size and cost of the converter, and also creates a high peak in the current during start-up. Concerning Fig. 13 second plot, it shows the case of a resonance frequency equal to the switching frequency. It is clear that there is no fluctuation, and also the current is in agreement with the output LED current.

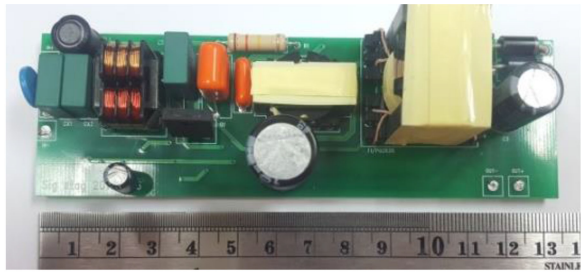

Fig. 14. Prototype photograph.

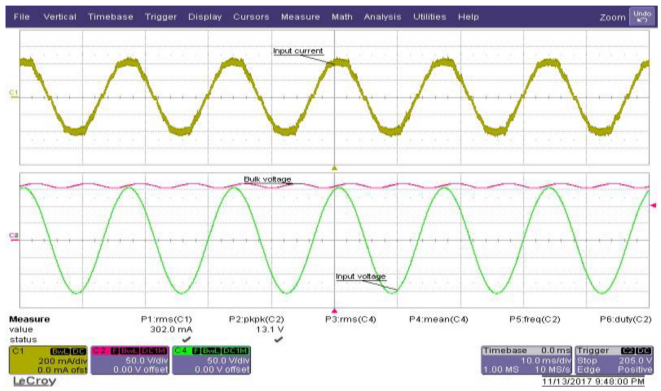

Fig. 15. Top: input current, and bottom: input sinusoidal voltage (green) and bulk voltage (red).

Fig. 14 shows the prototype photography. As can be seen, the converter is very compact.

V. Experimental Results and Discussion

The line voltage and current waveforms, as well as the buck voltage, are shown in Fig. 15. As can be seen, the current waveform is a pure sinusoidal waveform, which illustrates that the proposed technique insures that the PF and the THD will satisfy the standards. Analyzing the input current waveform, the PF is 0.997 and the THD is 2.5%. The efficiency is found to be 80%. Regarding the result of the efficiency, it is fair to justify that this is a low power application of only 25 W. Moreover, it is a low input and output voltages (110 and 37 V, respectively) and high current (0.7 A) application. In addition, the figure of efficiency includes all control and power circuitry, since this is a final prototype designed for stand-alone applications.

Fig. 16 shows the case of using the conventional IBFC. As shown, it is clear that the conduction angle is lower. However, the design of this converter was made in order to decrease the buck voltage as much as possible (85 V), further than this a CCM operation will occur. The PF in this case is 0.89 and the THD equal 23%, which is on the limit of the standards. Thus, there is no more room for improvement using the conventional IBFC. Moreover, as shown also in Fig. 16, the ripple voltage in the buck capacitor is very high, reaching 30%, which is not the case of the IIBFC, as it is found to be in the range of 8% using the same capacitor voltage rating, as shown in Fig. 15.

Fig. 17 shows the output voltage and current. It is clear that the control is working perfectly, as the voltage and currents are fixed at the desired values of 37 V and 0.67 A. As shown in Fig. 17,

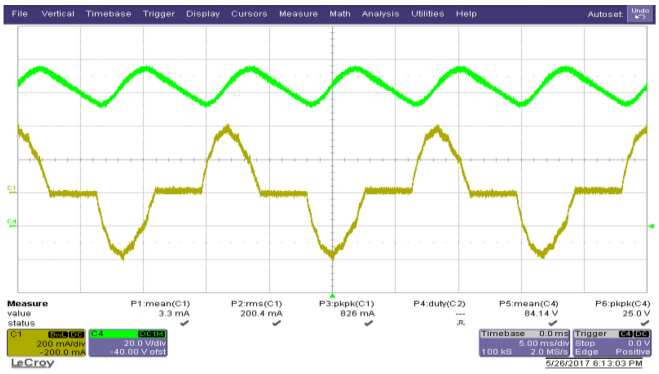

Fig. 16. Bottom: input current, and top: bulk voltage, for the conventional IBFC.

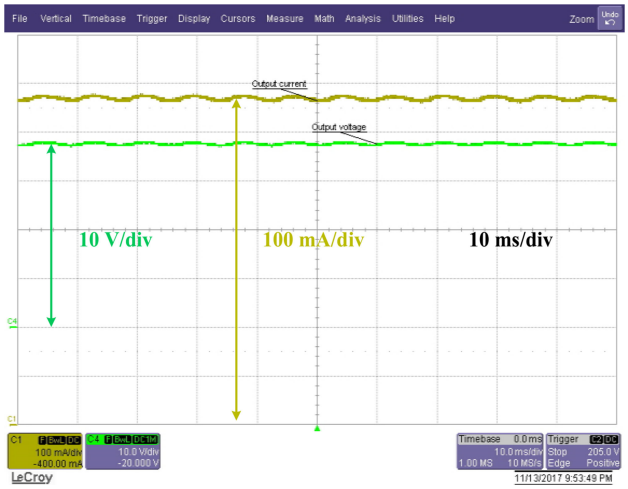

Fig. 17. Output current (yellow), and output voltage (green).

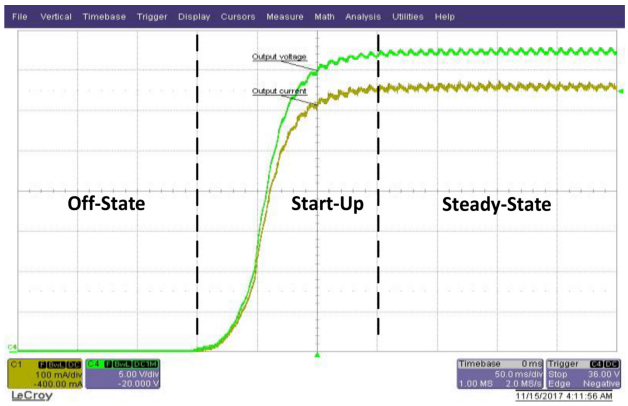

Fig. 18. Output current (yellow), and output voltage (green).

the ripple in the current equals 48 mA, taking into account that most of the ripple is high-frequency ripple. Concerning the low-frequency ripple, it is equal to 20 mA. Thus, the ripples are in the range required for this specific application. Fig. 18 shows the start-up process of the converter. As can be seen, it shows a smooth and fast starting up process, without overshoot, or oscillations.

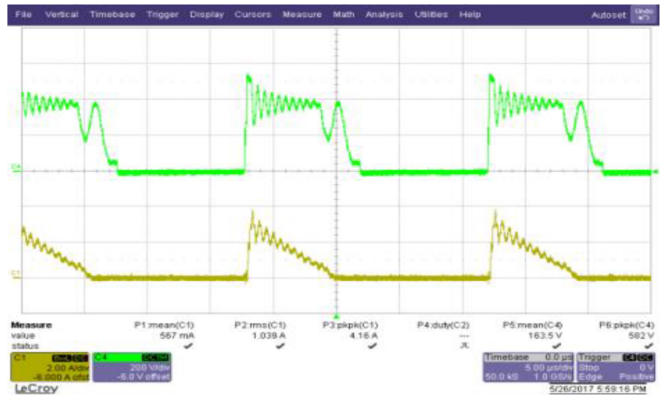

Fig. 19. Bottom: output flyback current, and top: voltage across the switch.

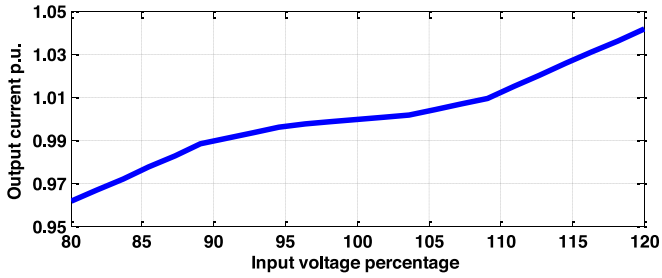

Fig. 20. Per unit output current with respect to the variation of input voltage.

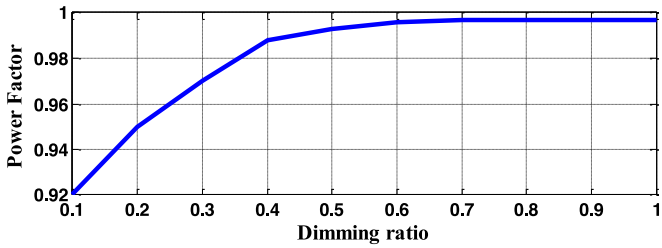

Fig. 21. Power factor with respect to dimming ratio.

Fig. 19 shows the switch voltage and the output flyback current. As shown in Fig. 19, the quasi-resonant technique is perfectly implemented, as the turn-OFF occurs at the voltage valley, which is the lowest value of the voltage over the switch within the switching period.

Fig. 20 shows the regulation curve related to the variation of the output current with the input voltage. The driver is tested for a variation of $\pm 20\%$ of the rated input voltage. The driver shows an acceptable operation, as the current is well controlled, with just $\pm 4\%$ of error.

Fig. 21 shows the power factor with respect to the variation of the dimming ratio. The experimental results prove that the interleaved topology will ensure a PF fulfilling the standards at any dimming ratio, reaching a minimum dimming ratio of 10%.

Commenting on Fig. 19, it is found that the switch experiences high voltage and current stresses. This is the case in most of single-switch integrated converters. This effect is the trade-off for using a single switch instead of two. Nevertheless, in spite of the higher stress in the switch, it is still better than having two switches with two driver circuits and two control strategies for both switches. However, by redesigning the parameters of the proposed driver, a reduction in the voltage across the switch

TABLE III
COMPARISON AMONG THE PROPOSED TECHNIQUE AND THE UP-TO-DATE PFC TECHNIQUES [34], [35]

Pulsating-Power-Buffering (PPB) [34]	Single-switch PPB single-phase PFC [35]	PROPOSED IIBFC
2 switches are used	*1 switch is used*	*1 switch is used*
1 inductor	*2 inductors*	*2 inductors*
No Isolation	*No Isolation*	*Isolation between input and output*
Complicated control (DSP is needed "TMS320F28069")	*Complicated control (DSP is needed "F28069")*	*Simple and straight-forward control (single IC "RT3706")*
Additional board for sensors is required	*Two sensors are required*	*One built-in voltage sensor is required*
High price and Bigger size	*High price and Bigger size*	*Low price and Compact size*
Line voltage (110V)	*Line voltage (110V)*	*Line voltage (110V)*
Output Voltage (100-200V)	*Output Voltage (120V)*	*Output Voltage (37V)*
Medium power application 110 W	*Medium power application 100 W*	*Low power application 25 W*
5% voltage ripple using 40μF	*4.7% voltage ripple using 30μF*	*2.7% voltage ripple using 100μF 4.3% voltage ripple using 30μF*
High efficiency, 94.7% at rated power 110 W	*Medium efficiency,89% at rated power 100 W*	*Low efficiency, 80% at rated power 25 W*

can be achieved to 300 V. However, the presented design is not aiming at a decrease in the voltage across the switch as a higher switch voltage provides other advantages as follows:

1) One diode will not conduct and can be removed.
2) The decrease in the voltage will lead to a higher ripple on the bus and output voltages.
3) Both flyback and buck current peaks will increase, and in return the ratings of the diodes need to increase. Thus, it is preferable to use a higher rating switch rather than three higher rating diodes. Moreover, concerning the switching losses, a soft turn-ON switching is assured, as it operates in DCM, and because a quasi-resonant technique is used the turn-OFF losses are minimized. On the other hand, a higher current in the diodes would lead to a higher conduction loss.

Finally, a comprehensive comparison with the up-to-date PFC methodologies [34]–[36] is shown in Table III. All three methodologies aim at absorbing continuous power from the ac main in order to have better THD and PF. In addition, they try to avoid sending the input power oscillations to the output, in order to reduce the output ripple. As shown in Table III, the proposed IIBFC has the following promising features compared to the other techniques:

1) single switch driver;
2) isolation between input and output;
3) simple control circuitry;
4) only one voltage sensor is required;
5) compact size;
6) low cost;
7) low output ripple.

On the other hand, it has a single drawback which is the lower efficiency.

VI. CONCLUSION

This paper presents a new topology that enhances both PF and THD to be well below the limitations specified by the IEC 61000-3-2 standard. This is done by inserting an interleaved capacitor between the rectifier and the converter. The converter used to drive the LED is the IBFC converter, previously presented in [24]. The interleaved capacitor voltage is fixed by a third winding added to the flyback transformer. Furthermore, the proposed IIBFC reduces the ripple by a factor of five, which means a significant reduction of the output and buck capacitors. Also, the proposed technique avoids any complex circuitry, or any other extra sensors apart from those used in the conventional IBFC, since the control technique is the same as that used for the IBFC. Regarding the power component, the proposed topology offers all these features by only adding an extra winding in the flyback transformer, a capacitor of 2.2 μF and an extra diode. However, the proposed technique ensures that a diode of the conventional IBFC will not be conducting so that it can be removed.

Finally, a prototype working at 110 V, 60 Hz, and 37 V output, driving a LED luminary of 25 W, has been designed and implemented to prove the previously illustrated characteristics. Experimental results have proven that the harmonic content of the input current equals 2.5%, and the power factor equals 0.997 at full power operation. Moreover, the converter meets the IEC-61000-3-2 standard at any dimming ratio, reaching a minimum dimming ratio of 10%. The converter efficiency is 80%, which is good considering the simplicity of the converter, the low power of the present application, and the good features offered by the converter.

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