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Designing a Delta-Sigma Modulator with Low Power Consumption and High Accuracy and Speed Using IIR Filter as NTF Relevant Structure

Seyyed Ali Eslami[1] · Farhad Razaghian[2] · Amir Amirabadi[2]

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Abstract
A fifth-order delta-sigma modulator with low power consumption, high speed, and accuracy is designed and simulated systematically and as circuitry. The proposed structures are implemented in MATLAB and HSPICE using technology parameters (0.18 μm CMOS TSMC). The final structure employs an IIR filter as an upgraded NTF-relevant structure. Many popular structures use a lot of power due to their incorporation of two integrators and an IIR filter placed after or before the IIR filter. Therefore, in the proposed structure, the number of integrators is reduced to one. The dual sampling technique is used in the modulators' structure to increase speed. In each configuration, the NTF equation is considered as an FIR filter. The structure seeks to optimally combine integrators and IIR filters with delta-sigma modulators. To enhance the stability of delta-sigma modulators, the NTF transfer function is finally converted from an FIR to an IIR filter. The results for this delta-sigma structure are as follows: sampling frequency: 12.5 MHz, oversampling ratio: 8, signal-to-noise ratio: 82 dB, dynamic range: 90.2 dB, bandwidth: 4.7 MHz for the system model and 4.5 MHz for the circuit model, and power consumption: 56.6 mW for the system model and 62.7 mW for the circuit model.

Keywords Delta Sigma modulator · Low power consumption · A/D converter · NTF

✉ Farhad Razaghian
Razaghian@azad.ac.ir

Seyyed Ali Eslami
alisls69@gmail.com

Amir Amirabadi
a_amirabadi@azad.ac.ir

[1] Department of Electrical and Computer Engineering, Science and Research Branch, Islamic Azad University, Tehran, Iran

[2] Department of Electrical Engineering, South Tehran Branch, Islamic Azad University, Tehran, Iran

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Abbreviations

FIR	Finite impluse response
IIR	Infinite impluse response
NTF	Noise transfer function
NSIQ	Noise-shaped Integrating quantizer
SAB	Simple amplifier biquad
DNSQ	Double noise-shaped quantization
VCO	Voltage controlled oscillator
VTC	Voltage to time converter
TDC	Time to digital converter
SAR	Successive approximation register
OSR	Oversampling ratio
CMOS	Complementary metal oxide semiconductor
SNR	Signal to noise ratio
SNDR	Signal to noise and distortion ratio
DAC	Digital to analog converter
SFDR	Spurious-free dynamic range
ADSL	Asymmetric digital subscriber line
PSRR	Power supply rejection ratio
CFF	Counter flip-flop
BFF	Bit flip-flop
FF	Flip-flop
ENOB	Effective number of bits
FFT	Fast fourier transform
ADC	Analog to digital converter
FOM	Figure of merit
APWM	Asynchronous pulse width modulation
DS	Double sampling
OPAMP	Operational amplifier
TDFQ	Time domain flash quantizer
DWA	Data weighted averaging
SDN	Software-defined networking

1 Introduction

In both wired and wireless communication, as well as in digital imaging and personal electronic devices, there is a significant demand for data converters that offer high accuracy, high bandwidth, and high power efficiency [18, 36]. Since many practical systems operate on analog signals, converting these signals to digital form is essential for easier processing [17]. This conversion is achieved using analog-to-digital converters (ADCs). Unlike analog circuits, digital circuits are less sensitive to noise and more resistant to variations in power supply and manufacturing processes. Additionally, digital circuits benefit from automated design, testing, and enhanced programmability

[8, 23, 28]. The use of Software-Defined Networking (SDN) principles enhances the programmability of networks [29, 30], enabling more efficient data flow management akin to digital circuits in sensor networks [1].

One of the most effective techniques for converting low-frequency signals, using the previously described sampling approach and noise shaping, is the Delta-Sigma modulator method. Traditionally, discrete-time $\Sigma\Delta$ modulators were predominantly used. However, continuous-time $\Sigma\Delta$ modulators have recently garnered increased attention [13, 24, 31, 38]. Discrete-time Delta-Sigma modulators are highly attractive due to their ease of implementation, high accuracy, and linearity. They rely on switched capacitor circuits, which depend only on capacitance values and are independent of the clock pulse rate. This means the clock pulse frequency of discrete Delta-Sigma modulators can vary widely [33, 35].

In contrast, continuous-time Delta-Sigma modulators face challenges from non-ideal elements such as clock jitter, additional loop delay, and temporal fluctuations [21]. Despite these issues, continuous-time Delta-Sigma modulators have recently gained significant attention due to their much higher speed compared to discrete-time modulators [25]. Additionally, continuous-time modulators tend to consume less power [12], contributing to longer battery life and reduced weight and size in portable applications. They also offer inherent anti-aliasing properties, eliminating the need for anti-aliasing filters required in discrete modulators [2], and generally exhibit better noise performance [6]. In a similar vein, Multi-objective Optimization Techniques are increasingly applied in sensor networks to optimize performance metrics such as power efficiency, accuracy, and speed, mirroring the design objectives of continuous-time Delta-Sigma modulators [9, 15].

Lower power consumption is not only crucial for portable devices but also reduces heat dissipation, which is vital for large integrated circuits. Even for non-portable applications, minimizing power consumption is important for environmental protection, making it a critical design consideration from both legal and ethical perspectives [14, 22, 26]. In recent years, numerous studies have focused on Delta-Sigma modulators [5, 7, 10, 19, 20, 27, 37, 39]. One notable study designed and simulated a Delta-Sigma modulator based on a VCO quantizer, utilizing three Opamp-based integrators to achieve 4th-order noise shaping [24].

The study offered a comparable investigation but indicated minimal power use. In fact, the key structure of this study is a 5-bit analog-to-digital converter based on a VCO [31]. The study focuses on a third-order continuous-time delta-sigma modulator with an input and output shift-based Data Weighted Averaging (DWA) circuit and a 3-bit Time Domain Flash Quantizer (TDFQ) circuit. The TDFQ circuit is used to save power and mitigate design problems at low voltages. This solution solves the linearity problem of the VTC converter based on delay, without calibration, reducing power consumption and expanding the system's dynamic range [4]. Additionally, the study presents a continuous-time delta-sigma modulator with a noise coupling concept based on Asynchronous Pulse Width Modulation (PWM) and a TDC converter [32].

The concept of noise coupling involves deriving the quantization error from the TDC and injecting its delayed version into the APWM input. This approach enhances the noise-shaping order of a unit. In one study, a continuous-time Delta Sigma modulator utilized a double noise-shaping quantizer (DNSQ), resulting in 6-bit quantization

alongside second-order noise shaping. The DNSQ circuit acquires the quantized error in the time domain from the NSIQ circuit (Noise-shaped Integrating Quantizer), then directly applies it to the quantizer based on the loop oscillator to implement second-order noise shaping internally [16].

Another study focuses on a delta-sigma modulator designed for low power consumption. This modulator features high bandwidth and low power consumption, achieved through a continuous-time delta-sigma modulator with a third-order filter utilizing lossless integrators. Additionally, it incorporates a biquadratic filter with a SAB amplifier (Single Amplifier Biquad) with loop compensation [3].

An active collector in this structure is realized through a common gate flow buffer, followed by a transfer resistance amplifier. To achieve medium speed and accuracy, the Hybrid Delta-Sigma modulator described in the study combines discrete-time and continuous-time Delta-Sigma modulators. This hybrid structure is implemented both systematically and as circuitry. In this specific design, the first stage operates in continuous time, while the second stage operates in discrete time [34].

Increasing the sampling frequency and decreasing the oversampling ratio (OSR) can expand the input signal bandwidth of an A/D converter, but it requires swift operating amplifiers and high rotational speed. This leads to increased clock pulse overhead, affecting digital components and resulting in a significant rise in power consumption. High-speed delta-sigma modulators are recommended to be designed with lower OSR to mitigate power consumption, but reducing OSR may limit the effectiveness of a Delta-Sigma A/D converter in achieving high accuracy [13, 24, 38].

To enhance operational speed, the study recommends employing a high-order, single-loop Delta-Sigma modulator using the Double Sampling (DS) method and a high-order structure. This design reduces the number of integrators to one, effectively reducing power consumption. The proposed design was meticulously developed both systematically and in circuitry, incorporating innovative structures to deliver results comparable to or better than other similar designs.

2 Delta-Sigma Modulators

2.1 Second-Order Delta Sigma Modulator

This section aims to present Double Sampled (speed from this approach) and the Second-Order Delta-Sigma modulator structure since the Double Sampled technique is employed in the Delta-Sigma modulator implementation to boost speed. A single-loop, second-order Delta Sigma modulator's construction is shown in Fig. 1.

In this type of modulator, if the connection of the filter loop with the NTF modulator is to be analyzed, first, Eq. (1) has to be used as follows:

$$L(z) = \frac{1 - NIF(z)}{NIF(z)} \tag{1}$$

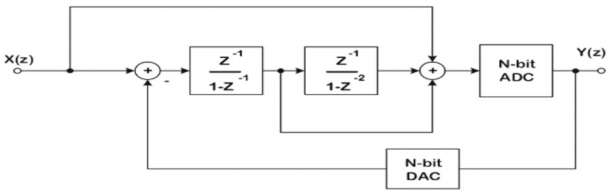

Fig. 1 Second-order double sampled modulator

If the noise-shaping function related to these proposed modulators with FIR filters is to be obtained, it should be reviewed as Eq. (2):

$$NTF(z) = \begin{cases} (1-z^{-1})(1+z^{-1}) \prod_{i=1}^{M} (1 - a_i z^{-1} + z^{-2}) & \text{if } L \text{ is odd} \\ (1-z^{-1})^2(1+z^{-1}) \prod_{i=1}^{M-1} (1 - a_i z^{-1} + z^{-2}) & \text{if } L \text{ is even} \end{cases} \tag{2}$$

The FIR noise-transfer function (Finite-Impulse-Response) is chosen to optimize DS structures with signal-transfer function. In the Second-Order delta-sigma modulator, only two first conditions of the NTF equation were considered. An extra zero is inserted in the $f_s/2$ noise-transfer function with $(1 + z^{-1})$ condition to decrease the effect of quantization noise folding into the signal bandwidth. The $(1 + z^{-1})$ condition is used as an integrator without local feedback to realize the modulator input. In the odd-order Delta/Sigma modulator, an NTF zero is introduced in DC and the other zeros are placed at frequencies inside the band to further influence noise quantization. In even-order modulators, an extra NTF zero is inserted in DC compared to odd-order modulators. Although inserting an extra zero in the $f_s/2$ frequency increases quantization noise within the band up to 6 dB and decreases SNR to the same amount, it prevents the folding effect of Quantization Noise. Additionally, inserting another extra NTF zero in the $f_s/2$ frequency can shape quantization noise more, increasing the stability of the modulator by reducing the maximum gain outside the band of the noise transfer function.

2.2 DC High-Order Delta Sigma Modulator

L(z) high-order circuits loop transfer function in the proposed DS modulators obtained by the equations mentioned in the previous sections will be in accordance with Eq. (3) and Eq. (4) taking into account the aforementioned points and the necessity of adding a zero to the modulator path to prevent quantization noise folding (4).For example, L(z) of second and third-order modulators are as follows:

$$L_2(z) = \frac{z^{-1}}{1-z^{-1}} \frac{1+z^{-1}-z^{-2}}{1-z^{-2}} = \frac{z^{-1}}{1-z^{-1}} \left(1 + \frac{z^{-1}}{1-z^{-2}}\right) \tag{3}$$

$$L_s(z) = \frac{z^{-1}}{1 - z^{-1}} \left(\alpha + \frac{\alpha(\alpha - 1)z^{-1} + \alpha(\alpha - 2)z^{-2} + (1 - \alpha)z^{-3}}{1 + (1 - \alpha)z^{-1} + (1 - \alpha)z^{-2} + z^{-3}} \right) \tag{4}$$

The proposed second-order DS modulator uses a delayed integrator and single-delayed resonator, allowing for two operational amplifiers. This allows for the implementation of input channels of a quantizer using a passive capacitive switching circuit. The resonator output is a function of noise-quantization, which can be used as the next stage input in cascode modulators. This approach simplifies the design of the modulator, making it suitable for use in various applications.

2.3 Proposed Fifth-Order Double Sampled Modulator

The proposed noise-transfer function for a high-order single-loop A double-sampled modulator can be implemented as a combination of integrators with one first-order IIR filter, as shown for the fifth-order modulator. Higher-order modulators with a large input signal can achieve stability by switching NTF from a FIR filter into an IIR filter or using a multi-bit quantizer. The noise-transfer function of these structures has a larger out-of-band gain. However, the proposed structures are considered FIR filters, so a multi-bit quantizer is needed for their stability. If a multi-bit quantizer is not sufficient, NTF poles should be located in suitable locations, requiring changes in the given structures. The DS modulator coefficients proposed in Fig. 2 to realize NTF Eq. (2) are obtained as follows:

$$\begin{aligned} &\text{for } L = 5 \\ &\beta = 1 \\ &f_1 = 4 - \alpha_1 - \alpha_2 \\ &f_2 = f_3 = 3 - \alpha_1(4 - \alpha_1) \end{aligned} \tag{5}$$

In this case, α1 coefficients are used for inserting NTF zeros at frequencies inside the baseband, which further formulates noise quantization. This primary design is proposed for high-accuracy and high-speed applications with low supply voltage (Fig. 2).

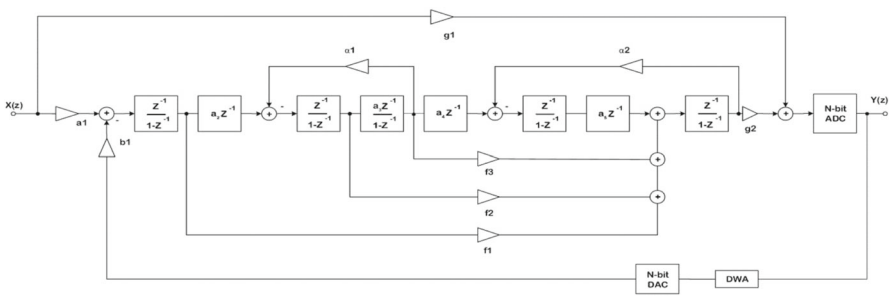

Fig. 2 The primary proposed fifth-order delta-sigma structure

This design is considered for an A/D converter with high accuracy (15 bits) and a sampling rate of 12.5 MHz, in which a fifth-order single-loop D/S modulator with a new structure is used. The output swing of a capacitive switched integrator is limited by the maximum amplitude of the output signal of the amplifier. It is directly proportional to the overload level of the modulator input. Maximizing the output swing increases the maximum value of the modulator input signal.

The study investigates the impact of amplifier output voltage saturation on the performance of a delta-sigma modulator. The accuracy of the design is limited by the kT/C noise of switches and thermal noise of amplifiers. To reduce integrator output swing, the signal scaling approach is used. Limiting or saturating blocks can be employed within the integrator loop in many modulator system simulations. The proposed D/S modulator uses integrators' output swings to be smaller than the feedback reference voltage. To improve the design, the amplifiers of the first, second, third, fourth, and fifth-order integrators need a peak output swing of 760 mV, 510 mV, 481 mV, 370 mV, and 770 mV from an 8.1 V power supply.

3 Systematic Implementation of the Proposed Modulator

This section discusses the systemic implementation of a proposed design using MATLAB, considering power supply noise in simulations (Fig. 2). The design includes a single signal transfer function and a fifth-order single-loop modulator with a multi-bit quantizer and a multi-bit DAC in its feedback channel. The DWA algorithm is used to linearize the multi-bit DAC and reduce its error. The structure includes four zeros of the noise-transfer function, which increase the modulator's dynamic range by 18 decibels at OSR = 8. The single signal transfer function reduces the integrator's input swing, prevents harmonic distortion, and increases the modulator's dynamic range.

The modulator design uses only one multi-bit DAC at the input of the first integrators, which is well linearized by the DWA method. Three feedforward paths lead to the input of the fifth integrator, expanding the modulator's dynamic range and eliminating the need for an extra gain stage. The IIR noise-transfer function is used to achieve stability at high input amplitudes with a number of achievable quantizer bits at low voltage and high speed. The modulator structure lacks an independent coefficient for synthesized noise transfer functions, but the system coefficients can be obtained through trial and error, reducing its sensitivity to non-matching coefficients. Since, in Fig. 2, transfer functions were written in the field of Z, the noise transfer function of the modulator is obtained as below:

$$\mathrm{NTF}(z) = \frac{\left(1 - z^{-1}\right)\left(\left(1 - z^{-1}\right)^2 + \alpha_1 z^{-1}\right)\left(\left(1 - z^{-1}\right)^2 + \alpha_2 z^{-1}\right)}{1 + d_4 z^{-1} + d_3 z^{-2} + d_2 z^{-3} + d_1 z^{-4} + d_0 z^{-5}} \tag{6}$$

In this equation, coefficients can be easily extracted as below:

$$
\begin{aligned}
d_0 &= -1+\beta \\
d_1 &= 5-f_1+f_2-f_3-\alpha_1-\alpha_2 \\
d_4 &= -5+f_1+\alpha_1+\alpha_2 \\
d_3 &= 10-3f_1+f_2-3\alpha_1-3\alpha_2+\alpha_1\alpha_2+f_1\alpha_1 \\
d_2 &= -10+3f_1-2f_2+f_3+3\alpha_1+3\alpha_2-\alpha_1\alpha_2-f_1\alpha_1
\end{aligned} \tag{7}
$$

function are placed by local feedbacks at both ends of the two pairs of integrators in baseband frequencies so that quantization noise inside the modulator band is shaped toward upper frequencies. To realize the noise-transfer function of the modulator as a high-pass FIR filter, its coefficients are written as follows:

$$
|X|_{\max} = V_{\mathrm{REF}}\left(\frac{2^N+8\alpha_1+8\alpha_2-2\alpha_1\alpha_2-30}{2^N}\right) \tag{8}
$$

$$
\begin{aligned}
f_1 &= 5-\alpha_1-\alpha_2 \\
f_2 &= f_3 = 5-\alpha_1(5-\alpha_1) \\
\beta &= 1
\end{aligned} \tag{9}
$$

In this case, the modulator noise-transfer function is simplified as follows:

$$
NIF(z) = (1-z^{-1})(1-(2-\alpha_1)z^{-1}+z^{-2})(1-(2-\alpha_2)z^{-1}+z^{-2}) \tag{10}
$$

It can easily be shown that the maximum value of the input signal of modulator and the input of the first integrator, if its noise-transfer function is as an FIR filter, are equal to the followings, respectively:

$$
|U|_{\max} = V_{\mathrm{REF}}\left(\frac{2(4-\alpha_1)(4-\alpha_2)}{2^N}\right) \tag{11}
$$

where V_{REF} is the reference voltage and N is the number of quantizer bits. In Fig. 3,

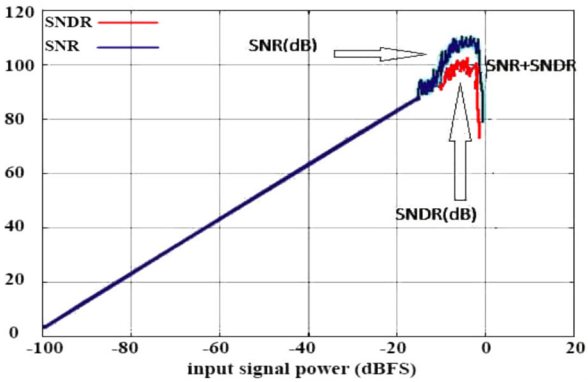

Fig. 3 SNR & SNDR of the proposed double sampled modulator based on input signal power

the SNDR of modulator output is depicted in terms of its input signal power, which shows a dynamic range of 105 dB. The implemented modulator's dynamic and OL ranges expand with input signals bigger than the full-scale range while remaining stable. Nevertheless, since the actual maximum input signal intensity is 0 dBFS, the dynamic range is 103.5 dB.

To prove the better performance of the proposed structure, Monte Carlo analysis was applied to the coefficients in the system block of the delta-sigma modulator with 30 samples, assuming a tolerance of 3% to 5% of the coefficients. The NTF of the proposed structure shown in Fig. 4 is acceptable. Considering the ability to implement this circuit with switch capacitor circuits, it will be an acceptable approximation for this circuit.

The impact of white noise on the five integrator inputs utilized in the organized block architecture of the suggested modulator is presented. The impact of a white noise source with an input range of 55 $\mu v/\sqrt{Hz}$ at every integrator's input will be represented in Fig. 5 when it comes to the NTF curve. The outcome pertaining to the SFDR diagram is displayed in Fig. 6.

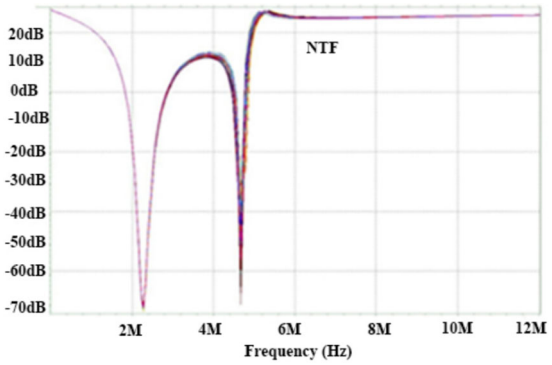

Fig. 4 Monte Carlo analysis of systematic block coefficients and their effect on the NTF curve with 3% to 5% tolerance for 30 samples

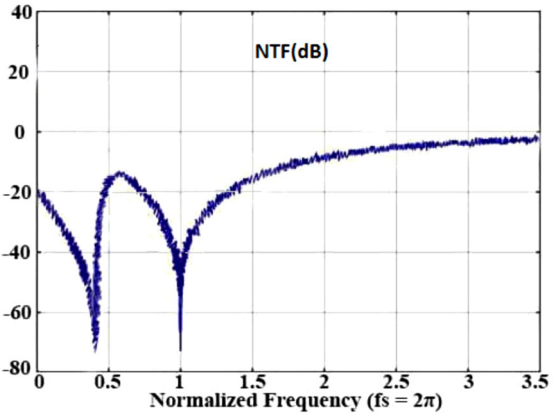

Fig. 5 The impact of white noise at all inputs of integrators on the NTF curve

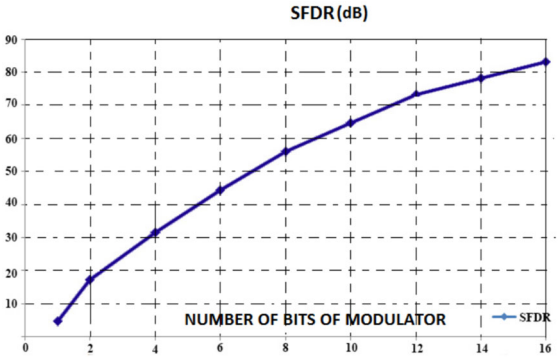

Fig. 6 SFDR diagram in terms of number of final bits of the Double Sampled modulator in the proposed structure

Table 1 Coefficients implemented by MATLAB

Parameter	Value
a_1	5.8
a_2,a_3,a_4,b_1	1
a_5	5.14
g_1	5.8
g_2	3
f_1	18.14
f_2	12.14
f_3	15.14
α_1	1.8
α_2	2.15

The optimal modulator coefficients were achieved following the MATLAB system block design and final simulation. Table 1 lists the suggested block coefficients from Fig. 2. The proposed converter's Table 1 and Fig. 2 show the 13 amplifier circuits that function as the modulator coefficients. All 13 amplifiers need to be properly constructed and simulated for the proposed converter to function satisfactorily at the intended frequency and voltage.

3.1 Design of amplifiers b1, a4, a3, a2

These four coefficients provide a single gain and function as a very high bandwidth buffer. The buffer circuit is frequently used to modify a stage having a low input impedance, a signal source with a high internal resistance to a low load resistance, or a stage with a high output impedance. To transfer the maximum amount of power between two stages, their impedances must match.A small portion of the source's generating driving force appears on the load resistor as a result of the source's decreasing generating driving force if it is directly connected to a small load resistor (R_L) with a large internal resistance (R) and an open circuit generating driving force (V). V is

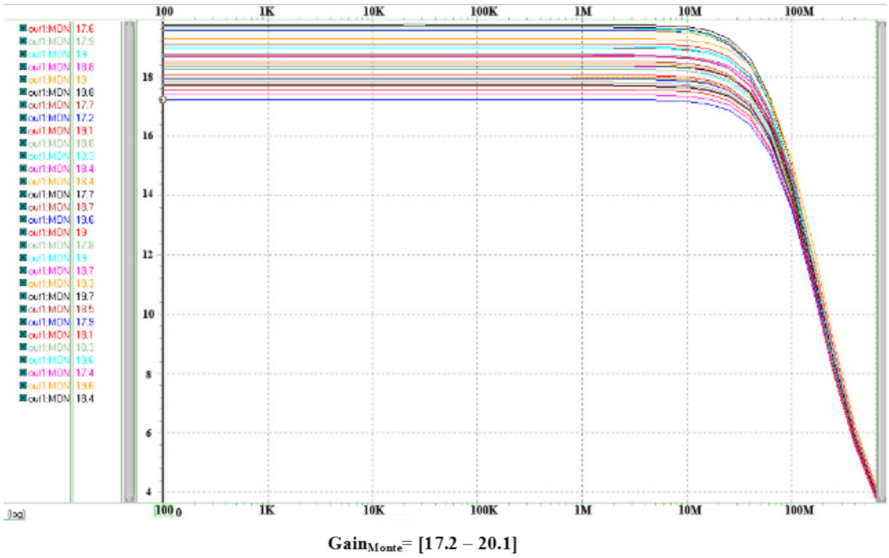

Fig. 7 Monte Carlo analysis is related to the gain of a circuit (f1 coefficient)

the circuit generator's driving force when a buffer circuit is employed to match the source.

The emitter or source follower circuit is the circuit that is most frequently utilized as a buffer circuit [11]. The harmonic distortion of the proposed low-gain amplifier circuit was assessed under transient conditions. The overall harmonic distortion was -78.63 dB up to 40 MHz in frequency.

For the recommended differential amplifier, the distortion level was appropriate. One of the circuits' gains underwent Monte Carlo analysis, the results of which are shown in Fig. 7.

According to the findings of the PSRR analysis, this process has a power supply rejection ratio of 84 dB, which is equivalent to the ratio shown in Fig. 8. The suggested buffer circuit can effectively remove power supply noise due to its high power supply rejection ratio.

Figure 8 shows that the PSRR value is clearly visible in this image, indicating that the suggested circuit's differential and structural arrangement are sufficient to remove noise from the power supply.

4 Implementation of the Proposed Modulator Circuit

For the circuit section, the outcomes of the structure simulation using HSPICE and 0.18μm TSMC Technology parameters, as suggested in Fig. 2, are given. Each targeted block needs to be developed and simulated at the transistor level in this step. The final step is to mix all the circuits to emulate the proposed delta-sigma modulator architecture.

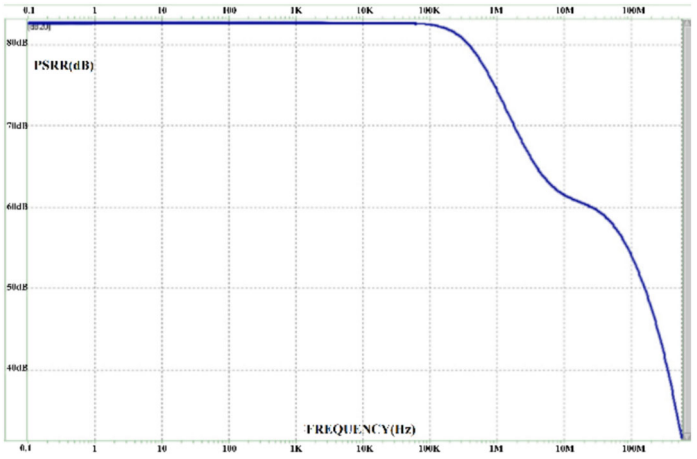

Fig. 8 PSRR of the proposed design for the circuit mode (f1 coefficient)

4.1 addition and Subtraction Circuits

One of the most crucial circuit sections in the suggested delta-sigma converter structure consists of seven addition and subtraction blocks. The suggested circuit structure for this task is shown in Fig. 9. In the suggested structure, the final output will be Eq. (12).

$$V_{OUT} = in_1 + in_2 - in_3 \tag{12}$$

Completely designed, no new design is required for addition or subtraction. Together, the two elements make up the suggested circuit. Following simulation, the suggested adder circuit has a 12μW power consumption and a harmonic distortion of -82.1 dB for each of the nine distinct harmonics up to 40 MHz. For the addition and subtraction circuit that is being suggested, that distortion value is appropriate.

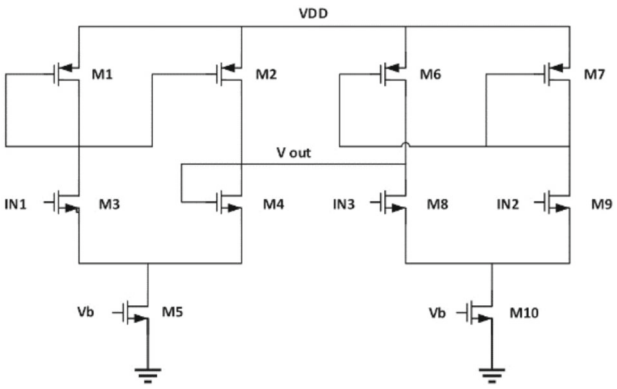

Fig. 9 Proposed structure for analog addition and subtraction circuit

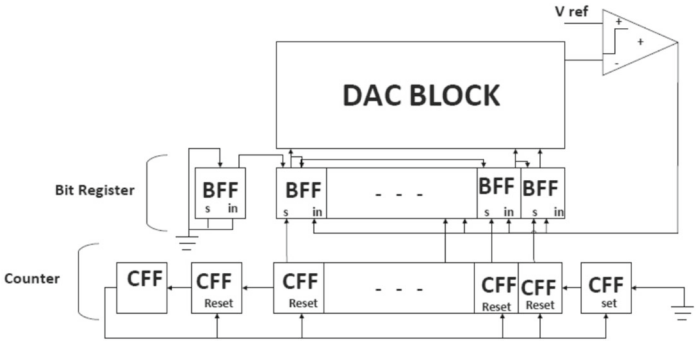

Fig. 10 The block diagram of the proposed ADC

4.2 ADC Converter Structure

The majority of systems employ analog input and output signals, which has led to an explosion in demand for quick and accurate ADC and DAC converters. These converters' digital component manipulates and stores bits. Various architectures with different requirements have been proposed so far to build this type of converter. A SAR-type ADC converter's block diagram is displayed in Fig. 10. The bit flip-flops in this figure are represented by the BFFs, and the ring-type flip-flops by the CFFs.

4.3 CFFs

A row of flip-flops (FFs) makes up a CFF counter. Every one of these FFs loads the next level in its output. Throughout each clock cycle, only one of these FFs is a "1". and the others are "0". The "1" advances one step to reach the final FF each time the clock strikes midnight. The output of this FF resets all FFs except for itself and the first FF when the last FF turns into "1". To repeat this cycle, it actually sets the first FF. This article suggests a 17-cycle converter, of which one is for error correction, 15 are for conversion, and one is for sampling. The design of FFs circuits is intended to be reset or set simply by reversing the clock in order to prevent excessive power consumption. The FFs' timing diagram is shown in Fig. 11. This number indicates that 18 FF counters are required. The reset time is displayed in the highlighted section.The pulse width of an FF before the first bit is regarded as half that of other FFs when it comes to setting and resetting the FFs by reversing the clock. In addition to moving on to the following FF, the output of FF_0,…, FF_{14} sets the FF of its corresponding bit. In each conversion cycle, the corresponding FF counter sets each bit FF once.

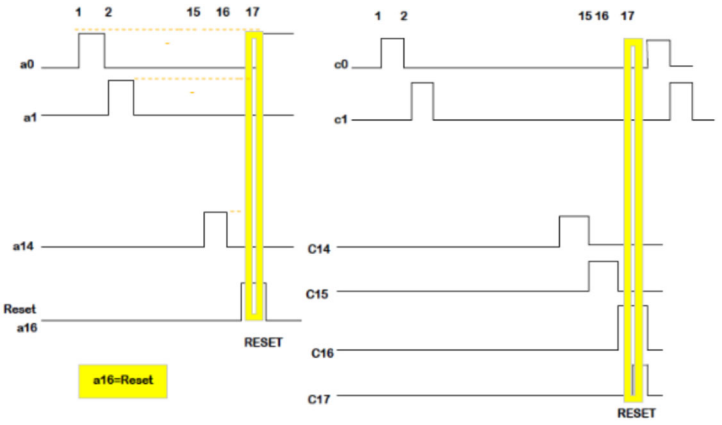

Fig. 11 The output pulses of the counter FFs

4.4 BFFs

When a bit's FF is set by its corresponding counter FF, the bit's output is always "1". The analog components of the capacitive array (DAC) and comparator circuit make decisions based on this change, and they indicate whether the bit's output stays at "1" or changes to "0" by returning it to the FF's input. Each of these FFs' clocks is the output of the subsequent, less valuable stage, as seen in the figure. The rising edge of the clock, or clock stage, is changed from zero to one by these FFs. They are loaded when their input clock is set to "0." When it is"1", they hold onto it. They only alter their state to record and store data when their clock shifts from "0" to "1". When the corresponding counter-set signal appears, each FF in a conversion cycle first changes to "1" and either stays at that value or changes to "0". As such, when they are set, they only rise once. As a result, these FFs only alter their state once every cycle and keep it there until the end.

4.5 The Digital Part

Figure 12 depicts the proposed DAC converter's structure. The digital portion of this figure is made up of 14 blocks. CFFs, BFFs, shift registers, and half-adders are all included in each block. The reset signal resets each of these blocks, resulting in a zero DAC bit output. The switches on the capacitors' bottom plates are wired with bit "0" to point Y and bit "1" to the VDD.

Figure 12 illustrates the process of a digital circuit, where the ΦS signal connects the Y point to the input voltage when it is "1", resets the digital blocks, and connects the upper plate of the DAC capacitors to the reference voltage. If not, it connects to the voltage of $V_{DD}/2$. The bottom plate of the capacitors is connected to point Y, which is now connected to the input, and the outputs D0 to D14 become "0". The input voltage is sampled by the capacitors, and the K1 and K2 switches are opened following the sampling cycle, and the Kin switch is linked to the reference voltage (VDD/2). The

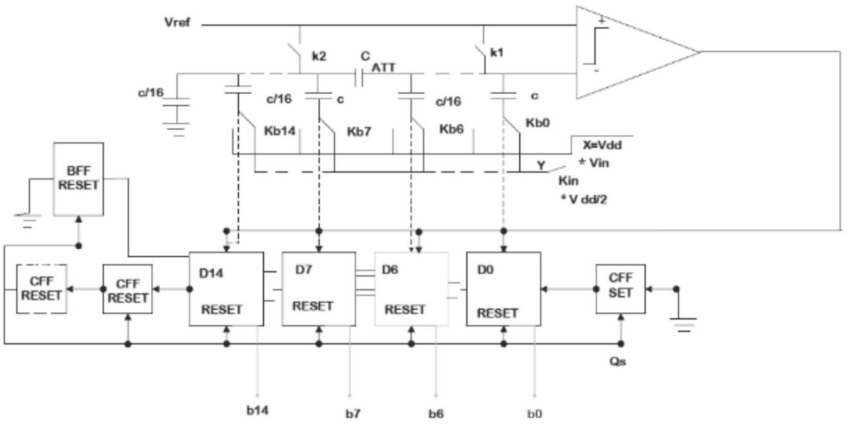

Fig. 12 The overall structure of the digital part of the converter

result is stored in the appropriate stage once the counter starts and sets the output bits of these stages (D0 to D14) to "1". The analog portion determines whether the bit stays at "1" or changes to "0" based on the voltage produced at the comparator's input when this bit changes to "1". For better comprehension, only half of this differential structure is shown in the Fig. 13. The four components of Fig. 12 are the shift register, half-adder, BFF, and CFF. It has two digital bit outputs: its corrected form (BIT) goes to the converter output, and its original form (DO) goes to this stage's DAC capacitor. The converter needs to be verified in the nth bit for use in the suggested delta-sigma modulator.

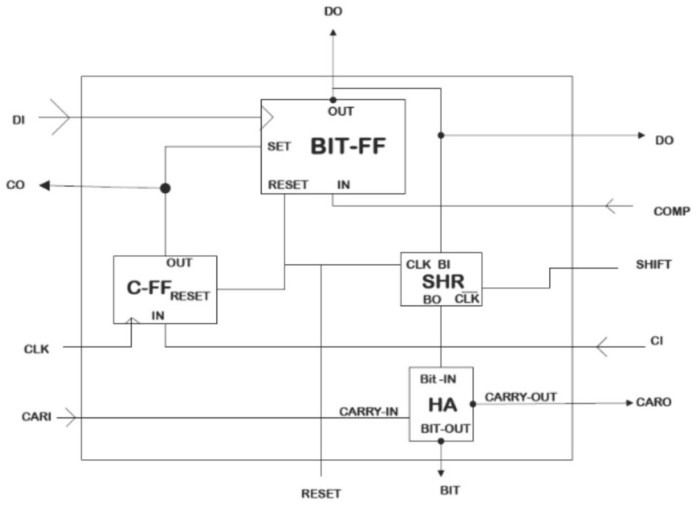

Fig. 13 The components of one of the digital blocks D0 to D14

DI is indeed the digital output of the DAC stage (n + 1), and the FF clock is the n^{th} stage's bit. CO is the CFF input of the stage (n + 1) and the CFF output of stage n. CARI is the output carry of the stage (n + 1) half-adder circuit and the input carry of the stage n half-adder circuit. DO is the digital output for stage n DAC and stage (n-1) BFF clock. CI is the CFF input of stage n and the CFF output of stage (n-1). CARO is the combined term for the input carry of the stage (n-1) half-adder circuit and the output carry of the stage n half-adder circuit. The RESET signal resets CFFs and BFFs at every stage and acts as a clock for the shift register circuit. Every stage's shift register clock is equal to SHIFT. CLK is the input clock for the CFFs at all stages.For BFFs in all stages, COMP is the comparator output and input bit. BIT represents the nth floor's output bit following error correction. In order to ensure that every bit exits at the final value, a shift register is added. The sixteenth and seventeenth CFFs, respectively, produce the SHIFT and RESET signals.

5 DAC Converter

Figure 14 depicts the DAC converter circuit used in this article. The DAC capacitors in this figure take a sample of the input voltage during the sampling cycle and hold it there. As illustrated in Fig. 15, we replace Thevenin's equivalent circuit of the less valuable part (eight bits) with it for a more straightforward analysis of this converter. This causes the digital converter to become analog. Since the capacitors in this section have binary relations, Eq. (13) states that the Thevenin's equivalent capacitator is equal to twice the largest capacitor.

Thevenin's equivalent circuit is presented in Eq. (13):

$$C_{thev} = \frac{C}{1} + \frac{C}{2} + \ldots \frac{C}{16} + \frac{C}{16} = 2C \tag{13}$$

$$C_{eq} = C_{thev} \| C_{ATT} = \frac{2C \times \frac{2C}{31}}{2C + \frac{2C}{31}} = \frac{C}{16} \tag{14}$$

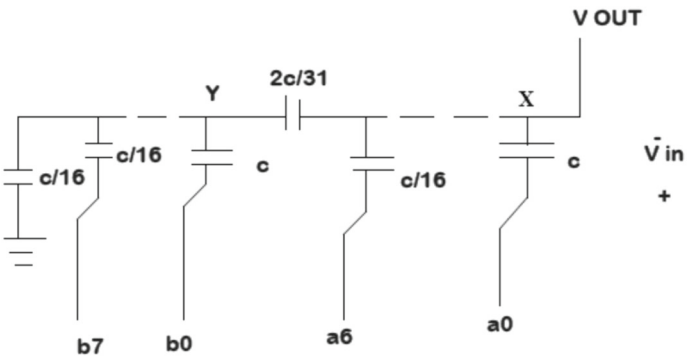

Fig. 14 DAC capacitor converter by load redistribution method and adding attenuation capacitor

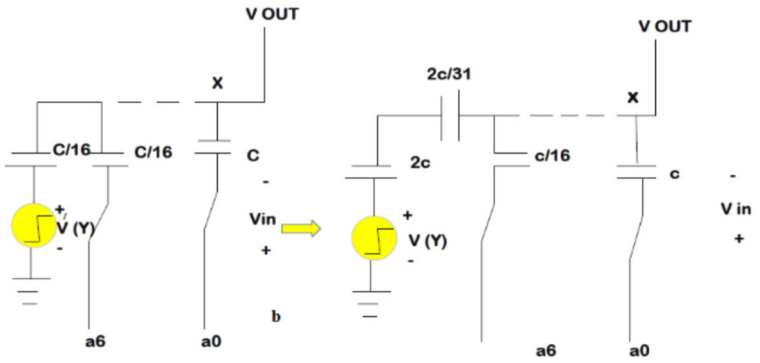

Fig. 15 **a** The 8-bit less valuable Thevenin's equivalent circuit without the effect of attenuation capacitator, **b** The 8-bit less valuable Thevenin's equivalent circuit with the effect of attenuation capacitator

Moreover, Thevenin's equivalent voltage is equal to the sum of the binary voltages minus the sampled voltage (because its polarity is negative).

$$V(Y) = b_0 2^{-1} + \ldots + b_7 2^{-7} - V_{in} \tag{15}$$

$$V_{(Y)'} = b_0 2^{-1} + \ldots + b_7 2^{-7} \tag{16}$$

Using this simplified circuit, we calculate DAC output voltage using the superposition theorem, which equals:

$$V(out) = a_0 2^{-1} + \ldots + a_5 2^{-6} + \frac{V'_{(Y)}}{32} - V_{in} \tag{17}$$

$$V(out) = a_0 2^{-1} + \ldots + a_5 2^{-6} + b_0 2^{-7} + \ldots + b_7 2^{-15} - V_{in} \tag{18}$$

The following can be obtained by calculating the equivalent capacitor of this capacitor using the attenuation capacitor connected in series with it. It is evident that the difference between the input voltage and the analog representation of the digital code of the DAC input is represented by Eq. (18). As previously mentioned, the DAC converter does more than just convert digital to analog; it also samples the analog signal input. As seen in Fig. 16, the variation in sampling pulses is related to the decrease in the charge injection effect brought about by the switches, a technique known as capacitor bottom plate sampling.

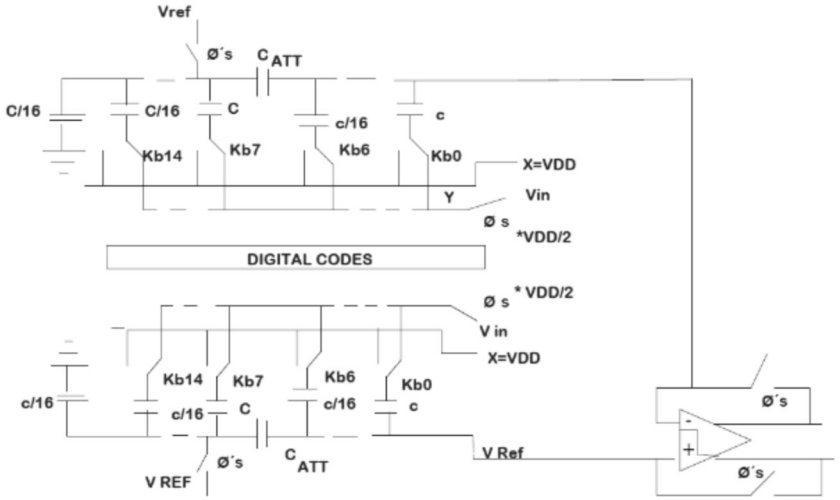

Fig. 16 ADC converter in the sampling phase

5.1 Comparator

Figure 17 shows the comparator circuit in use. There are four phases to this comparator. It eliminates the second stage offset at its output and the first, third, and fifth stage offsets at its input.

Figure 18 shows the circuit implementation of one of the comparator stages. Transistors M1 and M2, M3 and M4 form n-type and p-type differential pairs, respectively, in Fig. 18. As a result, the amplifier composed of these four transistors has a higher current-to-voltage share than conventional amplifiers. Every transistor uses a portion of the input signal to produce current at the output.Transistors M5 to M8, however, have two functions:Transistors M5 through M8 first appear as common-mode feedback and modify the output common-mode voltage if the common-mode output voltage changes.

The feedback function of transistors is examined by examining the rise in positive and negative output voltages by Δv. Transistors M7 and M8 inject less current down the path that transistors M3 and M4 take to reach the output, while transistors M5

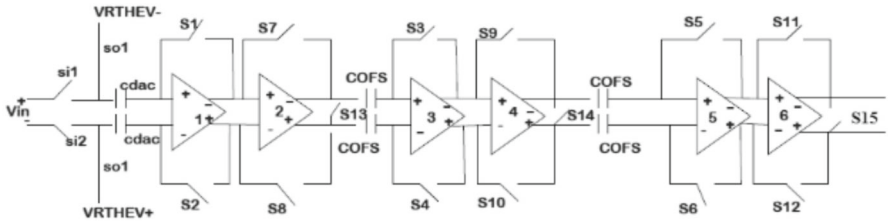

Fig. 17 Comparator structure

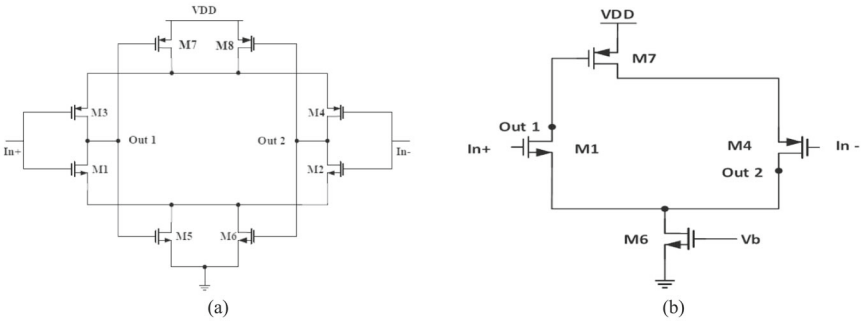

Fig. 18 The proposed comparator (**a**) and push–pull performance of transistors (**b**)

and M6 draw more current from the output through the same path as transistors M1 and M2, lowering the output voltage by nearly Δv. Two transistors M5 with M6 and M7 with M8 serve as current sources and supply the bias for n-type and p-type differential pairs, respectively. Power consumption must be decreased during the reset cycle, which ends in about half the time of the comparative cycle. Power reduction is typically achieved by adding switches to the current path that draws power from the power supply, necessitating the use of a large switch in each comparator amplifier. The next cycle sees a rapid increase in current due to the signal's arrival and the push–pull role of transistors M1 and M6 with M4 and M7, as well as M2 and M5 with M3 and M8. This expedites the process of signal detection and allows the comparator to only make errors in comparisons when the difference is at its minimum. After identifying the final bit, the error that the converter took into account can be fixed by fixing the error that the converter took into account.

5.2 Flip-flops Circuit Design

The internal circuit of one of the FFs that controls the DAC is depicted in Fig. 19. The first inverter activates and readies the data at the second inverter's input for use in the subsequent cycle when the clock reaches "0".

In order to keep data from being routed to the output and causing system disruptions (like oscillation and loop formation), the second inverter is turned off during this cycle. Furthermore, since the clock in this cycle is at zero, inverter number seven is activated. The output is reset or set, respectively, if the reset and reset reverse signals are active. This inverter is turned off in the subsequent cycle when clock "1" is activated to prevent it from using additional power as a result of interference with inverter 2. After setting the clock to "1", inverter 2 is activated and the data is sent to the output.

The output of the second inverter is connected to the output via two inverters and to the output complement through one inverter. Additionally, it passes through the sixth inverter to the data booster circuit 1. Setting and counter FFs have the same structure as DAC FFs; the only difference is that they don't boost data. The circuit needed to implement the inverters that function with the clock is shown in Fig. 20.

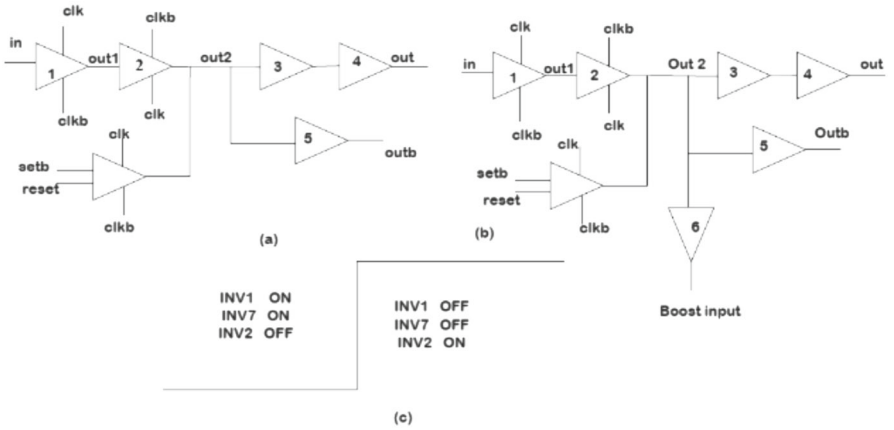

Fig. 19 a Bit flip-flop (BFF), **b** Counter flip-flop (CFF), **c** The way inverters are turned on

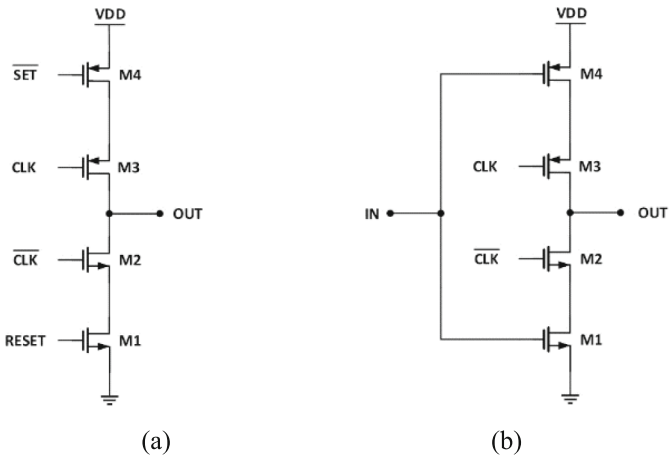

Fig. 20 a Clocked inverter related to set and reset, **b** clocked inverter

Additionally, the circuit needed to implement the set and reset the inverter is depicted in figure (a). The output path to VDD in the set and reset inverter only opens when the clock is at "0" and the set signal is at "1". Additionally, only when the clock is at "0" and reset to "1" does the output path to the ground open. Below are the findings from the suggested odulator's final simulation. All of the simulations take power supply noise into account. The output FFT for the sampling frequency of 12.5 MHz is displayed in Fig. 21.

$$\text{ENOB} = \frac{SNDR - 1.76}{6} = \frac{76 - 1.76}{6} = 12.37 \tag{19}$$

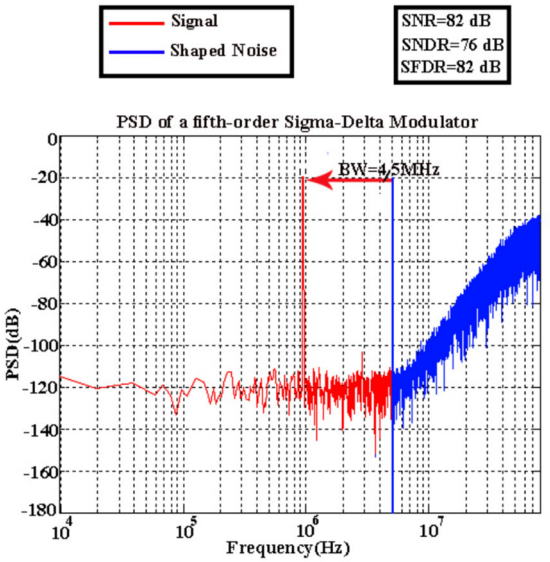

Fig. 21 The proposed converter's output FFT

6 Results of the System and Circuit Level Implementation

Table 2 displays the final outcomes attained for the suggested order-5 Sigma-Delta modulator. Thus, Figs. 22 and 23 present the stability analysis of the suggested design. The suggested modulator is constructed with an IIR noise conversion function, as can be seen in the figures. The 5-bit quantizer is stable to inputs approximately 0.65 of the feedback reference voltage and requires less output swing in its first integrator. Consequently, using Eq. (20), the noise conversion function of the suggested modulator

Table 2 designed structural results

Systematic	Specification	Circuitry
Process (μm)	0.18	0.18
Bit	15	15
SFDR (dB)	82	110
SNDR (dB)	76	103
Power (mw)	62.7	56.6
Bandwidth (MHz)	4.5	4.7
Sampling Frequency (MHz)	12.5	12.5
Power supply Voltage (v)	1.8	1.8
OSR	8	8

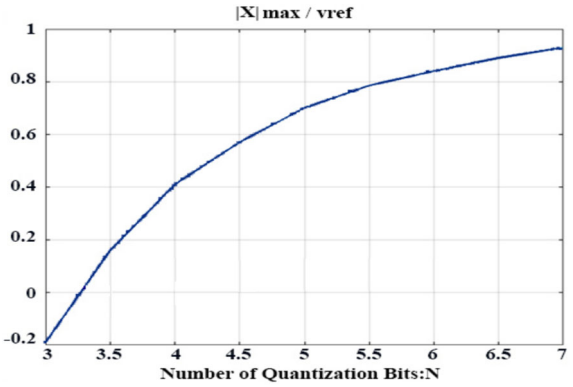

Fig. 22 Maximum input signal value in terms of N with IIR noise tansfer function

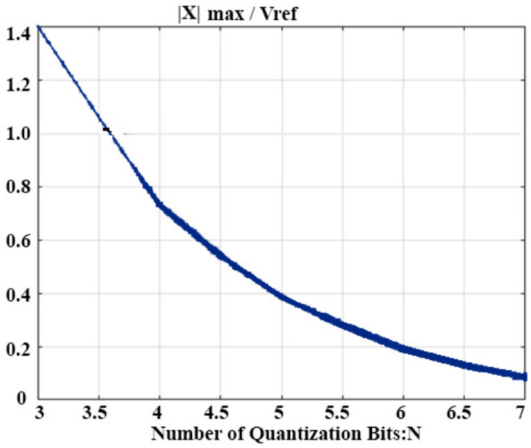

Fig. 23 The first integral input in terms of N with the IIR Noise transfer function

quantizer is chosen as an IIR filter, resulting in an accuracy of 5 bits.

$$\mathrm{NTF(z)} = \frac{\left(1-\mathrm{z}^{-1}\right)\left(1-1.875\mathrm{z}^{-1}+\mathrm{z}^{-2}\right)\left(1-1.955\mathrm{z}^{-1}+\mathrm{z}^{-2}\right)}{1-0.99866\mathrm{z}^{-1}+1.1265\mathrm{z}^{-2}-0.24248\mathrm{z}^{-3}+0.2223\mathrm{z}^{-4}+.06857\mathrm{z}^{-5}} \tag{20}$$

The results of this study were compared with those of reputable articles published in the past year in order to assess the effectiveness of the suggested modulator. Furthermore, two (FOM) were defined in accordance with Eqs. (21) and (22) to allow for a fair comparison between various designs. A comparison of the outcomes is presented in Table 3, where the better the suggested design, the smaller the FOM1.

$$FOM1 = \frac{Power}{2 \times BW \times 2^{ENOB}} \tag{21}$$

$$FOM2 = (DR)_{dB} + 10.\log(BW/Power) \tag{22}$$

Table 3 Comparison of the proposed modulator's results with other studies

No	Technology (μm)	Bit	Power supply (v)	Power consumption (mw)	Bandwidth (MHz)	SNDR (dB)	SNR (dB)	FOM1 (fj/conv.step)	FOM2 (dB)	Ref
1	0.13	5	1.5	87	20	78	81	330	153	[12]
2	013	12	1.2	40	10	72	86	488	147	[13]
3	0.09	3	1	5.8	20	65.3	65.9	96.3	161	[34]
4	0.09	6	1	18.2	30	79.4	-	38	184	[35]
5	0.13	6	1.2	11.4	15	80.4	81.7	44	174	[36]
6	0.04	4	1.1	22.8	75	65.5	66.8	98	163	[37]
7	0.18	15	1.8	56.6	4.7	103	110	18.3	170	System
8	0.18	15	1.8	59.4	4.5	76	82	21.2	161	Circuit

7 Discussion

The study presents a novel design of a Delta-Sigma Modulator (DSM) that employs an Infinite Impulse Response (IIR) filter as the Noise Transfer Function (NTF) structure to achieve low power consumption, high accuracy, and high speed. To assess the efficacy of the proposed DSM, its performance metrics are compared against several other designs documented in literature, summarized in the Table 3.

7.1 Power Consumption

One of the primary advantages of the proposed DSM design is its low power consumption. As observed in the comparison table, the power consumption of DSMs varies significantly across different technologies and designs. The proposed system (No. 7) operates at 56.6 mW, which is considerably lower than some of the higher power designs, such as the system in reference [24] (87 mW) and [3] (22.8 mW). Although there are designs with lower power consumption, such as the one in reference [4] (5.8 mW), the proposed DSM balances power consumption with other performance metrics effectively.

7.2 Signal-to-Noise-and-Distortion Ratio (SNDR) and Signal-to-Noise Ratio (SNR)

The SNDR and SNR are critical for assessing the accuracy and performance of DSMs. The proposed design exhibits an SNDR of 103 dB and an SNR of 110 dB, which are significantly higher compared to other systems. For instance, the DSM in reference [4] has an SNDR of 65.3 dB and an SNR of 65.9 dB, while the design in reference [31] shows an SNDR of 72 dB and an SNR of 86 dB. The high SNDR and SNR values of the proposed DSM indicate superior performance in terms of signal clarity and noise suppression.

7.3 Bandwidth

Bandwidth is another crucial parameter, especially for applications requiring high-speed data processing. The proposed DSM supports a bandwidth of 4.7 MHz, which is lower than some high-bandwidth designs like the system in reference [3] (75 MHz) and [32] (30 MHz). However, the proposed DSM's bandwidth is adequate for many applications and demonstrates a good balance between bandwidth and power consumption.

7.4 Figure of Merit (FOM)

Two figures of merit (FOM1 and FOM2) are used to provide a holistic assessment of the DSM performance. FOM1, measured in fJ/conversion step, and FOM2, measured in dB, offer insights into the energy efficiency and overall performance effectiveness, respectively. The proposed DSM achieves an FOM1 of 18.3 fJ/conversion step and an

FOM2 of 170 dB, which are among the best in the comparison table. This indicates that the proposed DSM is highly efficient in terms of energy consumption per conversion step and overall performance.

7.5 Comparative Analysis

The proposed DSM design demonstrates a commendable trade-off between power consumption, accuracy, speed, and overall performance. It outperforms many existing designs in terms of SNDR and SNR, which are crucial for maintaining signal integrity. While its power consumption is not the lowest, it is sufficiently low given the high SNDR and SNR values. The bandwidth, though not the highest, is adequate for numerous applications and complements the other performance metrics well.

The proposed DSM utilizing an IIR filter as the NTF structure stands out for its high SNDR and SNR, low power consumption, and competitive FOM values. These attributes make it a robust choice for applications demanding high accuracy and efficiency. While there are trade-offs, particularly in bandwidth, the overall design achieves a balanced performance that makes it a viable and attractive option compared to existing DSM designs. Future work could focus on further optimizing bandwidth without compromising the achieved gains in power efficiency and signal quality.

8 Conclusion

The designs and simulation of a Sigma Delta modulator with high speed, accuracy, and low power consumption were covered in this article. There is an integrator and an IIR filter in the suggested design. It was found that the two integrators and IIR filter that are positioned before and after the IIR filter in basic designs use a significant amount of power. The second set of modulators in the proposed design speed things up by using the dual sampling approach, and there is only one integrator. In both scenarios, the NTF equation is thought of as a FIR filter.IIR filters and integrators are used in the final design. In order to improve the stability of the Sigma Delta modulator, we switched the NTF conversion function from the FIR to the IIR mode. When compared to similar designs, the designs produced results that were acceptable when implemented as both a system and a circuit. This structure is most commonly used in ADSL2 and ADSL2 + systems.

Data availability Available upon request.

Declarations

Conflict of interest None.

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