A 12-Bit, 300-MS/s Single-Channel Pipelined-SAR ADC With an Open-Loop MDAC

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***Abstract*— Compared to pipelined analog-to-digital converters (ADCs), pipelined- successive approximation register (SAR) ADCs have been actively explored for better energy efficiency in recent years. Nonetheless, the pipelined-SAR architecture inherently limits the sampling speed of the ADC due to the slow operation of the first SAR ADC, which becomes an increasingly important limitation with the recent expansion of high-speed applications. In this paper, we introduce our new design of a pipelined-SAR ADC to enable faster speed. New loop-unrolled architecture with the split capacitor is used for the first SAR ADC to improve the speed. A resistive open-loop multiplying digital-to-analog converter with a new calibration scheme is designed to reduce the power consumption at high speed. As a result, the 65-nm design can achieve 300-MS/s sampling rate with a single channel. It is among the fastest pipelined-SAR ADC design so far. The peak signal-to-noise-and-distortion ratio is 63.6 dB with a 10-MHz input. It consumes 12.5-mW power from a 1.2-V supply to achieve a power efficiency of 34 fJ/conversion-step.**

***Index Terms*— Calibration technique, high-speed analog-to-digital converter (ADC), loop-unrolled successive approximation register (SAR), open-loop multiplying digital-to-analog converter (MDAC), pipelined-SAR ADC.**

I. Introduction

HIGH-SPEED high-precision analog-to-digital converters (ADCs) are widely used in various fields, such as image processing, information storage, and wireless communication [1]–[3]. Pipelined ADC is the primary candidate for these applications. Time interleaving [4] is actively researched to achieve speed higher than single-channel ADCs. Power consumption is a major limiting factor in these systems. Various techniques, such as OPAMP sharing [5]–[7] and multi-bit multiplying digital-to-analog converter (MDAC) [8], have been actively explored to reduce the pipelined ADC power by reducing the number of OPAMPs in the pipeline. More recently, pipelined-successive approximation register (SAR) ADCs have been actively researched to combine low-powered SAR ADC into the pipeline [9]–[11]. By using SAR ADCs as the sub-ADCs in the pipeline, a high-resolution pipelined ADC can be designed with only two stages. Hence, only one OPAMP is needed for a whole pipelined-SAR ADC, which could further reduce the pipelined ADC power.

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With a better power efficiency, pipelined-SAR ADCs have been explored for high-speed applications. However, the speed of pipelined-SAR ADCs is limited. The critical issue is that the quantization time of a 6-bit SAR ADC is much longer than the conventional flash sub-ADCs. This additional delay will erode the time available for either sampling or amplification. In [9], the sampling time was shrunk to accommodate this additional SAR ADC bit-cycling time. Improvement has also been made on the speed of the SAR ADC. In [12], a loop-unrolled asynchronous SAR ADC was used to eliminate the SAR logic delay from the critical path. The bit-cycling period was shortened. In this loop-unrolled architecture, N comparators were used to resolve N-bit resolution. The individual comparator offset requires calibration. As mentioned in [13], the input common-mode voltage of comparators would drop during bit cycles which results in offset drifts. Hence, the foreground offset calibration in [12] cannot address the offset issue effectively.

The power consumption of a pipelined-SAR ADC is dominated by the OPAMP in the conventional closed-loop MDAC. It has been shown in [8] that a high-resolution first stage leads to the demand of large OPAMP gain-bandwidth (GBW) product and high OPAMP dc gain. In recent sub-micrometer CMOS processes, it needs large power consumption to push up the non-dominant poles while maintaining reasonably high gain in an OPAMP. In [14] and [15], open-loop MDAC was used to save the power. However, the process variation and non-linearity are the major bottlenecks for open-loop MDACs. Complicated non-linear gain calibration was needed [15], which limits the application of open-loop MDACs. In [12] and [16]–[18], constant-slewing dynamic amplifiers were used in an open-loop MDAC. This architecture further reduces power, but the MDAC gain is not only sensitive to the process variation but also to any change in the transient settling process, such as clock jitter and supply spikes. In [19], a passive residue transfer technique was introduced to remove the MDAC completely. Hence, there is no gain for the residual voltage, which demands very stringent noise and offset control on the backend.

In this paper, our focus is on the speed of pipelined-SAR ADCs. We analyzed the speed limitation of the pipelined-SAR architecture, and found that, for sampling speed beyond 200 MS/s, the SAR ADC generally limits the ADC sampling speed in the 65-nm CMOS processes. In order to design a pipelined-SAR ADC with higher speed, we developed a new asynchronous loop-unrolled SAR ADC with split capacitor to maximize the speed of the SAR ADC. To reduce the gain sensitivity to static process voltage temperature (PVT) spread

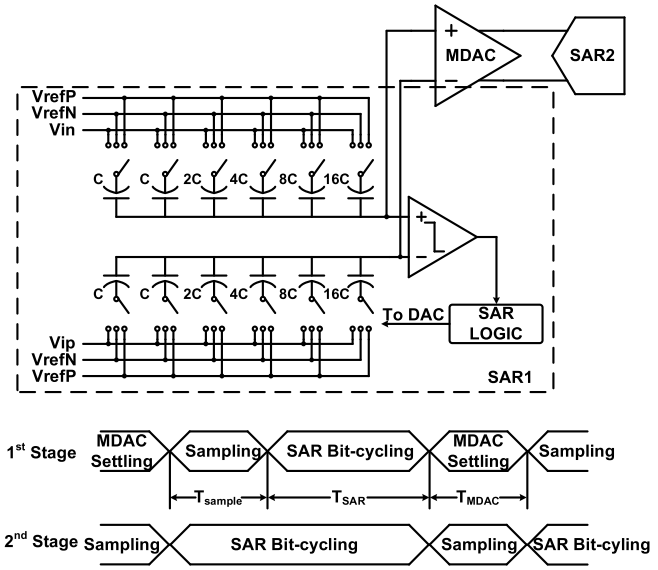

Fig. 1. Conventional pipelined-SAR ADC architecture.

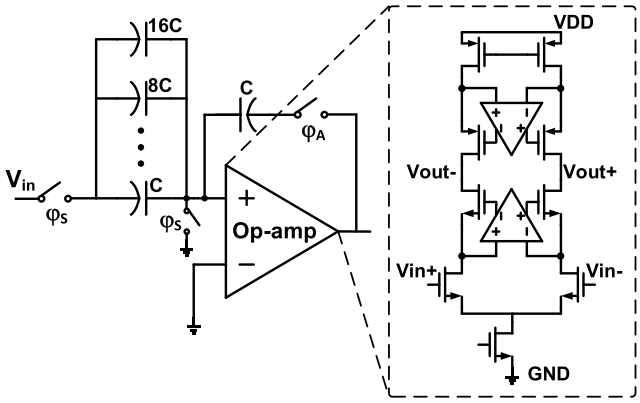

Fig. 2. Conventional closed-loop MDAC.

and dynamic interferences, we also designed a resistive open-loop MDAC with a new calibration scheme using digital-to-analog converter (DAC) gain to compensate the MDAC gain variation. This new calibration architecture has good robustness in practical designs.

II. Fundamentals of Pipelined-SAR ADC

A pipelined-SAR ADC is essentially a two-stage pipelined ADC as shown in Fig. 1 with its typical operation timing diagram. To resolve 12 bits, the first stage of the ADC resolves 6 bits, while the second stage resolves 7 bits with 1 bit overlap for redundancy. To enable the 6-/7-bit quantization, instead of the conventional flash sub-ADCs, SAR ADCs are used for less power consumption and less design complexity. In this ADC, the MDAC amplifies the residue voltage by $2^5 = 32\times$. As MDAC and sub-ADC share one sampling path, a dedicated S/H stage is not needed.

As the analysis in [9] shows the high-resolution MDAC that shortens the pipeline so as to reduce the overall MDAC power consumption. The pipelined-SAR architecture also reduces the power consumption of sub-ADCs. Therefore, the overall power consumption of a pipelined-SAR ADC could be reduced compared to a conventional pipelined ADC implementation with the same specifications.

Nonetheless, the SAR ADC adds new constraints to the pipeline operation timing. As shown in the timing diagram in Fig. 1, the slow SAR bit-cycling process adds another phase to the operation of the pipeline. Hence, the critical path of the ADC quantization cycle is

$$T_{\text{period}} = T_{\text{sample}} + T_{\text{SAR}} + T_{\text{MDAC}}. \tag{1}$$

A. MDAC Speed Limitation

The MDAC settling time is proportional to the slew and linear settling times. For a conventional closed-loop MDAC as shown in Fig. 2, its settling time can be shortened with a well-studied tradeoff of its power. With common assumptions that the slew time equals the linear settling time and the OPAMP in the MDAC has 70° phase margin, it can be derived similarly as in [20] that

$$T_{\text{MDAC}} = 14\tau_{\text{MDAC}} = \frac{7}{\pi f_{\text{CL}}}. \tag{2}$$

where f_{CL} is the closed-loop bandwidth of the OPAMP. To maintain the stability, the OPAMP's non-dominant poles should locate at frequencies higher than $2f_{\text{CL}}$ to leave a phase margin of 60°. For a closed-loop MDAC, the OPAMP needs high gain. In recent sub-micrometer CMOS processes, usually two-stage or gain-boosting stages are used to maintain a reasonably high gain. The architecture is complicated with a number of poles. Take a four-pole system as an example. The highest possible f_{CL} is $1/6f_T$ when the three non-dominant poles are close to f_{T}.

In our 65-nm CMOS process, to enable 70-dB gain, f_{T} of the output stage is about 40 GHz at the slowest temperature corner (85 °C, SS corner). Hence, the maximum achievable OPAMP closed-loop bandwidth is about 6 GHz. The shortest achievable τ_{MDAC} is 14 ps. Hence, the shortest possible MDAC settling time in our process is about 200 ps. Nonetheless, to push all the non-dominant poles close to f_{T} and to achieve 70-dB gain demands tremendous power from the OPAMP.

B. SAR Speed Limitation

To shorten the critical path of the SAR ADC, asynchronous bit cycling is normally adopted. The critical path of each bit cycle is consists of three delays as

$$T_{\text{bit}} = t_{\text{DAC}} + t_{\text{latch}} + t_{\text{logic}} \tag{3}$$

where t_{DAC} is the DAC capacitor array settling time, t_{latch} is the latch delay, and t_{logic} is the delay of the SAR logic. In a high-speed design, as mentioned in [21], the SAR logic delay can occupy up to 75% of 1-bit cycle. To shorten the bit cycle, multiple comparators can be used in a loop-unrolled SAR ADC as shown in Fig. 3. One comparator is used to decide each bit. The comparator output directly controls the switch of one binary capacitor. In parallel, the comparator

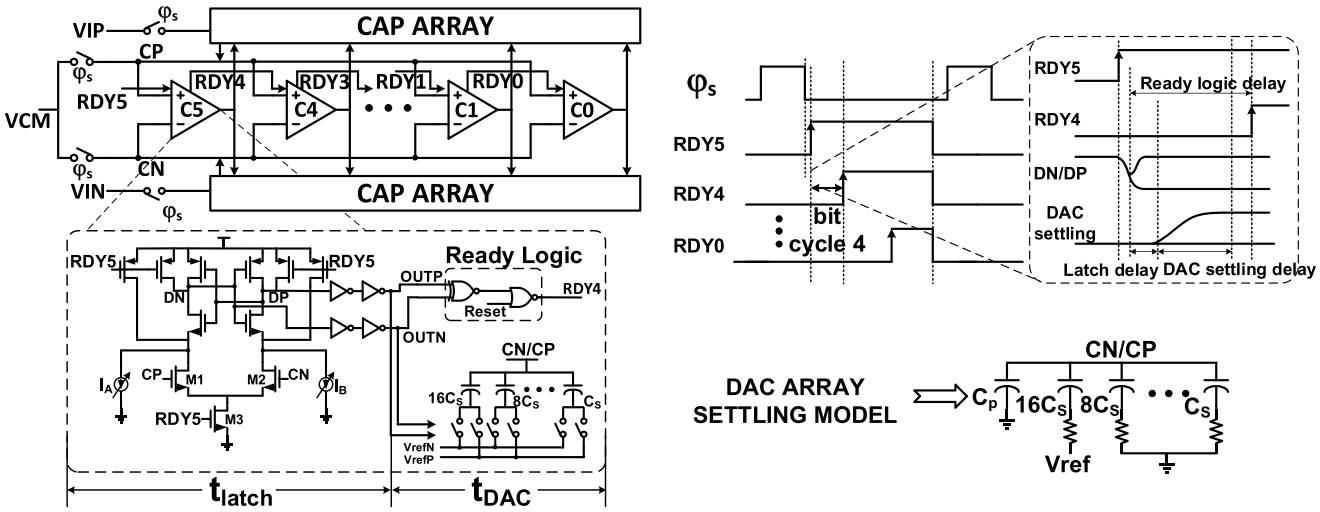

Fig. 3. Loop-unrolled SAR ADC architecture.

output generates a ready signal to trigger the next comparator through a simple ready logic. With this architecture, the critical path is reduced to

$$T_{\text{bit}} = t_{\text{DAC}} + t_{\text{latch}}. \tag{4}$$

For an N-bit SAR ADC, the DAC should be settled within 1/2 LSB at each conversion step. Then, the settling time can be derived similarly as in [20] as

$$t_{\text{DAC}} \geq \tau_{\text{DAC}} \ln 2^{N+1} \tag{5}$$

where τ_{DAC} is the DAC time constant depending on the capacitive load and the ON-resistance of switches. Although this high-speed SAR architecture eliminates the logic delay, the multiple comparators increase the parasitic capacitance at the top-plate node (CN/CP). On the other hand, the ON-resistance reduces by increasing the switch width, which leads to higher switch capacitive load. Consequently, it needs larger buffer and comparator to keep the latch delay small, which in turn loads the top-plate node. In our analysis, we set a practical limit on the comparator-led parasitic capacitance at the top-plate node to the highest weighted capacitor size, which is 64 fF in our design. With this limit, in our process, the largest possible PMOS switch connecting to V_{refP} is 16 μ m/60 nm, which has an ON-resistance of 80 Ω at the slowest corner. Based on the equivalent DAC settling model in Fig. 3, it can be calculated that the DAC settling time is 75 ps.

As mentioned in [22], the latch delay can be calculated as

$$t_{\text{latch}} = t_0 + \tau_{\text{latch}} \ln \frac{V_{\text{FS}}}{V_{\text{in}}} + t_{\text{buffer}} \tag{6}$$

where t_0 is the initial slew time which can be derived as

$$t_0 = \frac{2C_{\text{L}} V_{\text{thp}}}{I_0} \tag{7}$$

where I_0 is the bias current, V_{thp} is the threshold voltage of the PMOS, and C_{L} is the loading of the latch. As the input transistor size is limited by the parasitic capacitance constraint, the maximum I_0 is 300 μA in our design. The latch load in Fig. 3 includes four gate capacitors and three drain-bulk capacitors, which is 10 fF in our process. So, the minimum t_0 is 24 ps.

In (6), τ_{latch} is the latch time constant. For the latch in Fig. 3, the minimum is about $2\tau_{\text{ft}}$, which is about 8 ps. V_{FS} is the full logic swing. V_{in} is the input voltage to the latch. For every bit cycle in the asynchronous SAR ADC, the best case with the minimum regeneration time is simply 2^5 LSB, 2^4 LSB, 2^3 LSB, 2^2 LSB, 2 LSB, and LSB [23]. t_{buffer} is the buffer delay in Fig. 3. Using typical buffers with fan out of 3, two buffer stages are needed to drive the 90-fF load from the switch and the ready logic. In our process, the minimum buffer delay is 20 ps. Hence, the minimum two-stage buffer delay is 40 ps.

Hence, the minimum bit-cycling time of the 6-bit SAR in Fig. 3 can be calculated following (4) as:

$$T_{\text{SAR}} = 6 \times 75 + \sum_{i=1}^{6} (24 + 8 \ln \frac{V_{\text{FS}}}{2^{6-i}\text{LSB}} + 40) \text{ ps}.$$

It is around 1 ns at the worst corner in our 65-nm process, which is much slower compared to the MDAC settling time.

Most recently high-speed pipelined-SAR work focused on speeding up the MDAC. However, if the SAR ADC speed is not increased accordingly, it can easily become the dominant delay in a pipelined-SAR ADC. In this paper, we developed circuit techniques to improve the speed of the SAR ADC and a reliable open-loop MDAC to reduce the MDAC power.

III. Circuit Implementation

Our ADC design targets to achieve 12-bit resolution at 300 MS/s with a differential input signal range of 1.6 V. To reduce the critical delay in SAR ADC, similar to [24], we minimized the capacitor size in the SAR ADC by separating the sampling capacitor arrays of the MDAC and the SAR ADC as shown in Fig. 4. The MDAC capacitor array is designed with the 12-bit sampling noise requirement (1.28 pF). However, SAR1 only needs to resolve 6 bits. Hence, a much smaller sampling capacitor can be used. Indeed, the capacitor size is dominated by the matching requirement instead of the noise requirement (128 fF). Method-of-moments (MoM)

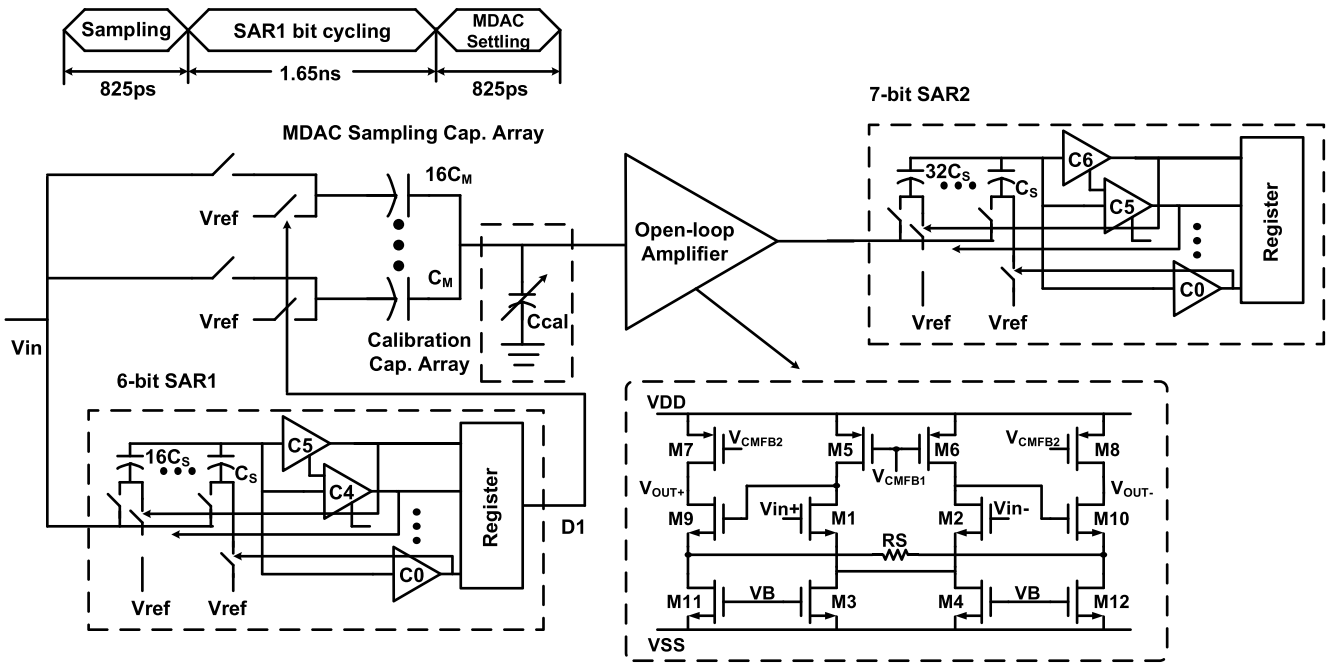

Fig. 4. New pipelined-SAR ADC.

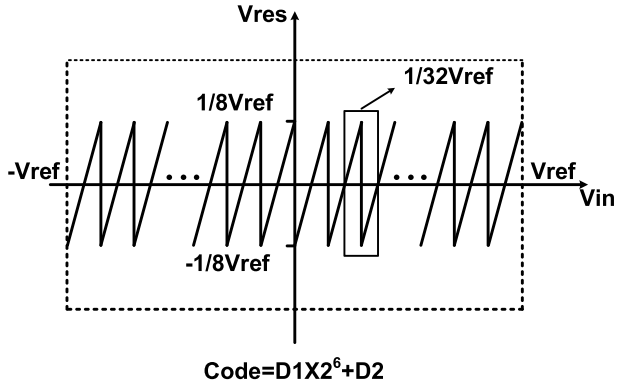

Fig. 5. Ideal transfer function of the MDAC in our pipelined-SAR.

capacitors are used. Although different capacitors were used for MDAC and SAR1 in [25], the two capacitor arrays are connected during the bit cycling. Hence, SAR1 still need to drive both capacitor arrays in [25].

Nonetheless, by separating the sampling capacitors, the mismatch of time constants between the two sampling paths could possibly lead to sampling offset [26]. The MDAC is designed with the transfer function in Fig. 5 to include 1-bit redundancy, which can tolerate up to 0.5 LSB (12.5 mV) mismatch between the two sampling paths. With the size of the capacitors and switches we used, it is verified that the mismatch of the two paths can be less than this tolerance reliably through Monte Carlo simulations. This is also verified by measurements. Through Spectre simulations, it can be found that the tolerance to clock skew between the two channels for the 150-MHz Nyquist signal is 16 ps [27].

SAR1 resolves 6 bits with an LSB size of 25 mV. With the 6-bit code from SAR1 (D1), an open-loop MDAC amplifies the residual with a gain of 8 to suppress the output signal range so as to reduce the non-linearity of the open-loop amplifier. The signal range to SAR2 is ±200 mV. It resolves this amplified residual with 7-bit resolution. Hence, the LSB size of SAR2 is 3.125 mV. As the range of a SAR1 code includes 64 SAR2 codes, the input-referred digital code can be calculated by D1 × 64 + D2, which creates 1-bit redundancy.

The sample period of the ADC is 3.3 ns. Its three operation phases are listed in Fig. 4.

A. High-Speed SAR ADC Design

In a typical bottom-plate sampled SAR ADC, a common-mode voltage V_{CMO}, which is the common-mode voltage of V_{refP} and V_{refN}, is needed at the bottom plates [28]. For high-speed operation, this V_{CMO} unfavorably increases the ON-resistance of bottom-plate switches so as to cause longer DAC settling. We developed a split-capacitor array as shown in Fig. 6 to eliminate V_{CMO}. The capacitor connected to V_{CMO} is split into two identical capacitors with one connected to V_{refP} and the other connected to V_{refN}, as shown in Fig. 6(c). In this way, single-transistor switch could be used. As shown in Fig. 6(a), the MSB capacitor $16C_{\mathrm{S}}$ is split into two $8C_{\mathrm{S}}$ capacitors. All capacitors split except the LSB capacitor C_{S}. The logic circuits controlling V_{refP} and V_{refN} switches for common-mode balancing are shown in Fig. 6(b). After the sampling period ϕ_S and before the bit cycling, the RDY signal for all comparators are low, so split capacitors in Fig. 6(c) are connected to V_{refP} and V_{refN} by CM_P<N > and CM_N<N > signals separately. When the bit cycle starts, CM<N> signals turn off and the split capacitors are controlled simultaneously by the conventional bit cycle logic. With the split-capacitor array, settling time of the SAR capacitor array can be reliably limited to 80 ps in our design process, which reduces the

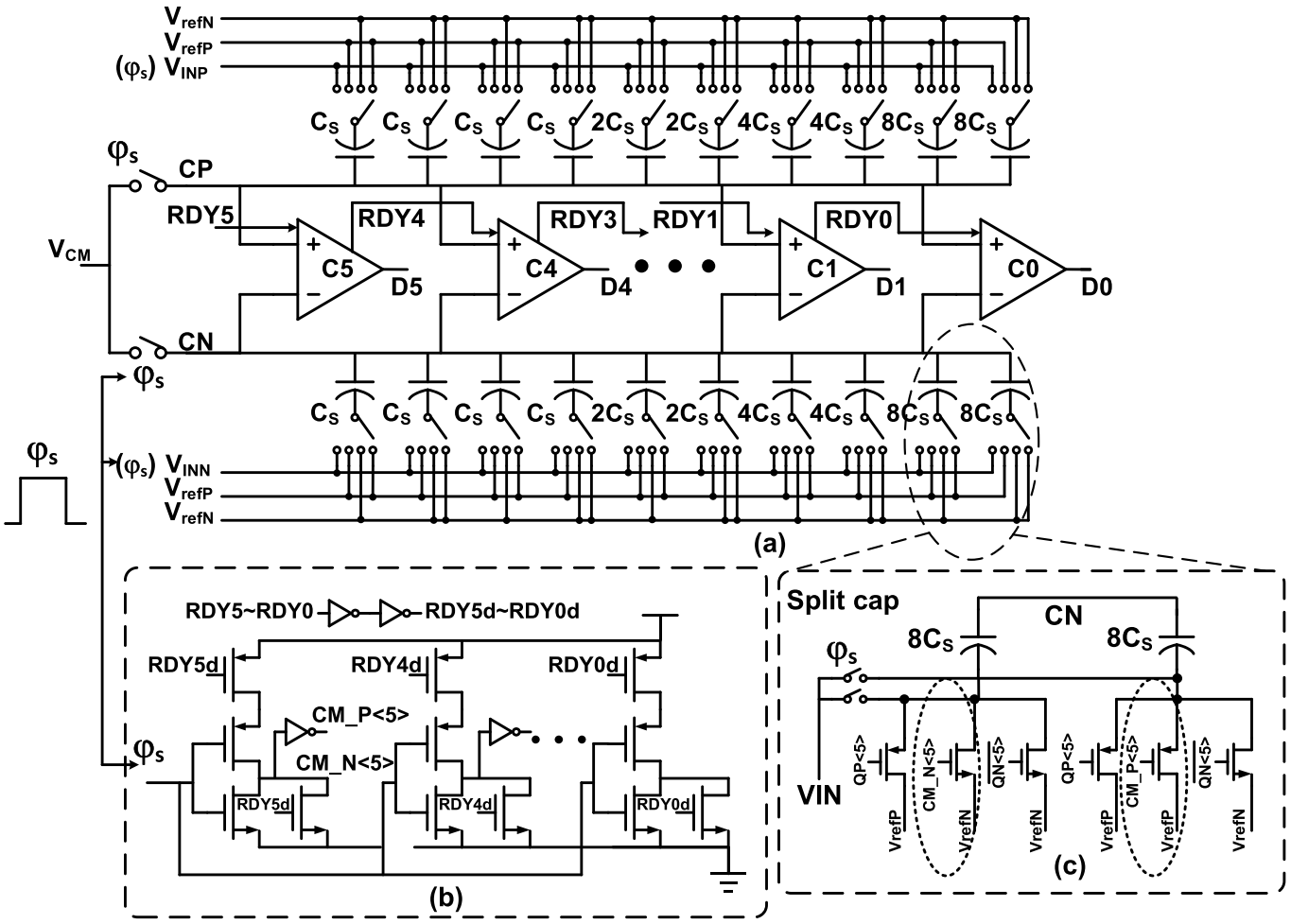

Fig. 6. First SAR ADC with split cap array.

settling time by about 60% compared to the capacitor array using the V_{CMO} switch with the same switch size.

Following the design methodology in Section II, the input pair and the biasing current of comparators are sized to have its input capacitance, at the most, equal the most significant capacitor. The regenerative pair is sized to have τ_{latch} to be 10 ps.

As shown in Fig. 1, the bit-cycling time of SAR2 is not in the critical path. Therefore, SAR2 can have smaller switches with less capacitive parasitics. Nonetheless, as SAR2 has a smaller LSB, it is designed with a larger latch to reduce the metastable zone of comparators in SAR2.

B. Open-Loop MDAC Design

To avoid the additional frequency limitation from non-dominant poles so as to reduce the power, an open-loop MDAC is adopted in our design. To enable robustness against transient non-idealities, resistive open-loop amplifier is selected. Without the stability constraint, the bandwidth of the open-loop amplifier is simply determined by *RC* at the output node. In our pipelined-SAR ADC, the available time for the MDAC settling is 0.8 ns, which requires a time constant of 0.15 ns or 1.1-GHz bandwidth from the amplifier. Considering the slew time, the amplifier is designed with 2-GHz bandwidth.

A major challenge of the open-loop MDAC design is its non-linearity over the wide signal range. The simulations show that the MDAC in our pipelined-SAR ADC needs about −50-dB total harmonic distortion (THD) for the 7-bit SAR2. The normal differential input signal range to the MDAC is 25 mV. Nonetheless, the mismatch between the MDAC sampling path and the SAR ADC sampling path could double the maximum MDAC input signal to 50 mV. Instead of amplifying the signal to the full-scale range, our MDAC is designed to amplify the signal to 1/4 of the signal range. Hence, the MDAC's gain is 8 instead of 32, which helps to relax the MDAC linearity design.

A two-stage open-loop amplifier as shown in Fig. 4 is implemented for the MDAC. The gain is slightly over designed to 10. The first stage is designed for a higher gain of 5 as the output signal swing is smaller compared to the second stage. The simulation shows that, if the second pole is 3 times of the first pole, the settling time is increased by 50 ps compared to a single-pole system. So, a 6-GHz bandwidth is designed for stage 1. As the input capacitance of stage 2 is small (25 fF), a larger output resistance (500 Ω) can be allowed from stage 1. Hence, stage 1 is designed with an input transconductance of 10 mS for a gain of 5. Within the ±25-mV input range, Monte Carlo simulation shows that stage 1 can reliably achieve THD less than −62 dB. The second stage is designed with a

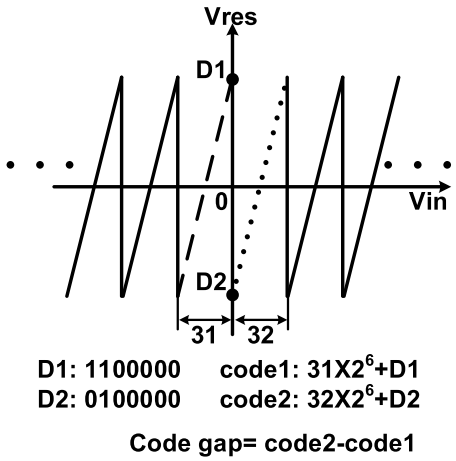

Fig. 7. Gain calibration scheme.

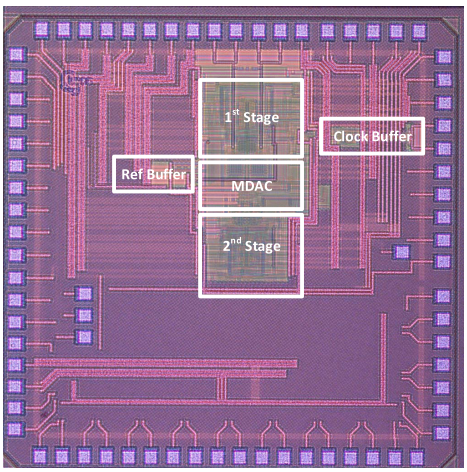

Fig. 8. Die phototograph.

gain of 2. With 250-fF loading, the output resistance of stage 2 is less than 300 Ω. Hence, the input trans-conductance of stage 2 should be larger than 6.67 mS. Nonetheless, the input signal to stage 2 is ±125 mV. The simulation shows that the amplifier linearity cannot achieve −50 dB with this wide signal range. Hence, resistive source degeneration is used to improve the linearity. With the degeneration, Monte Carlo simulation shows that stage 2 can reliably achieve THD lower than −54 dB.

C. Open-Loop MDAC Calibration

Another major challenge of open-loop MDAC design is the gain accuracy due to PVT spread. With the MDAC transfer function as shown in Fig. 5, simulations show that the MDAC gain error should be less than 0.2% or 2% to enable ADC THD lower than −80 dB. To enable this accuracy, a gain error compensation scheme is designed in our open-loop MDAC as shown in Fig. 4. The overall MDAC gain is the product of gains of the DAC array and the two-stage amplifier as shown in the following equation:

$$A_{\text{overall}} = \frac{C_M}{C_{\text{cal}} + C_M} \cdot A_{\text{OPAMP}}. \tag{8}$$

By tuning the calibration capacitor size, the gain of the DAC array can be adjusted to compensate for the PVT spread of the open-loop amplifier. A 5-bit accuracy is designed for the calibration capacitor to control the MDAC gain error.

Based on our new calibration architecture, a self-calibration process is designed to measure the MDAC gain error. The principle can be explained with Fig. 7. During calibration, the input of the pipelined-SAR ADC is shorted. The zero input is quantized twice. In the first quantization, 31 is fed to the DAC. Hence, the MDAC amplifies according to the dashed line in Fig. 7. In the second quantization, 32 is fed to the DAC. The MDAC amplifies according to the dotted line in Fig. 7. The difference between the two codes after digital error correction is the code gap. By tuning the calibration capacitor, the code gap can be tuned into zero, and then the gain error is canceled. This calibration procedure can run periodically to track the slow variation of the temperature and the voltage supply.

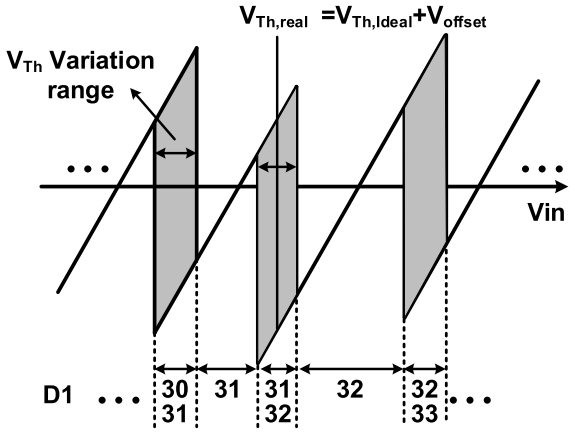

Fig. 9. Reconstructed transfer function form histogram data.

IV. Measurements and Analysis

The ADC is designed and fabricated in a 65-nm CMOS process. The micrograph of the pipelined-SAR ADC chip is shown in Fig. 8. The active area is of 0.5 mm^{2}excluding the low-voltage differential signaling (LVDS) output and driver. The ADC chip operates at 300 MS/s. A 1.2-GHz sinusoidal wave was converted to differential by a transformer and was sent to the chip to generate the 25% duty ratio 300-MS/s sampling clock. The output codes were captured with a logic analyzer.

SAR1 was tested with the histogram method. Its differential nonlinearity (DNL) is less than 0.23 LSB, and integral non-linearity (INL) is less than 0.18 LSB. With the redundancy in the pipeline, this non-linearity is sufficient for the pipeline operation. The offset of SAR1 threshold voltages determines the offset of thresholds in MDAC's transfer function. This offset is due to the mismatch in SAR1 and the mismatch between the sampling paths of SAR1 and the MDAC. With the ADC histogram data, the MDAC transfer function, similar as Fig. 9, can be generated. Between two major codes, there is a region of mixed codes due to noise from SAR1. The middle of this region is the essential threshold voltage between the two codes. The measured offset of the thresholds is listed in Fig. 10(a). The measured noise range is shown in Fig. 10(b). It can be seen that the offset and noise error are both well within the pipeline tolerance.

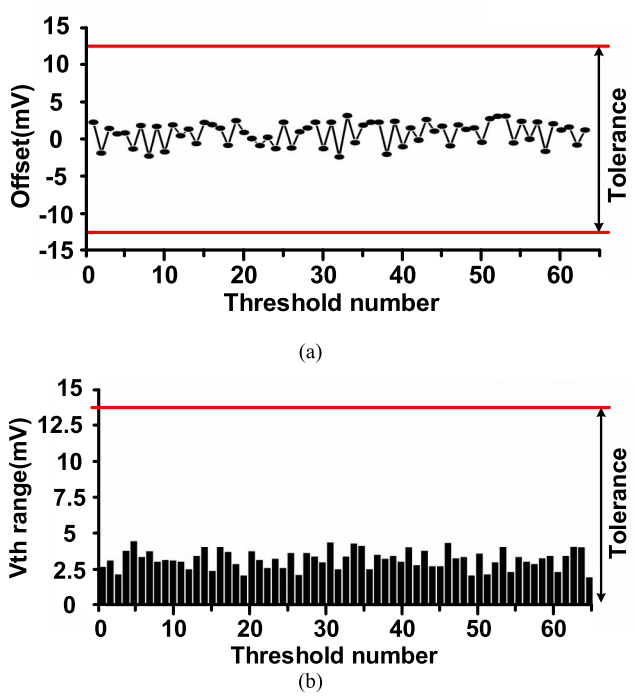

Fig. 10. (a) Threshold offsets. (b) Noise around the thresholds.

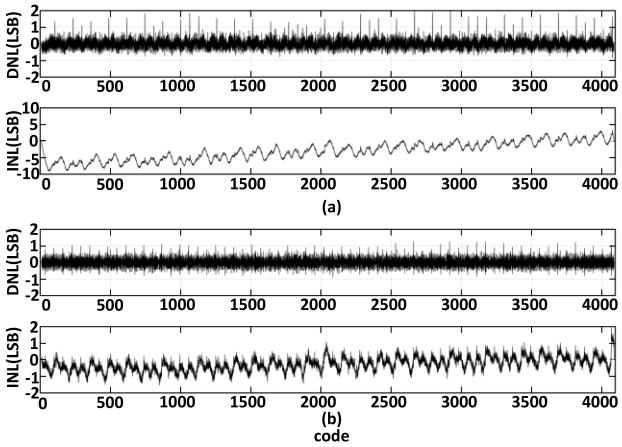

Fig. 11. DNL and INL. (a) Before calibration. (b) After calibration.

The ADC was measured for its DNL and INL with the histogram method before and after the MDAC gain calibrations. The results are shown in Fig. 11. Without calibration, the overall DNL is −0.88/2.2 LSB, while the INL is −9.01/3.54 LSB. With MDAC gain calibration enabled, the DNL is reduced to −0.9/1.25 LSB and the INL is reduced to −1.55/1.96 LSB. The ADC was also tested with high-speed sinusoidal input signals for its dynamic performance before and after the MDAC gain calibration. With a 10-MHz, 1.6-Vp–p signal, the ADC output spectrum with 20k-pt fast Fourier transform (FFT) before and after calibrations is shown in Fig. 12. Before calibration, the ADC has −58.2-dB THD, and 48.1-dB signal-to-noise-and-distortion ratio (SNDR), which is equivalent to 7.7-bit effective number of bits (ENOB). After calibration, the ADC has −76.4-dB THD, and 63.55-dB SNDR, which is equivalent to 10.26-bit ENOB. As the THD is much smaller than SNDR, the ADC SNDR is dominated by noise. The frequency of the input signal is increased up to the Nyquist frequency of 150 MHz. Fig. 13 shows the dynamic performance versus the input frequency.

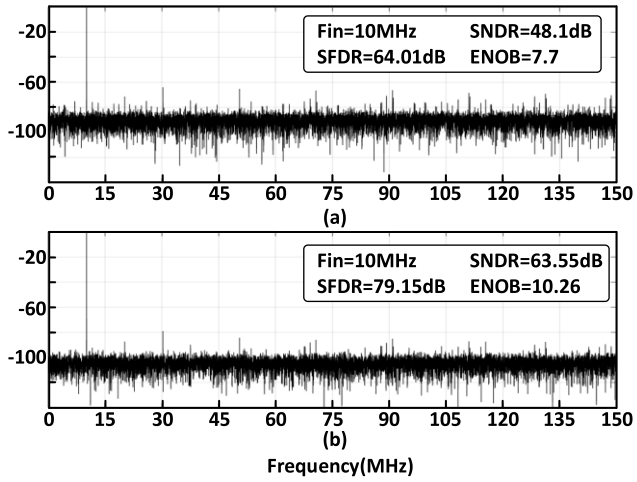

Fig. 12. FFT spectrum. (a) Before calibration. (b) After calibration.

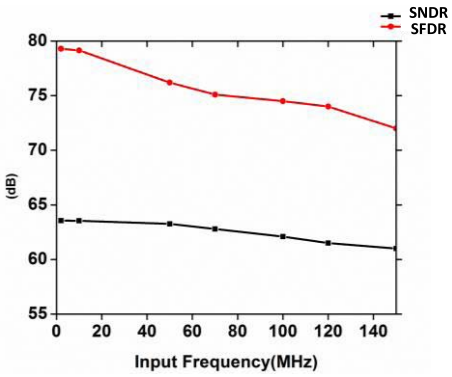

Fig. 13. Dynamic performance measurement at different input frequencies.

To test the robustness of the ADC architecture under PVT spread, the ADC chip is tested with different supply voltages. With the supply voltage increases to 1.25 V, SNDR of the calibrated chip drops to 62.5 dB. When the supply voltage drops 1.15 V, the SNDR drops 61.2 dB. After running the calibration procedure again with both supplies, SNDR of the chip increases back to 63.95 and 63.11 dB, respectively. It can be calculated from the calibration results that the MDAC gain is around 20.26, 20.41, and 20.55 dB with supplies at 1.15 1.2, and 1.25 V, respectively. One more ADC chip was tested. Before calibration, the SNDR of the second chip is 50.38 dB. After calibration, the SNDR is improved to 63.87 dB. Limited by equipment, the temperature variation cannot be tested. From simulations, the MDAC gain is 19.91 dB at 85 °C and 20.78 dB at 0 °C. This variation range is still within the compensation range of the calibration capacitors.

The temporal noise of the ADC is measured by shorting the ADC input. The measured temporal noise is 0.86 LSB_{rms}. This is consistent with the SNR measurement from the FFT test.

Running at 300 MS/s, the ADC core power consumption is 12.5 mW. The reference buffer, clock buffer, and LVDS output buffer power are not included. The power breakdown is plotted in Fig. 14. The MDAC consumes most of the power (41%). The Walden figure-of-merit (FoM) of the ADC is 34 fJ/conversion-step. SAR2 consumes more power than

TABLE I
BENCHMARK DESIGN PERFORMANCE COMPARISON

	[30]JSSC'15	[31]ESSCIRC'17	[9]JSSC'11	[32]JSSC'15	[12]JSSC'12	[17]JSSC'17	[24]CICC'14	[18]JSSC'18	This work
Architecture	Pipelined Close-loop	Pipelined Open-loop	Pipelined-SAR Close-loop	Pipelined-SAR Close-loop	Pipelined-SAR Open-loop	Pipelined-SAR Open-loop	Pipelined-SAR Open-loop	Pipelined-SAR Open-loop	Pipelined-SAR Open-loop
Interleaving	No	No	No	No	2X	No	No	2X	No
Process	65nm	28nm	65nm	40nm	40nm	65nm	65nm	16nm	65nm
fs(S/s)	250M	280M	50M	160M	250M	330M	160M	300M	300M
Resolution	12	12	12	12	11	12	13	12	12
Power(mW)	49.7	13	3.5	4.96	1.7	6.23	11.1	3.6	12.5
SNDR(dB)	67	64	66	65.3	58.65	67.7	68.3	69.18	63.55
FoM(fJ)	108.5	35.8	52	20.6	7	15.4*	32.6	5.1	34
Area(mm^2)	0.59	0.22	0.16	0.042	0.066	0.08	0.09	0.11	0.5

* is the FoM at Nyquist input

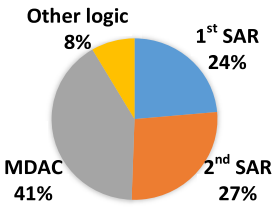

Fig. 14. Power-consumption breakdown of the ADC.

SAR1 because the reduced MDAC output range leads a smaller LSB size for SAR2. However, this range reduction enables the resistive open-loop MDAC with sufficient linearity for 12-bit resolution. The open-loop MDAC reduces the ADC power significantly. As the MDAC power still dominates in our design, this power tradeoff is beneficial.

The performance of our pipelined-SAR chip is compared with a list of benchmark designs shown in Table I. References [30] and [31] are recent pipelined ADC designs with similar speed and resolution to our design. They showed higher FoM as expected. The rest of benchmarks in Table I included all recently reported pipelined-SAR designs. Compared to these designs, our design using the new loop-unrolled split-capacitor architecture in SAR1 achieves the fastest speed except [17]. Lee [9], Martens *et al.* [18], and Zhou *et al.* [32] used conventional SAR ADC. Verbruggen *et al.* [12] also use the loop-unrolled sub-SAR ADC, but the SAR ADC shares the same capacitor array with the MDAC, so the bit-cycle is longer. Huang *et al.* [17] use the passive residue transfer technique as [19] to arrange the SAR ADC and the MDAC to operate in a pipeline fashion. Hence, the ADC speed is limited by only the sampling time, operation speed of the SAR ADC, and the residue transfer speed, which increases the speed significantly. However, the price of the residual transfer technique is that the voltage transfer needs to be done with good linearity and low noise as the SAR ADC becomes the first stage of the pipelined ADC with attenuation instead of gain. Also, it puts more stringent requirement on the MDAC and the second SAR ADC with the signal attenuation in the first SAR. Our SAR1 is still faster than SAR1 in [17].

For MDAC, open-looped MDAC generally achieves lower power consumption. Reference [32] has better power efficiency than our design. This is mainly a process issue. The design in [32] operates at a much lower speed in 40-nm process. On the other hand, our speed has been pushed closer to the process limit. In our SAR ADCs, transistor switch size needs to be increased significantly to reduce the ON-resistance slightly. Hence, the power efficiency of our SAR ADC is less compared to [32]. Open-loop dynamic amplifiers were used in [12], [17], and [18] to achieve very good power efficiency. Dynamic amplifiers in this paper amplify the residual voltage by discharging a capacitor with a current proportional to the MDAC input voltage within a duration. In addition, Huang *et al.* [17] implemented a calibration technique to compensate the static PVT spread for dynamic amplifiers. While they are very power efficient, these amplifiers are sensitive to dynamic issues in the transient settling process, such as clock jitter and power supply spikes, besides static PVT spread. On the other hand, the resistive open-loop amplifier in our work and [24] is based on the settled voltage, which is insensitive to dynamic issues in principle. Our calibration scheme provides a solution to remove the static PVT spread for open-loop amplifiers.

It is worth of mentioning that the split-capacitor looped-unrolled SAR ADC technique and the DAC gain calibration technique are additive to many pipelined-SAR ADC designs in Table I, such as designs using dynamic amplifiers. These two techniques can make SAR1 in those designs run faster and be more robust against PVT spread.

V. CONCLUSION

This paper describes the design of a 12-bit, 300-MS/s pipelined-SAR with open-loop MDAC. It analyzes the speed limitation of pipelined-SAR ADCs, and it finds the first SAR ADC would be the bottleneck for pipelined-SAR ADCs to

achieve very high speed. In this paper, a loop-unrolled SAR ADC is designed with split capacitor to achieve faster speed. A calibration technique based on DAC gain is designed for a resistive open-loop MDAC to compensate its PVT spread. With these techniques, this pipelined-SAR ADC achieves one of the highest sampling speeds with a single channel. It also achieves a Walden FoM of 34 fJ/conversion-step.

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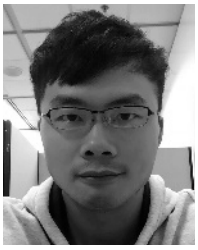

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