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A novel design of 1-bit full adders for eliminating voltage step in BBL-PT full adder using 32-nm CNTFET technology

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ABSTRACT

The full adder is essential for building computing systems like multipliers. Optimizing its design with CNTFET technology enhances low power, speed, and circuit density. This article presents a novel approach to address the challenges in Branch-Based Logic and Pass-Transistor (BBL-PT) based 1-bit full adder. The proposed approach involves the use of alternative modified level restorers, including a current sink, D-CNTFET (Diode connected CNTFET), modified current sink, and source structures. The BBL-PT full adder suffers from a voltage step issue in its output. The proposed solution eliminates this drawback using four alternative restorer structures. For +0.9 V supply voltage at 32-nm CNTFET technology, among all the proposed adder designs, the current sink based adder has a reported power consumption of 0.0845 μW, which is exceptionally low with the propagation delay is specified as 6.127 Ps and the Power-Delay Product (PDP) is 0.5177 aJ. The deliberate use of the current sink restorer in the design contributes to achieving these exceptional performance characteristics. An N-bit parallel adder (N=8, 16 & 32) using the proposed full adders is presented, with performance evaluated at 32-nm CNTFET technology and +0.9 V supply using Mentor Graphics tools. Results highlight its efficiency and superiority over existing solutions.

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KEYWORDS
CNTFETs; full adder; level restorer structures; leakage power; parallel adder implementation

1. Introduction

As Si-MOSFETs have advanced to the nanoscale, continued scaling has faced challenges due to short channel effects, such as *Drain-Induced Barrier Lowering* (DIBL), velocity saturation, and hot carrier generation. These effects negatively impact device performance, particularly increasing power consumption during the turn-off phase (Fuad et al., 2023). In contrast, CNTFETs provide several advantages over traditional MOSFETs in digital electronics (Naveen et al., 2022).

CNTFETs utilise *Carbon Nanotubes* (CNTs) as the conducting channel, which are cylindrical carbon allotropes available in two forms: *Single-Walled Carbon Nanotubes* (SWCNTs) and *Multi-Walled Carbon Nanotubes* (MWCNTs). A SWCNT is created by rolling a single sheet of carbon atoms along a specific vector, represented as $C = n_1a + n_2b$, where n_1 and n_2 are positive integers defining chirality, and **a** and **b** are lattice unit vectors, as illustrated in Figure 1 (Gupta & Dixit, 2021).

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SWCNT includes armchair CNT ($n1 = n2 = n$), zigzag CNT ($n1 = n, n2 = 0$) and Chiral CNT ($n1 \neq n2$ and $n1, n2 \neq 0$) (Gupta & Dixit, 2021). CNTFETs as shown in Figure 2 are generally designed in terms of number of CNTs in the channel (N), centre-centre distance between two consecutive tubes known as Inter-CNT Pitch (S) and the *Diameter of CNT* (D_{CNT}) (Deng & Wong, 2007).

D_{CNT} can be calculated from Eq. (1) that the threshold voltage of the CNTFET is an inverse function of the diameter of CNT (Deng & Wong, 2007) which is calculated by Eq. (2), Where n1, n2 are the chiral numbers.

In this paper, for a CNTFET with the chiral numbers (n1, n2) = (19, 0), D_{CNT} is 1.487 nm and subsequently its threshold voltage is 0.289 V.

$$D_{CNT} = \frac{a \times \sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\Pi} \approx 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 n_2} \tag{1}$$

$$V_{th} \approx \frac{E_g}{2.e} = \frac{\sqrt{3}}{3} \frac{a.V_\Pi}{e.D_{CNT}} \approx \frac{0.43}{D_{CNT}} \tag{2}$$

Table 1 presents the CNTFET model parameters, their values, and brief explanations. Based on the results in Sections 4 and 5, an appropriate value for the CNTFET transistor is selected from the Stanford CNTFET Model technology for the 1-bit adder analysis. The advantages of CNTFETs – such as low power consumption, high on/off current ratio (minimising leakage currents), faster switching speed, improved circuit density, and CMOS compatibility, make them a promising alternative to traditional MOSFETs in full adder designs.

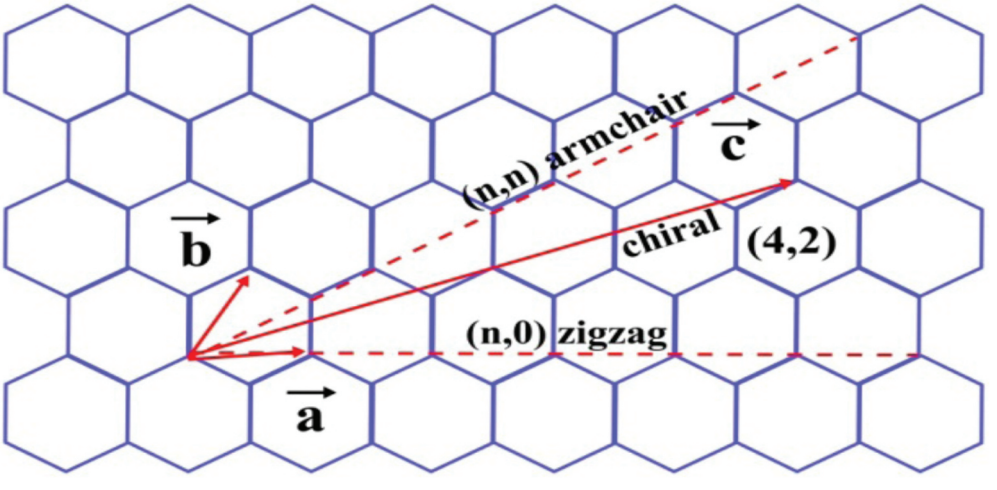


Figure 1. Unrolled graphite sheet and chirality of the CNT tube.

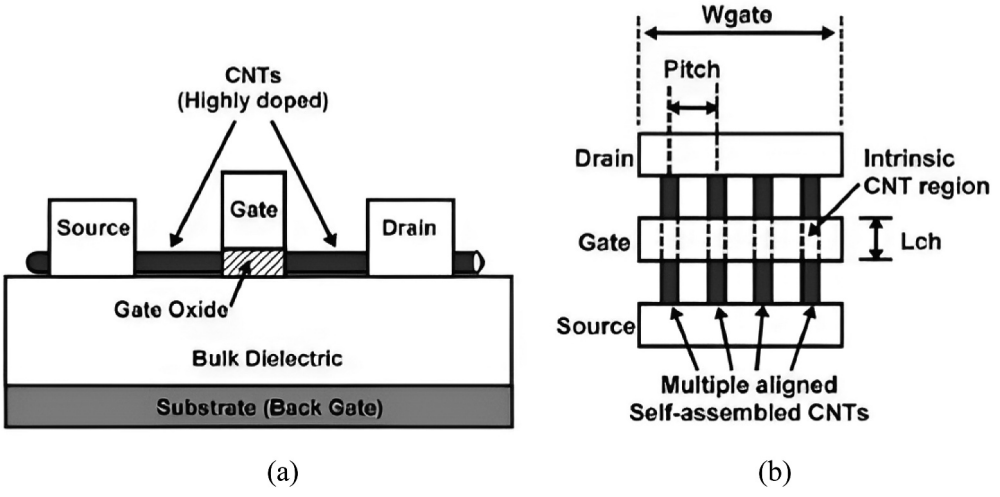


Figure 2. CNTFET structure (a) Cross-sectional view, (b) top view.

2. State of the art

The *full adder* (FA) is a vital component in advanced VLSI circuits and serves as a fundamental building block for high-speed, low-power digital applications. Its versatility makes it essential in designs, such as Carry Propagate Adders, Carry Look Ahead Adders, and various multipliers (Array, Radix-n, and Wallace Tree). FAs are also crucial in building Counters, *Arithmetic Logic Units* (ALUs), Memory units, Finite State Machines, Microprocessors, and Microcontrollers. In many systems, the adder significantly impacts the critical path, directly influencing overall system performance.

Standard implementations exist for FA cells, outlined as follows:

(1) The traditional CMOS FA circuit, as described in reference (Weste & Harris, 2015), comprises 28 transistors. It relies on the standard CMOS structure, utilising pull-up PMOS and pull-down NMOS networks.
(2) The circuit based on *Complementary Pass-Transistor Logic* (CPL) for the FA, as outlined in reference (Kang & Leblebici, 2011), utilises 32 transistors. CPL employs two distinct components for generating sum and carry outputs.
(3) The FA circuit based on T*ransmission-Gates CMOS* (TG-CMOS) architecture, as detailed in reference (Anjaneyulu & Reddy, 2023), consists of 20 transistors.
(4) By employing the multi-threshold voltage concept in CNTFET technology, a ternary circuit with a single supply can be constructed for both successor and predecessor (Hosseini & Etezadi, 2021).
(5) The FA cell known as the *Transmission Function Full-Adder* (TFA), as discussed in reference (Alioto et al., 2012), is grounded in transmission function theory and consists of 16 transistors.
(6) Energy-efficient CNTFET-based full adder design with Static CMOS output drive is discussed in reference (Johnson & Anderson, 2022).

(7) A novel *full adder* (FA) circuit based on Approximate Computing uses 12 transistors and incorporates *Gate Diffusion Input* (GDI) and *Dynamic-Threshold* (DT) techniques, leveraging CNTFET technology advancements (Sadeghi et al., 2023).
(8) Two innovative 1-bit inverter-based ternary FA cells, with the second design utilising just 37 CNTFET transistors (Mahmoudi et al., 2020). These designs are developed based on a novel concept of Majority-NOT based full adder.
(9) 1-bit FA design using hybrid logic, incorporating 16 transistors as indicated in reference (Tirumalasetty & Machupalli, 2019).
(10) A novel design of a hybrid FA using *Pass Transistors* (PTs), *Transmission Gates* (TGs) and CMOS logic is presented (Hasan et al., 2020).
(11) A high performance CNTFET-based FA cell applicable in: Carry ripple, carry select and carry skip adders discussed in reference (Tari et al., 2020).
(12) A multiplexer-based ternary FA cell utilising CNTFET technology is presented in Tabrizchi & Dehghani (2021) to analyse how variations in process (P), voltage (V), and temperature (T) affect the performance and behaviour of the circuit.

The remaining section of the paper is structured as follows: Section 3 details the implementations of the proposed 1-Bit full adders based on restorer structures, while Section 4 elaborates on the simulation results. This paper further discusses the implementation of an N-bit parallel adder ($N = 8$, 16 & 32) based on the proposed full adders in Section 5. Lastly, Section 6 ended up with the conclusion.

3. Proposed 1-bit full adder cell implementations

A *Full Adder* (FA) cell is a fundamental building block with three 1-bit inputs (A, B, and C_{in}) and two 1-bit outputs (Sum (S_{out}) and Carry (C_{out})). The relationships between the inputs (A, B, and C_{in}) and the outputs (sum and carry) are defined by specific logical expressions of the Full Adder cell as

$$Sum = ABCin + \bar{A}\bar{B}Cin + \bar{A}B\bar{Cin} + A\bar{B}\bar{Cin} \tag{3}$$

$$Cout = AB + BCin + ACin \tag{4}$$

Branch-based logic leveraging the advantages of reduced parasitic capacitances, minimal contacts, and fewer metal connections, branch-based logic is well-suited for low-power designs and high-speed applications (Piguet & Piguet, 2004). Its utilisation in *Silicon on Insulator* (SOI) technology further enhances its benefits, enabling the implementation of efficient and high-performance logic circuits, such as fast adders (Elangovan & Devika, 2021).

The BBL-PT full adder implementation suffers from weak high output levels due to the discharge in the pass transistors used in the sum block. This issue can be mitigated by employing a feedback pull-up PMOS transistor to enhance drive strength for subsequent stages, effectively restoring the weak logic '1' to a stronger level.

The level restoration method for the BBL-PT full adder, which aims to strengthen weak logic '1' outputs from pass transistors, can lead to a voltage step at the output node 'Sout' during a 0 → 1transition (as shown in Figure 12). This voltage step may lead to increased power consumption, signal integrity issues, and potential errors in downstream circuitry,

compromising the overall performance. To address this, alternative-level restoration structures can be proposed to eliminate the voltage step problem.

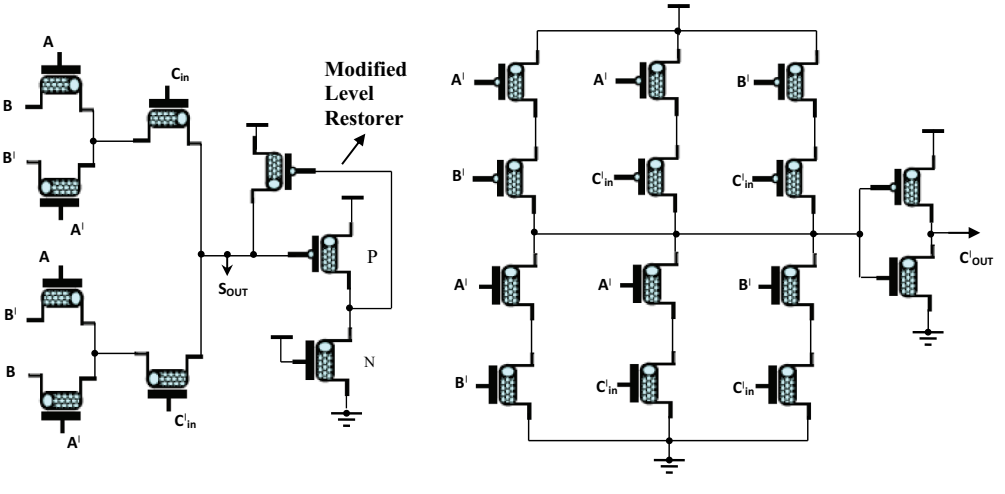
3.1. 1-bit full adder based on current sink restorer

In the proposed alternative-level restorer structure for the BBL-PT full adder, a current sink restorer is utilised as shown in Figure 3. This current sink restorer consists of a current sink load and a common gate configuration using an N-CNTFET. The purpose of this structure is to provide improved level restoration and eliminate the voltage step issue during $0 \rightarrow 1$ transitions.

The current sink restorer operates as follows:

- The current sink load, which is typically an N-channel CNTFET, is biased with a fixed bias supply. This bias supply ensures a constant current flow through the load, making the load behave as a current sink.
- The N-channel CNTFET in the common gate configuration serves as the input transistor. Its gate is connected to the fixed bias supply, keeping the transistor in an ON condition at all times.
- The P-channel CNTFET in the current sink restorer acts as the pull-up network. It provides the necessary pull-up capability to restore the output voltage level.

In the BBL-PT full adder, the SUM block is implemented using pass transistors rather than branches, as the latter requires a higher transistor count (24), making it less advantageous. This choice is illustrated in Figure 3(a). The carry function, however, is implemented using a branch structure, following the simplification method outlined in reference (Piguet & Piguet, 2004), as shown in Figure 3(b).



(a) Sum Circuit (b) Carry Circuit

Figure 3. Proposed 1-bit full adder circuit with current sink restorer structure.

The carry circuit is remains consistent across all proposed 1-bit full adders. The N-CNTFET and P-CNTFET networks are represented as sums of products derived from Karnaugh maps, with the corresponding equations for each component as follows:

$$CP = CN = \bar{A}\bar{Cin} + \bar{B}\bar{Cin} + \bar{A}\bar{B} \tag{5}$$

In Figure 3(a), the full adder sum circuit utilises N-CNTFET transistors, which are characterised by stronger '0' levels and weaker '1' levels when an input is applied. When logic '1' is passed through the N-CNTFET network and the node 'Sout' must be charged to a weak logic '1,' the pull-up P-CNTFET transistor in the current sink restorer behaves as follows:

When the voltage at node 'Sout' is less than $V_{DD}/2$ (indicating a weak logic '1'), the P-CNTFET transistor in the current sink restorer reaches its switching threshold and turns ON. Since, when the voltage at node 'Sout' falls below a certain threshold, it triggers the P-CNTFET transistor to conduct.

Once the P-CNTFET transistor (P) in the current sink restorer turns ON, the output of the restorer circuit becomes logic '1'. This logic '1' output turns OFF the pull-up P-CNTFET transistor connected to the node 'Sout'. By turning off the pull-up P-CNTFET transistor, the node 'Sout' is no longer charged by the pull-up network. Instead of being charged by the pull-up P-CNTFET transistor, the node 'Sout' is charged with an effective drive current that equals the current provided by the N-CNTFET network. This occurs because the N-CNTFET transistors in the network continue to conduct and supply the necessary current to charge the node 'Sout' to the weak logic '1' level.

When the voltage at node 'Sout' reaches $V_{DD}/2$, indicating logic '1' input to the restorer, the P-CNTFET transistor (P) in the current sink restorer is turned OFF and N-CNTFET (N) is always ON condition irrespective of input. Consequently, the output of the restorer becomes logic '0'. This turning ON of the pull-up P-CNTFET transistor allows the effective drive current charging the capacitance at node 'Sout' to become the sum of the current flowing through the N-CNTFET network and the additional current provided by the pull-up P-CNTFET transistor.

By combining the current from the N-CNTFET network and the pull-up P-CNTFET current, the effective drive current for charging the capacitance at node 'Sout' is increased. This results in a faster and more robust transition to logic '1' and reduces the delay during the $0 \longrightarrow 1$transition and can lead to eliminate the voltage step at the output node 'Sout'.

3.2. 1-bit full adder based on D-CNTFET restorer

The proposed 1-bit full adder with a D-CNTFET restorer structure, shown in Figure 4, has its drain terminal shorted to the gate terminal. As the output voltage (V_O) rises, the drain current (Ids) through the CNTFET increases exponentially, keeping the N-CNTFET continuously in the ON state.

When the voltage at node 'Sout' is less than $V_{DD}/2$ (indicating a weak logic '1'), the P-CNTFET transistor (P) in the D-CNTFET restorer reaches its switching threshold and turns ON. Since when the voltage at node 'Sout' falls below a certain threshold, it triggers the P-CNTFET transistor to conduct.

Once the P-CNTFET transistor (P) in the D-CNTFET restorer turns ON, the output of the restorer circuit becomes logic '1'. This logic '1' output turns OFF the pull-up

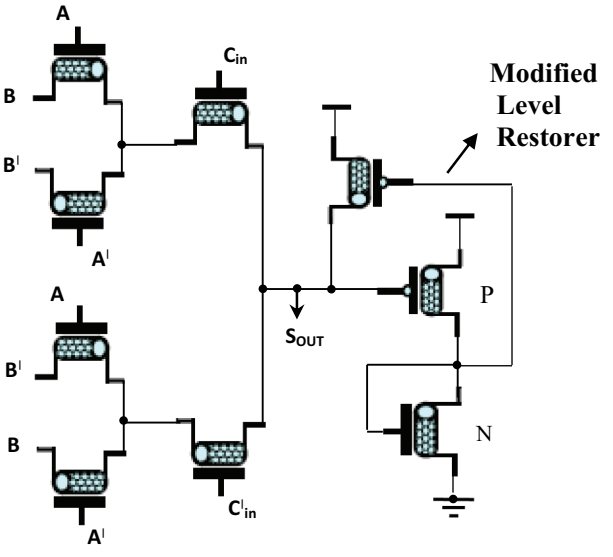


Figure 4. Proposed full adder circuit with D-CNTFET restorer structure.

P-CNTFET transistor connected to the node 'Sout'. By turning off the pull-up P-CNTFET transistor, the node 'Sout' is no longer charged by the pull-up network. Instead of being charged by the pull-up P-CNTFET transistor, the node 'Sout' is charged with an effective drive current that equals the current provided by the N-CNTFET transistors network.

When the voltage at node 'Sout' reaches $V_{DD}/2$, indicating logic '1' input to the restorer, the P-CNTFET (P) in the D-CNTFET restorer turns OFF, while the N-CNTFET (N) remains ON regardless of the input. As a result, the restorer output becomes logic '0'. The activation of the pull-up P-CNTFET enables the effective drive current at node 'Sout' to combine the N-CNTFET current with the additional current from the P-CNTFET, leading to a faster and stronger 0 → 1 transition to logic '1' and eliminating the voltage step at 'Sout.'

3.3. 1-bit full adder based on modified current sink restorer

The current sink restorer (Figure 3) requires an on-chip battery, which is difficult to integrate. The modified current sink restorer (Figure 5) addresses this issue by using a voltage divider Complementary-CNTFET circuit and a P-CNTFET pull-up network. This design eliminates the need for an on-chip battery and provides an alternative DC voltage source. The voltage divider ensures a suitable DC voltage for the N-CNTFET, keeping it ON, while the P-CNTFET pull-up ensures proper signal propagation and desired logic functionality.

The inclusion of a capacitor in the modified current sink and source-based adder circuits (Figures 5 and 6) acts as a charge storage element, allowing controlled transistor

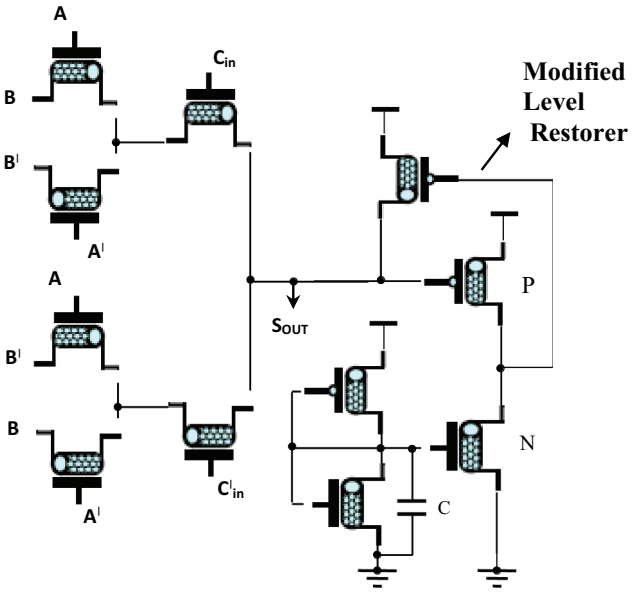


Figure 5. Proposed full adder circuit with modified current sink restorer structure.

operation. This reduces continuous current flow and helps lower leakage power dissipation while retaining the restorer circuit's ability to eliminate the voltage step issue.

This approach introduces modified current sink structure as alternatives to the basic current sink restorer. These modified structures enhance the performance of the restorer circuit by optimising the current flow and improving the transition characteristics. By modifying the current sink structure, the effective drive current for charging the capacitance at the node 'Sout' is increased during the transition from logic '0' to logic '1.' This increased drive current allows for a faster and more robust transition, reducing the delay and further minimising the voltage step.

3.4. 1-bit full adder based on modified current source restorer

The current source restorer faces challenges due to the need for an on-chip battery. To address this, the modified current source restorer (Figure 6) incorporates a voltage divider Complementary-CNTFET circuit, eliminating the battery requirement. The voltage divider supplies the necessary DC voltage to keep the P-CNTFET (P) in the ON state, ensuring proper logic functionality and signal propagation.

In the modified current source restorer, when logic '1' is passed through the N-CNTFET network and the voltage at node 'Sout' is below $V_{DD}/2$, the N-CNTFET turns OFF, resulting in a weak logic '1' at the output. As the voltage at 'Sout' reaches $V_{DD}/2$, the N-CNTFET turns ON while the P-CNTFET remains ON, causing the output to switch to logic '0.' The combined currents from the N-CNTFET and the pull-up P-CNTFET charge the node capacitance, ensuring faster transitions and proper signal propagation.

In summary, the proposed level restorer structures provide controlled and gradual voltage transitions in the BBL-PT full adder's output stage. By optimising current flow and

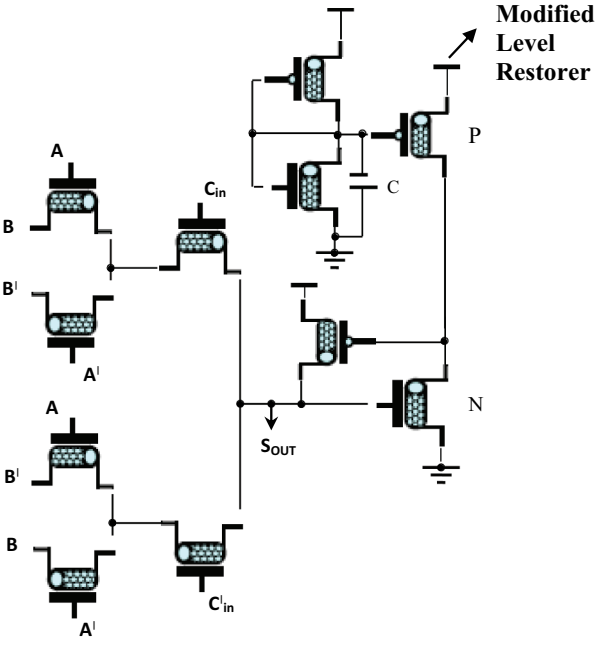


Figure 6. Proposed full adder circuit with modified current source restorer structure.

improving transition dynamics, these designs resolve the voltage step issue, leading to enhanced performance.

4. Simulation results

The proposed 1-bit FA circuits were simulated using a 32-nm Stanford CNTFET Model technology at a supply voltage of 0.9 V (Stanford CNTFET Model, 2024). The Mentor Graphics Schematic Design Composer CAD tool is used for the simulations, and the threshold voltage (V_{th}) is set to 0.289 V. The chirality vector of the CNT used in CNTFETs is specified as (19, 0), defining the carbon atom arrangement and influencing the CNTFET's electrical properties. The Stanford CNTFET Models are designed for Zigzag CNTs with this chirality vector. The (19, 0) chirality vector represents a zigzag CNT with semiconducting properties, essential for CNTFETs in switching applications. This chirality provides a suitable band-gap for efficient on-off switching in digital circuits.

To ensure the practical applicability of the proposed 1-bit adders in VLSI applications, a practical simulation environment was set up based on the configuration shown in Figure 7. In order to accurately reflect practical environment, buffers were incorporated at both the input and output of the test bench (Wind et al., 2024). Two inverters with the same W/L have been employed to construct the input and output buffers.

The distance between the centres of two adjacent nanotubes is called pitch, which has a direct impact on the width of the connections and gate of the transistor. The width of the gate of a CNTFET is estimated by the following equation (Kim & Lombardi, 2009):

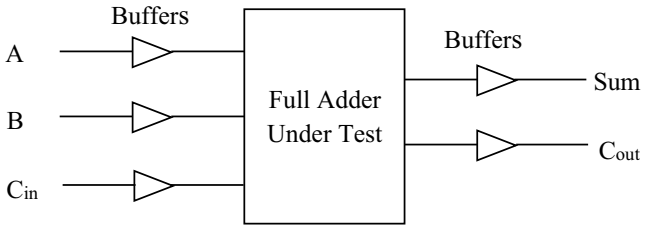


Figure 7. Simulation test bench for the proposed full adders.

$$W_{gate} = \max(W_{min}, \mathrm{N} \times \mathrm{Pitch}) \tag{6}$$

Where N is the number of nanotubes under the gate, W_{min} is the minimum width of the gate determined by the photolithography process. As per the Stanford CNTFET Model technology (Model, 2024), $N = 3$ and Pitch = 20 nm provided in Table 1 and the W_{gate} is 60 nm for all the CNTFET transistors.

The performance analysis of different existing 1-bit FA designs was compared with respect to the newly proposed designs in terms of power, delay, and PDP are presented in Table 2.

Frequency & Load Analysis: To improve operating frequency, reducing load capacitance is a critical parameter, as output load directly influences power consumption and circuit performance. In this analysis, we varied output loads from 1 fF to 8 fF, while maintaining a fixed 1 fF capacitance at the buffer output during all simulations. The highest frequency at which the considered adder operates reliably with valid logic levels is denoted as f_{dmax} (Parameshwara & Srinivasaiah, 2017), was found to be 1.44 GHz for the proposed 1-bit current sink-based adder at +0.9 V and 1 fF output load, indicating its optimal frequency for proper logic operation.

Table 3 presents a comparison of the proposed 1-bit FA designs by varying the supply voltage (V_{DD}). The aim is to evaluate the impact of different supply voltages on power consumption, delay, and overall performance of the proposed adder circuits.

By varying the supply voltage impacts adder designs, with higher voltages increasing power consumption but reducing delay for faster operation, while lower voltages reduce power consumption but increase delay, resulting in slower operation. Table 3 compares these trades-offs, providing insights into optimising the supply voltage for the proposed 1-bit full adders, balancing power efficiency and performance.

4.1. Leakage power measurement

CNTFETs exhibit a high on/off current ratio, minimising leakage currents and power dissipation, which enhances power efficiency in full adder circuits. Lowering the supply voltage in CNTFET-based designs further reduces leakage power while maintaining performance, making them ideal for energy-efficient adder design. Leakage power calculations for the proposed and alternative 1-bit full adder implementations are summarised in Table 4.

Table 1. Some of the CNTFET model parameters.

CNTFET Parameter	Value	Brief Description
Supply	0.9V	Supply Voltage
$L_{channel}$	32 nm	Channel Length
L_{ss} /L_{dd}	32 nm	Fermi level of doped CNT source/drain region
t_{ox}	4 nm	Thickness of high-k top gate dielectric material
K	16	Dielectric constant of high-k top gate dielectric material
E_{fi}	6 eV	Fermi level of the doped S/D tube
C_{sub}	20 pf/m	Capacitance between channel and substrate
Pitch	20 nm	Distance between the centers of two neighboring CNTs within the same device
Tubes	3	Number of CNTs
n_1,n_2	19,0	Chirality Vector

Table 2. Performance comparisons of the proposed and alternative implementations of 1-bit full adder cells with V_{DD} = +0.9 V at 32-nm CNTFET technology.

Design	Power (μW)	Delay (Ps)	PDP (aJ)	Transistor Count
BBL-PT (Ilham Hassoune et al., 2010)	0.0924	16.439	1.5189	23
CMOS (Weste & Harris, 2015)	0.3334	15.674	5.2257	28
CPL (Kang & Leblebici, 2011)	1.3965	14.780	20.6402	32
TGA (Anjaneyulu & Reddy, 2023)	0.4954	13.241	6.5595	20
TFA (Alioto et al., 2012)	0.3584	16.253	5.8250	16
SCMOS CNTFET (Johnson & Anderson, 2022)	1.0641	21.682	23.0718	28
MVL CNTFET (Mahmoudi et al., 2020)	0.8572	17.493	14.9949	37
Hybrid Adder(16T) (Tirumalasetty & Machupalli, 2019)	0.4528	16.042	7.2638	16
CNTAFS (Tari et al., 2020)	1.3854	8.475	11.7412	20
PVT-CNTFET (Tabrizchi & Dehghani, 2021)	0.7462	7.962	5.9412	24
Proposed Full Adder 1 (Current Sink Restorer)	**0.0845**	**6.127**	**0.5177**	**23**
Proposed Full Adder 2 (D-CNTFET Restorer)	0.0962	7.825	0.7527	23
Proposed Full Adder 3 (Modified Current Sink)	0.1542	8.451	1.3031	25
Proposed Full Adder 4 (Modified Current Source)	0.1196	8.4582	1.01160	25

Table 3. Comparison table for the proposed 1-bit full adder designs against variation in supply voltage V_{DD}.

	Supply Voltage V_{DD} (V)								
	0.7 V			0.8 V			0.9 V		
Design	Power (μW)	Delay (Ps)	PDP (aJ)	Power (μW)	Delay (Ps)	PDP (aJ)	Power (μW)	Delay (Ps)	PDP (aJ)
Proposed Full Adder 1	**0.0386**	**7.141**	**0.2756**	**0.0572**	**6.593**	**0.3771**	**0.0845**	**6.127**	**0.5177**
Proposed Full Adder 2	0.0524	8.647	0.4531	0.0786	8.295	0.6519	0.0962	7.825	0.7527
Proposed Full Adder 3	0.0842	9.378	0.7896	0.0963	8.753	0.8429	0.1542	8.451	1.3031
Proposed Full Adder 4	0.0915	9.413	0.8612	0.0984	8.892	0.8749	0.1196	8.4582	1.0116

The proposed full adders exhibit higher leakage power dissipation compared to the *CNTFET-based Adder Circuit* (CNTAFS), mainly due to a characteristic of their restorer circuits. In these circuits, either the N-channel or P-channel CNTFET remains always ON during operation, leading to significant leakage power consumption, even as the restorer circuits effectively eliminate the voltage step issue.

Table 4. Leakage power comparison of the proposed and alternative implementations of 1-bit full adder cells with V_{DD} = 0.7 V, 0.8 V & 0.9 V at 32-nm CNTFET technology.

	Leakage Power (nW)		
Design	0.7V	0.8V	0.9V
BBL-PT (Ilham Hassoune et al., 2010)	0.64	0.93	1.21
CMOS (Weste & Harris, 2015)	0.76	0.9	1.42
CPL (Kang & Leblebici, 2011)	1.12	1.5	1.83
TGA (Anjaneyulu & Reddy, 2023)	0.98	1.34	1.56
TFA (Alioto et al., 2012)	1.13	1.4	1.72
SCMOS CNTFET (Johnson & Anderson, 2022)	0.26	0.42	0.84
MVL CNTFET (Mahmoudi et al., 2020)	0.45	0.76	1.1
Hybrid Adder(16T) (Tirumalasetty & Machupalli, 2019)	1.28	1.49	1.74
CNTAFS (Tari et al., 2020)	**0.21**	**0.32**	**0.71**
PVT-CNTFET (Tabrizchi & Dehghani, 2021)	0.34	0.58	0.96
Proposed Full Adder 1	0.49	0.82	1.19
Proposed Full Adder 2	0.42	0.93	1.22
Proposed Full Adder 3	0.71	1.08	1.34
Proposed Full Adder 4	0.82	1.15	1.39

4.2. Temperature stability analysis

The performance of the proposed current sink-based adder circuit was evaluated over a temperature range of −50°C to 150°C. The results revealed excellent temperature stability, with a minimal carry variation of just 0.00000304%, as shown in Figure 8. This stability establishes the adder circuit's suitability for commercial and industrial applications, demonstrating robustness and reliability even under extreme operating conditions.

To assess output constancy for the current sink restorer-based full adder (Figure 3), parametric variations were conducted concerning the *CNTFET Diameter* (D_{CNT}) and *Threshold Voltage* (V_{th}). Figure 9 illustrates how the *Power-Delay Product* (PDP) changes with variations in DCNT, while Figure 10 shows the effect of threshold voltage variations on PDP.

The delay parameter is defined as the time taken for the input to reach 50% of the power supply level until the output reaches the same level (Rafiee et al., 2022), as shown in Figure 11. The maximum delay across all transitions is considered the cell delay, representing the worst-case scenario. Propagation delay times for high-to-low τ_{PHL} and low-to-high τ_{PLH} transitions determine the input-to-output signal delay during these output changes (Mohammadi & Dolatshahi, 2022).

The voltage point $V_{50\%}$ is defined as follows

$$V_{50\%} = V_{OL} + \frac{1}{2}(V_{OH} - V_{OL}) = \frac{1}{2}(V_{OL} + V_{OH}) \tag{7}$$

Thus, the propagation delay times $\tau_{PHL}$and $\tau_{PLH}$are found from Figure 12 as

$$\begin{aligned} \tau_{PHL} &= t_1 - t_0 \\ \tau_{PHL} &= t_3 - t_2 \end{aligned} \tag{8}$$

The average propagation delay τ_P is given by

$$\tau_p = \frac{\tau_{PHL} + \tau_{PLH}}{2} \tag{9}$$

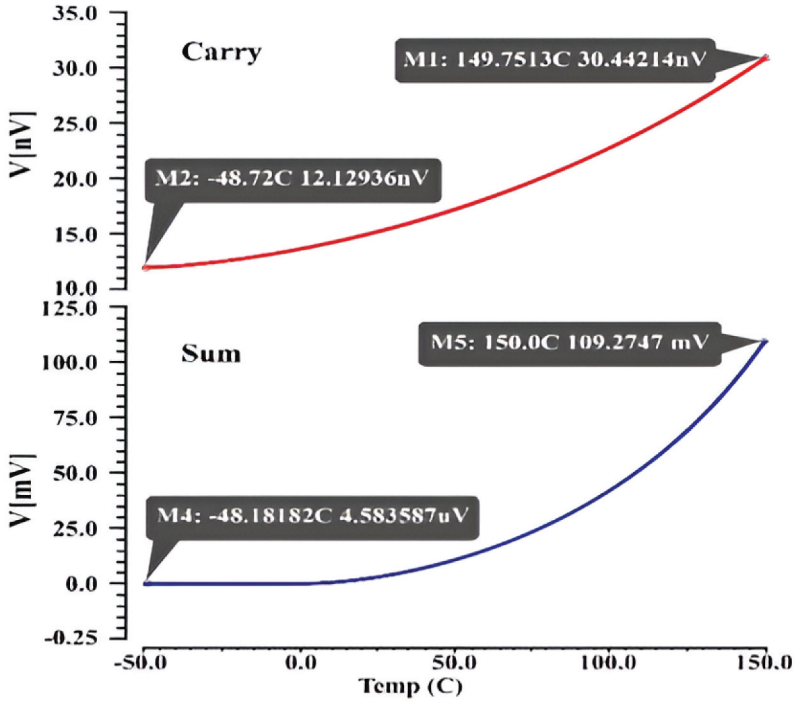


Figure 8. Simulated temperature stability of proposed current sink restorer based adder circuit.

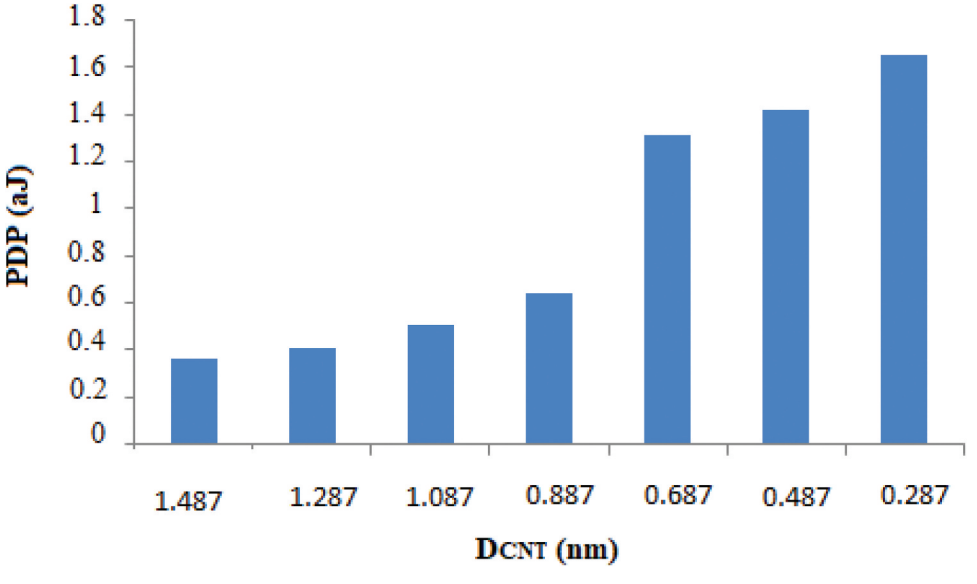


Figure 9. PDP vs. D_{CNT} variations.

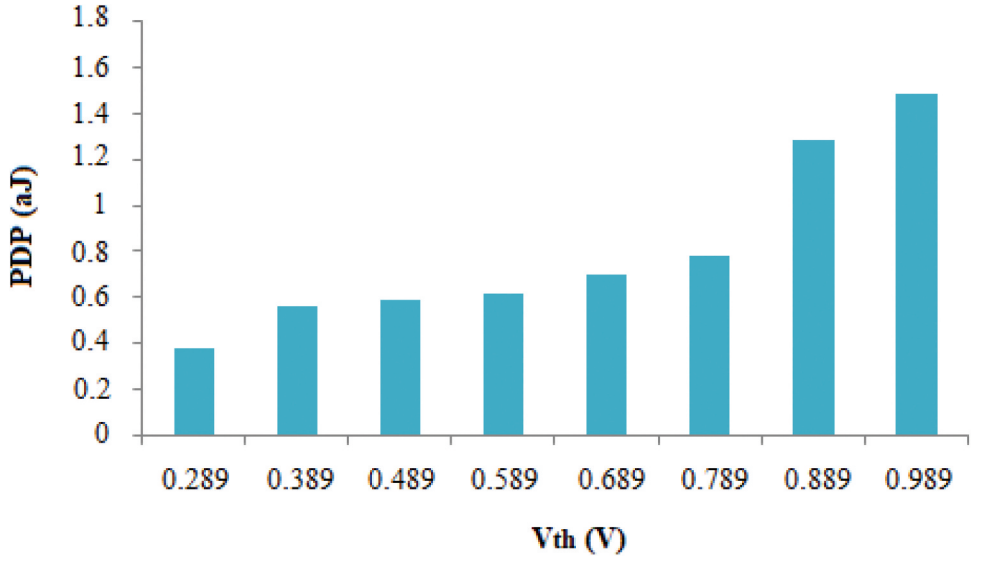


Figure 10. PDP vs. V_{th} variations.

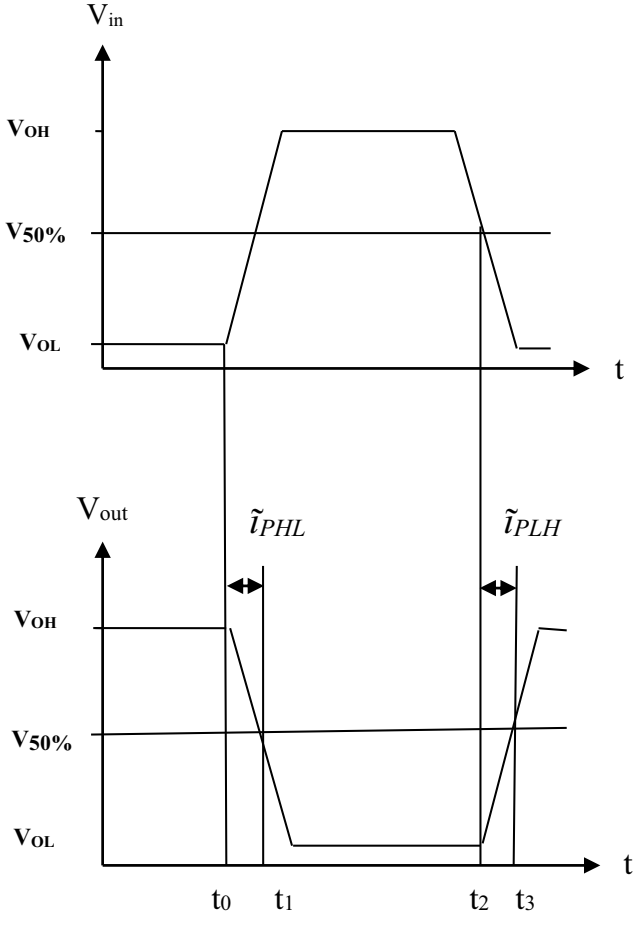


Figure 11. Propagation delay calculation.

The input and output waveforms of the existing (BBL-PT) 1-bit full adder were simulated and are shown in Figure 12. A voltage step is noted in the SUM output waveform during 0 → 1 transitions in the BBL-PT adder. This issue can be resolved by implementing alternative level restorer structures, as demonstrated in Figures 13–16.

Proposed structures effectively eliminate the voltage step during the SUM output 0 → 1 transition. Figures 14 and 16 illustrate the simulated waveforms for all possible input combinations (A, B, and C_{in}) ranging from 000 to 111.

The proposed 1-bit full adders were compared with *Quantum-dot Cellular Automata* (QCA) based full adders, as shown in Table 5. QCA represents a promising alternative to CMOS technology for nanoscale applications. Efficient adders are crucial in arithmetic circuit design, and QCA-based adders are anticipated to be essential for the next generation of digital systems (Seyedi & Navimipour, 2018a, 2018b, 2021a, 2021b, 2022).

5. Parallel adder implementation

The CNTFET-based N-bit parallel adder ($N = 8$, 16, & 32) utilises the proposed 1-bit full adder circuits. The 8-bit parallel adder takes two 8-bit binary numbers as input, producing binary sum and carry outputs, as illustrated in Figure 17. This diagram shows the interconnection of multiple 1-bit full adder instances to create the complete 8-bit parallel adder circuit (Tirumalasetty et al., 2024).

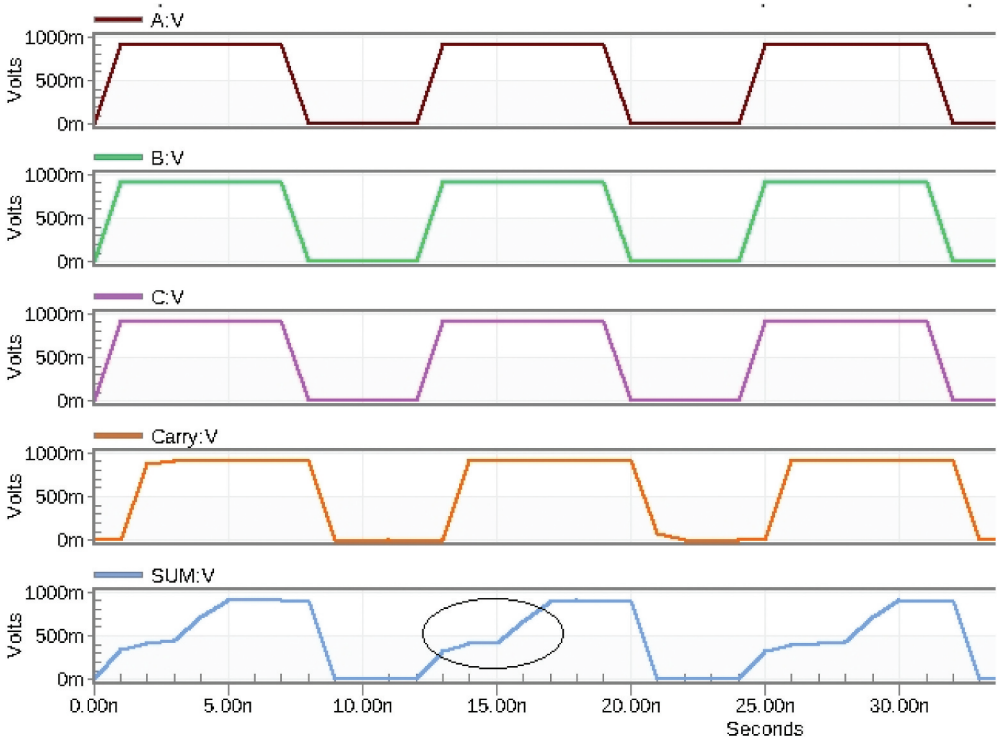


Figure 12. Simulated input & output waveforms of BBL-PT full adder (Ilham Hassoune et al., 2010).

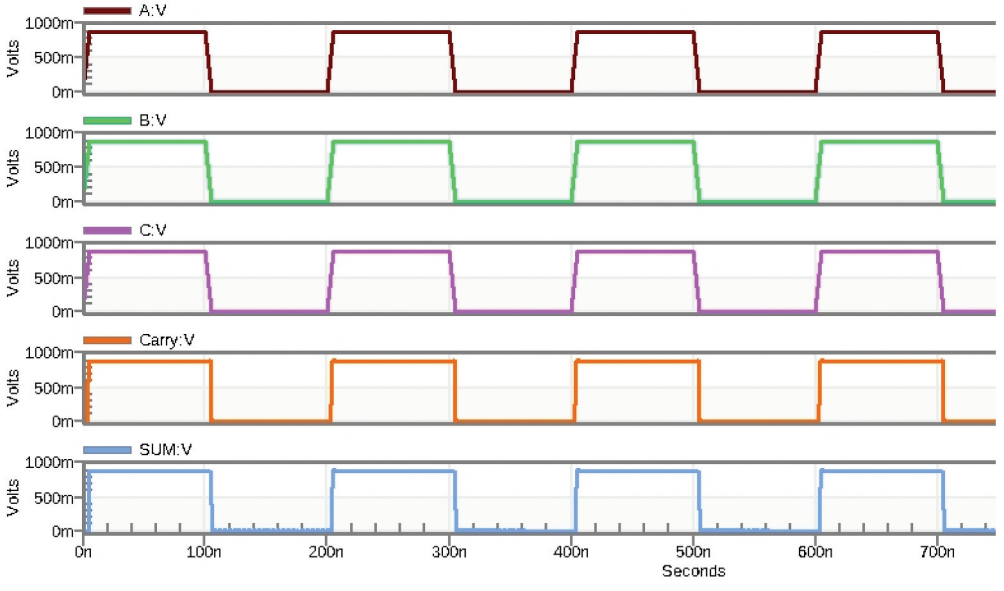


Figure 13. Simulated input & output waveforms of proposed 1-bit full adder (current sink).

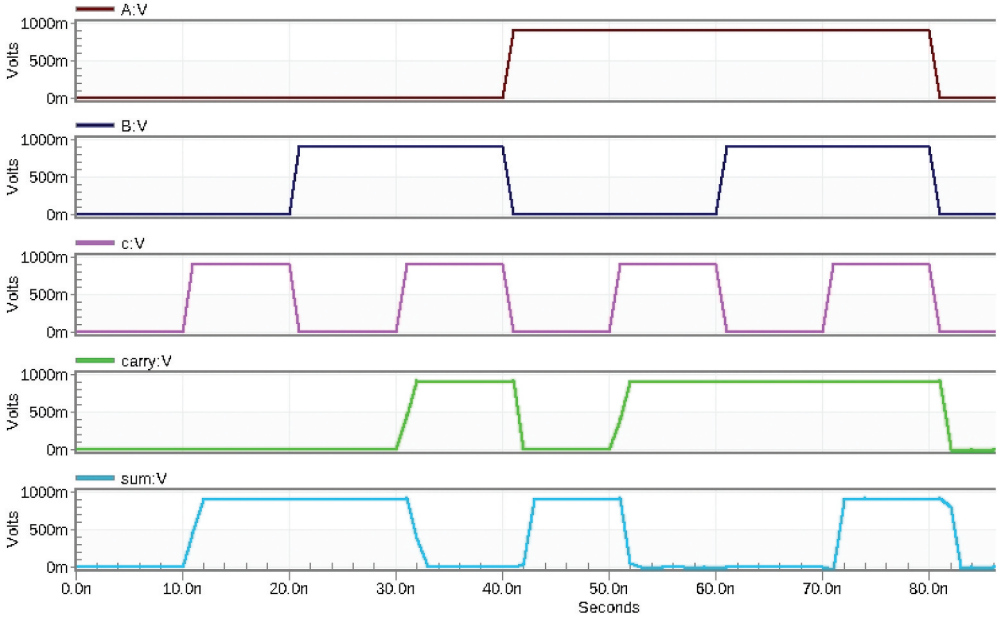


Figure 14. Simulated input & output waveforms of proposed 1-bit full adder (D-CNTFET).

Table 6 presents a performance comparison of the proposed 8-bit, 16-bit, and 32-bit parallel adders with existing adder structures in terms of power consumption, propagation delay, and PDP.

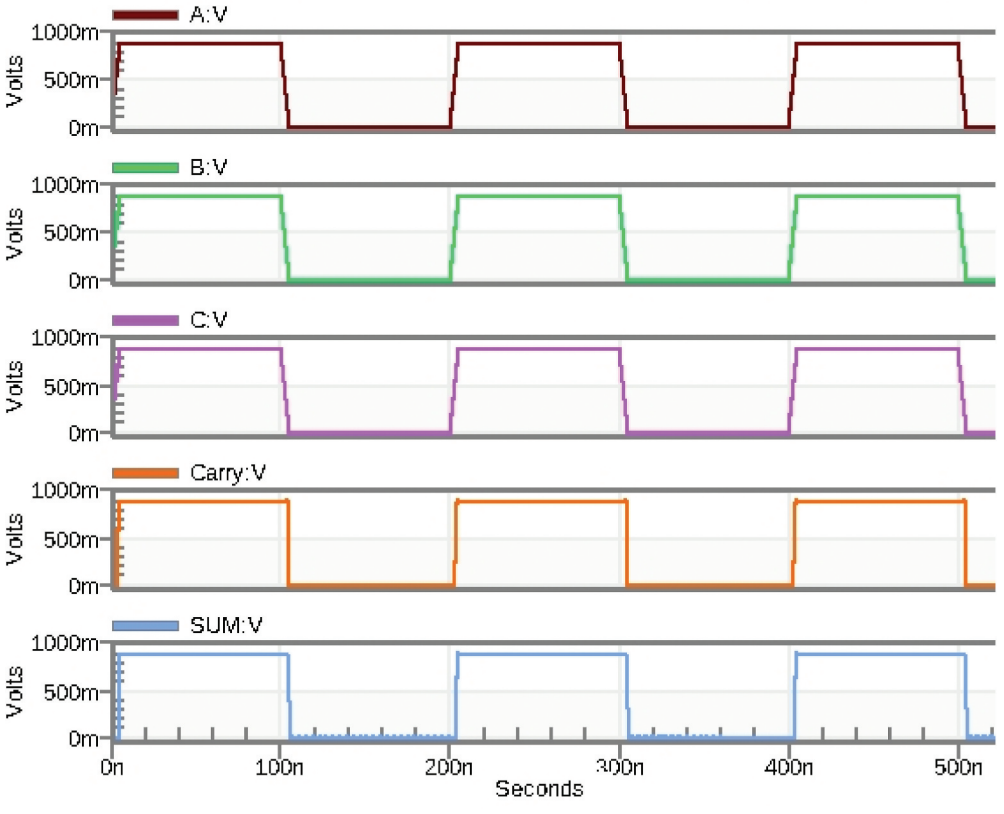


Figure 15. Simulated input & output waveforms of proposed 1-bit full adder circuit (modified current sink).

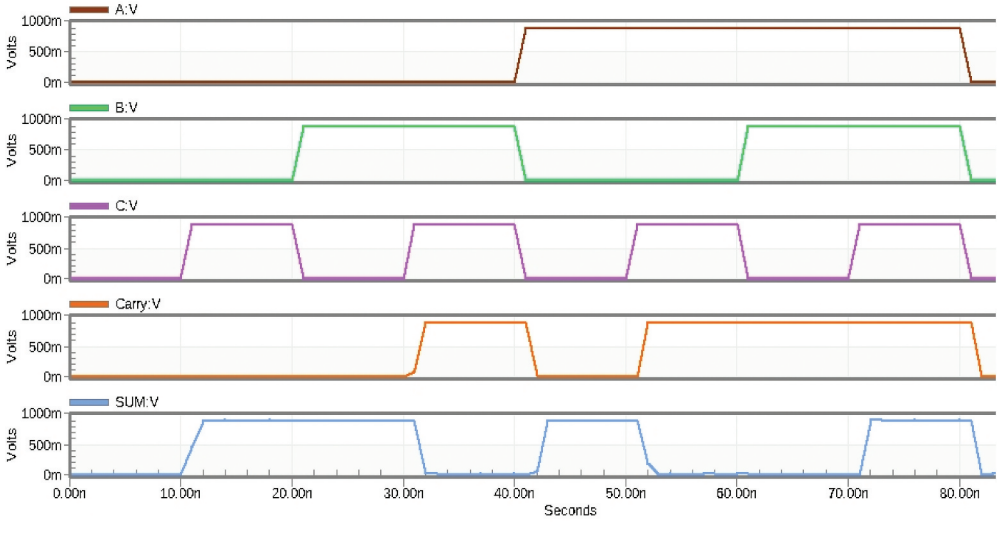


Figure 16. Simulated input & output waveforms of proposed 1-bit full adder circuit (modified current source).

Table 5. Delay value comparison of the proposed & QCA implementations of 1-bit full adder cells.

S.No	Design	Delay Value (Clock Phase)
1.	Full adder based on Nano scale QCA (Seyedi & Navimipour, 2018b)	3 Clock Phase
2.	Fault-tolerance full adder (Seyedi & Navimipour, 2018a)	97% achieves Fault -tolerance
3.	Three level full adder based on QCA (Seyedi & Navimipour, 2021b)	70% improvement in cell number
4.	Multi layer full adder based on QCA (Seyedi & Navimipour, 2021a)	2 Clock Phase
5.	Three input majority gate based on Quantum Computing (Seyedi & Navimipour, 2022)	Lowest latency of the 0.5 clock cycle
6.	**Proposed Full Adder 1**	6.127 Ps
7.	**Proposed Full Adder 2**	7.825 Ps
8.	**Proposed Full Adder 3**	8.451 Ps
9.	**Proposed Full Adder 4**	8.4582 Ps

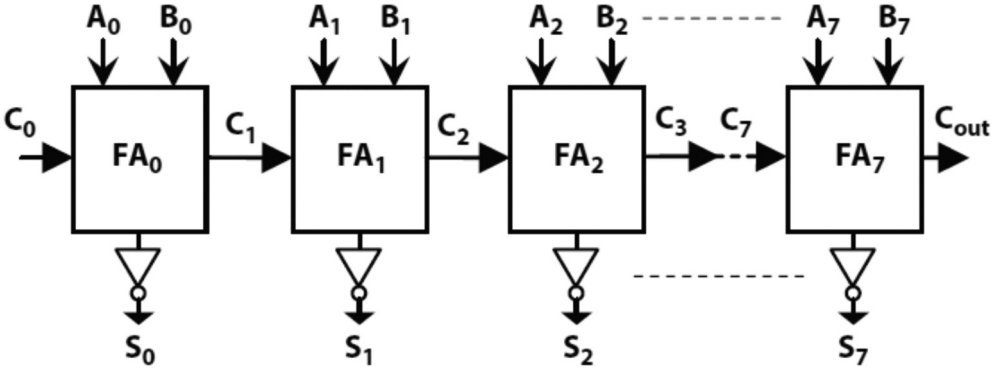


Figure 17. 8-bit parallel adder implementation using proposed 1-bit full adders.

Table 6. Performance comparisons of the proposed and alternative implementations of parallel adders (PA) with V_{DD} = +0.9 V at 32-nm CNTFET technology.

	8-Bit PA			16-Bit PA			32-Bit PA		
Design	Power (μW)	Delay (Ps)	PDP (aJ)	Power (μW)	Delay (Ps)	PDP (aJ)	Power (μW)	Delay (Ps)	PDP (aJ)
BBL-PT (Ilham Hassoune et al., 2010)	0.286	24.547	7.020	0.528	43.326	22.876	1.186	95.517	113.283
CMOS (Weste & Harris, 2015)	0.587	38.245	22.449	0.958	64.874	62.149	1.837	113.428	208.367
CPL (Kang & Leblebici, 2011)	3.567	33.428	119.237	5.847	44.592	260.729	9.813	82.629	810.838
TGA (Anjaneyulu & Reddy, 2023)	2.895	31.257	90.489	4.587	59.587	273.325	F*	F*	F*
TFA (Alioto et al., 2012)	2.567	44.872	115.186	5.254	83.743	439.985	F*	F*	F*
SCMOS CNTFET (Johnson & Anderson, 2022)	3.164	58.357	184.641	5.268	104.629	551.185	8.264	182.684	1509.70
MVL CNTFET (Mahmoudi et al., 2020)	2.864	51.758	148.234	4.927	97.176	478.786	F*	F*	F*
Hybrid Adder(16T) (Tirumalasetty & Machupalli, 2019)	0.487	46.547	22.668	0.984	89.285	87.856	1.768	192.438	340.230
CNTAFS (Tari et al., 2020)	3.413	28.148	96.069	6.861	53.486	366.967	10.864	97.154	1055.48
PVT-CNTFET (Tabrizchi & Dehghani, 2021)	1.527	19.875	30.349	2.849	34.381	97.951	5.754	64.864	373.227
Proposed Full Adder 1	**0.275**	**15.857**	**4.3606**	**0.402**	**30.875**	**12.411**	**1.347**	**59.386**	**79.992**
Proposed Full Adder 2	0.297	19.682	5.845	0.438	36.284	15.892	1.562	67.495	105.427
Proposed Full Adder 3	0.584	22.895	13.370	0.936	40.852	38.237	2.197	78.562	172.600
Proposed Full Adder 4	0.527	23.458	12.362	0.893	42.381	37.846	1.961	81.493	159.807

The proposed 32-bit parallel adder, using the current sink-based design, achieves a propagation delay of 59.386 Ps, outperforming D-CNTFET, Modified Current Sink, and Modified Current Source Restorer adders. In contrast, the Hybrid and SCMOS-CNTFET adders exhibit the highest delay. This superior delay performance highlights the current sink-based adder's capability for faster computation and reduced processing time.

Among the 32-bit PA designs, both the BBL-PT and proposed current sink-based adders demonstrate superior power efficiency with lower power consumption. However, the BBL-PT adder has a higher propagation delay of 95.517 Ps, trading off speed for power savings. In contrast, the CPL and CNTAFS designs exhibit the highest power consumption. The proposed current sink-based 32-bit adder achieves an impressive Power-Delay Product (PDP) of 79.992 aJ, outperforming all other designs by balancing power consumption and delay for superior efficiency. In contrast, the SCMOS-CNTFET and CNTAFS adders have the highest PDP values among the evaluated designs.

The performance analysis of 8-bit, 16-bit, and 32-bit parallel adders in terms of power consumption, delay, and PDP is shown in Figures 18–20. The proposed PA (current sink based) and BBL-PT parallel adders exhibit lower power consumption than other designs, with BBL-PT at 1.186 µW and the proposed 32-bit adder at 1.347 µW. Although the proposed design shows slightly higher power consumption, it remains competitive in efficiency.

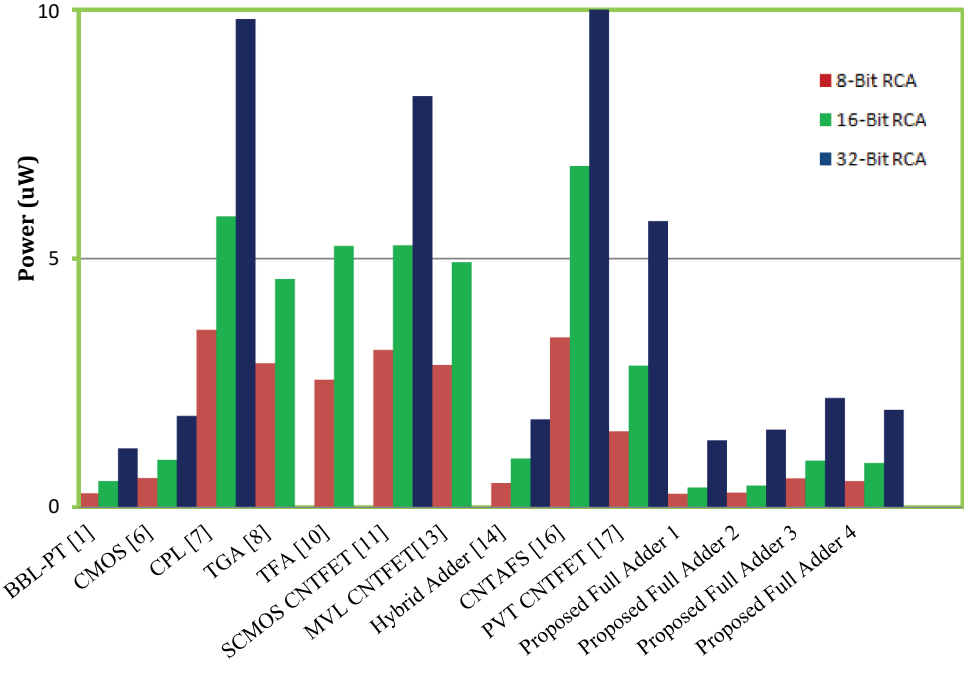


Figure 18. Performance comparison of proposed and alternative implementations of parallel adder's for power consumption.

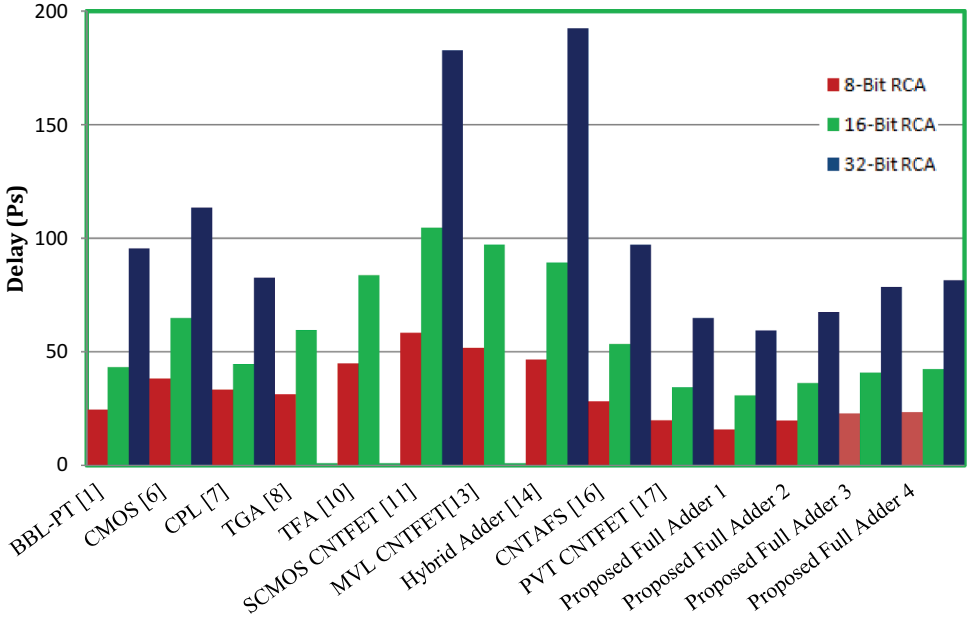


Figure 19. Performance comparison of proposed and alternative implementations of parallel adder's for delay.

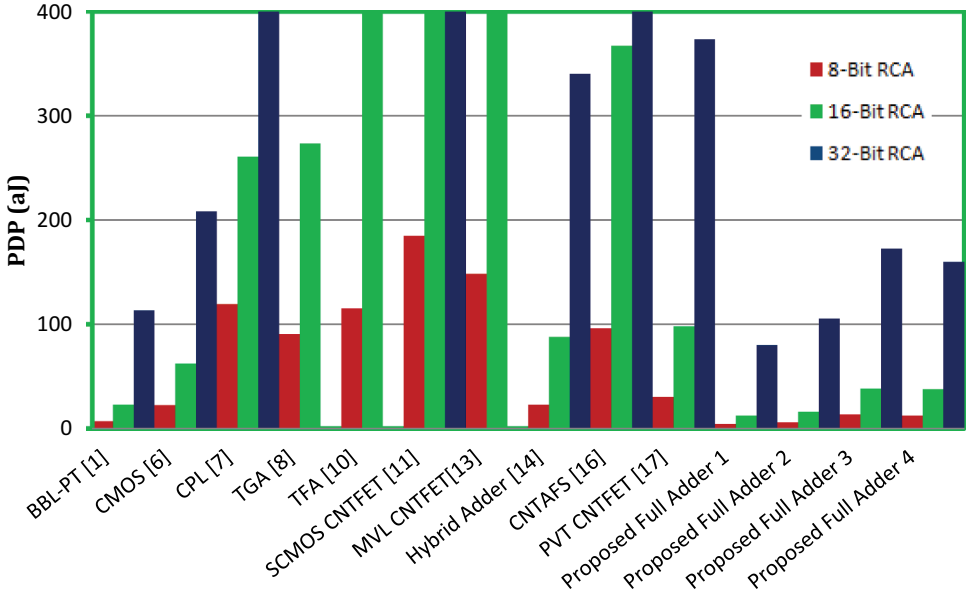


Figure 20. Performance comparison of proposed and alternative implementations of parallel adder's for PDP.

The performance evaluation of the proposed and alternative parallel adders was conducted using all possible input patterns to measure average power consumption and worst-case delay. Figure 20 presents the findings, with the proposed 32-bit PA (Current Sink Based) showing a PDP of 79.992 aJ, demonstrating its efficiency and advantages over other implementations.

A potential drawback of the proposed structures is their dependence on CNTFET technology, which, despite its benefits in power and delay, may pose integration challenges in current manufacturing processes. Additionally, the modified current sink and source structures may need extra design adjustments for compatibility. However, advancements in design automation tools and methodologies can help mitigate these challenges

The 32-bit PA (Current sink based) reports a delay of 59.386 Ps, power consumption of 1.347 μW, and a PDP of 79.992 aJ, indicating high energy efficiency and reduced heat dissipation. These results, summarised in Table 6, show that the proposed design outperforms existing alternatives with lower delay, power consumption, and PDP, highlighting its superior efficiency.

6. Conclusion

This paper introduces alternative modified level restorers for the BBL-PT full adder using current sink, D-CNTFET, modified current sink, and modified current source structures with 32-nm CNTFET technology. The proposed structures effectively eliminate the voltage step in existing design. Simulation results show that the proposed full adder circuits outperform most standard cells, achieving superior power efficiency (0.0845 μW), delay (6.127 Ps), and PDP (0.5177 aJ) at a supply voltage of +0.9 V. These advancements enhance the reliability and efficiency of full adder circuits, essential components in computing systems.

In addition to the individual performance improvements observed in the proposed full adders, the paper also presented the design of an N-bit PA ($N = 8$, 16 & 32) using the proposed full adders, showcasing the practical applicability of the proposed designs in terms of power, delay and PDP. The purpose of designing the N-bit PA is to assess the functional performance enhancements achieved in more complex circuits. The results obtained from the N-bit PA showcase good performance in terms of functional performance. Indeed, the intrinsic benefits of the proposed full adders and their associated improvements can be fully exploited when implementing high-performance complex structures.

Disclosure statement

No potential conflict of interest was reported by the author(s).

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