# Computer Architecture Lab

Shiraz University

## Homework

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# Introduction

**Your assignment is:**

- simulating Register file

registerfile.v
regFileTest.v

```
module registerFile(input [4:0] rs1, rs2, rd
                    input       clk, writeSignal
                    input [31:00] data
                    output[31:00] dataOut1, dataOut2
                   )
```

- simulating ALU

ALU.v
ALUTestBench.v

```
module ALU( input  [31:00] firstInput, secondInput,
            input  [03:00] alucontrol,
            output [31:00] ALUout,
            output         zero);
endmodule
```

# Register File:

- x0 register is always zero
- we have thirty two 32 bit registers
- you can change the rd register in negative edge of clock
- initial value of each register is zero

# ALU:

- in case you want to use always loop **ALUout** and **zero** should be reg data type
- for shift instruction only use **5 least significant** bits of **secondInput**
- don't forget to initialize reg date type

| ALU Ctr | Operation |
|---|---|
| 0000 | add |
| 0001 | sub |
| 0010 | xor |
| 0011 | or |
| 0100 | and |
| 0101 | not |
| 0110 | shift left logical |
| 0111 | shift right logical |
| 1000 | set less than |