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Electronic-Embedded Transformer Based DC Transformer with Trapezoidal Current and Natural Current Sharing

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***Abstract* – By incorporating an integrated low voltage full bridge [1], the concept of an electronic-embedded transformer (EET) offers a straightforward means of achieving high-frequency, high-power fixed-gain isolated DC-DC conversion, known as a DC transformer (DCX), through parallel operation of EET units with natural current sharing. However, EET-DCX, characterized by triangular transformer current, exhibits a higher root mean square (rms) value compared to the sinusoidal current in LLC/CLLC-DCX. To address this limitation, this research paper proposes a trapezoidal current modulation technique for EET-DCX.**

Through the implementation of trapezoidal current modulation, EET-DCX can effectively reduce the rms current by 15% and 11% when compared to triangular current EET-DCX and sinusoidal current CLLC-DCX, respectively. Consequently, this modulation scheme contributes to a noteworthy reduction of total conduction loss, encompassing both device and transformer winding losses, by 28% and 23%. Notably, the proposed trapezoidal current modulation retains all the advantages of previous EET-DCX designs, including natural current sharing, optimal operation at any frequency, load-independent voltage gain, simple open-loop control, and full load range zero voltage switching (ZVS). This letter provides an in-depth analysis of the proposed modulation technique, supported by verification on a 12-kW prototype featuring four parallel transformers.

To enhance understanding, two accompanying videos have been prepared to illustrate the current sharing behavior and frequency variation within the EET-DCX system. These visualizations provide valuable insights into the practical implementation and performance of the proposed trapezoidal current modulation approach.

***Index Terms* – trapezoidal current, dc transformer (DCX), natural current sharing, zero voltage switching (ZVS), electronic-embedded transformer (EET).**

I. Introduction

The increasing demand for high-frequency and high-power dc transformers (DCX) is being propelled by the rapid development of energy storage systems in renewable energy, microgrids, and transportation electrification. Resonant LLC/CLLC-DCX, characterized by its low circulating current and full load range zero voltage switching (ZVS), has emerged as a popular choice [2]-[10]. However, when transferring the same amount of real power, the sinusoidal current exhibits a larger root mean square (rms) current compared to a quasi-square current. Moreover, implementing a transformer-level parallel configuration in LLC/CLLC-DCX poses difficulties due to poor current sharing caused by small tolerances on the resonant tank. Consequently, scaling up the power rating becomes a challenging task. To overcome these limitations, a solution has been presented in [1], which introduces a scalable electronic-embedded transformer (EET) DCX with natural current sharing.

Fig. 1(a) illustrates the EET-DCX configuration, which enables the realization of transformer-level parallelism through the integrated low voltage (LV) bridge depicted in Figure 1(b). A comprehensive analysis of the EET-DCX, covering aspects such as natural current sharing, load-independent voltage gain,

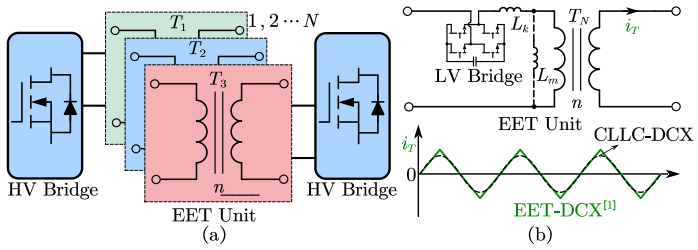

Fig. 1 Electronic-embedded transformer concept: (a) transformer-level parallel with multiple EET units, (b) EET unit circuit and the transformer current in [1].

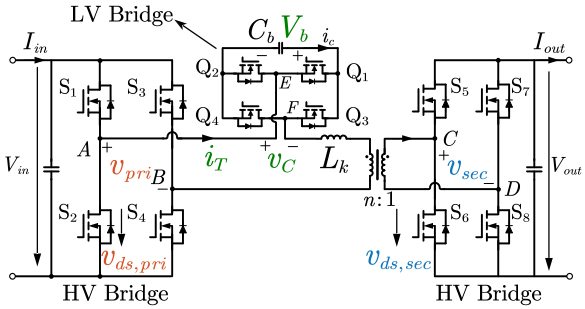

Fig. 2 Circuit diagram of EET-DCX with one EET unit.

simple open-loop control, and full load range zero voltage switching (ZVS), can be found in [1]. However, a remaining issue with the EET-DCX pertains to the triangular waveform of the transformer current, without considering the magnetizing inductance. In comparison to the sinusoidal current employed in typical CLLC-DCX, the triangular current depicted in Figure 1(b) exhibits a larger root mean square (rms) value. Consequently, this leads to higher conduction losses in both the devices and transformer windings. Notably, the device losses encompass the two high voltage (HV) bridges and multiple LV bridges within the EET units.

In order to mitigate the root mean square (rms) current in the EET-DCX, this research paper proposes a trapezoidal current modulation. The proposed approach maintains the same EET-DCX topology as described in [1] and introduces a simple open-loop phase shift to transform the transformer current from a triangular waveform to a trapezoidal waveform. By employing this modulation technique, the trapezoidal current exhibits smaller rms and peak values under the same power transfer conditions. As a result, this modulation not only reduces total conduction losses but also diminishes switching losses on the integrated LV bridge due to the lower peak current. Importantly, all the advantages associated with the triangular current modulation presented in [1], such as natural current sharing, load-independent voltage gain, and the absence of resonant point tuning requirements, are retained in this proposed trapezoidal current modulation. In summary, the previous triangular current modulation can be included as a special case within this newly proposed trapezoidal current modulation.

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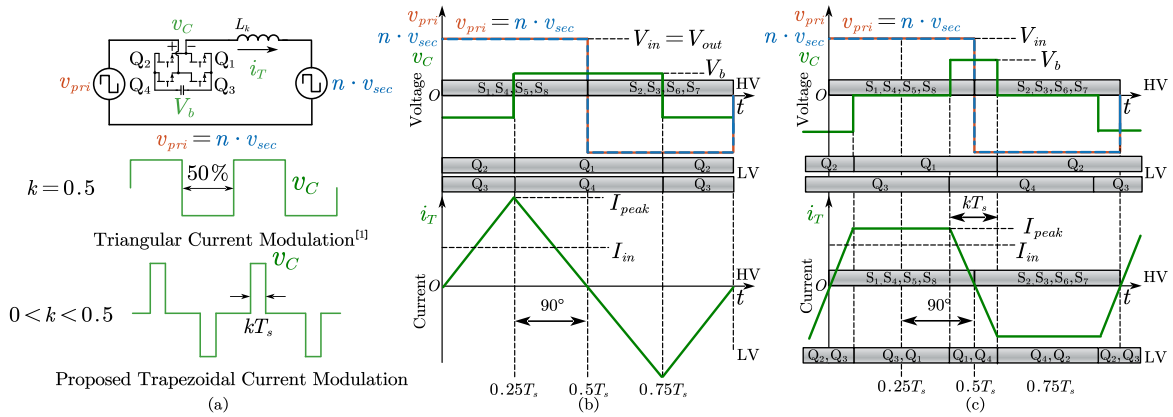

Fig. 3 (a) simplified EET-DCX circuit and related v_C waveforms. (b) previous triangular current modulation in [1], (c) proposed trapezoidal current modulation.

II. Trapezoidal Current Modulation for EET-DCX

Fig. 2 illustrates the circuit diagram of the EET-DCX with a single EET unit. The configuration comprises two HV bridges and one LV bridge integrated within a *n*:1 transformer. The diagram showcases various key elements: V_{in} and V_{out} denote the input and output voltages, while I_{in} and I_{out} represent the input and output currents, respectively. Additionally, v_{pri} and v_{sec} correspond to the output voltages of the two HV bridges. The floating dc voltage across C_b is denoted as V_b, and its amplitude will be further discussed and derived in subsequent sections. Furthermore, v_C indicates the LV bridge's output voltage with an amplitude equivalent to V_b. L_k represents the leakage inductance of the transformer, while i_T represents the current flowing through the transformer. It is worth noting that the magnetizing inductance is disregarded in this context as it exclusively pertains to the HV bridges' ZVS and is unrelated to the LV bridge's ZVS. Further details regarding the ZVS implementation of the HV bridges can be found in [1]. Considering the configuration in Fig. 2, it is worth noting that the two HV bridges can be simplified as two synchronized square voltage sources with a 50% duty cycle, as depicted in Fig. 3(a). Fig. 3(b) illustrates the detailed waveforms of voltage and current pertaining to the triangular current modulation. It is important to mention that this modulation technique has been extensively discussed in [1]. In the steady state, the relationship between V_{in} and V_{out}, I_{in} and I_{out}, as well as v_{pri} and v_{sec} can be directly determined based on the aforementioned analysis.

$$V_{in} = n \cdot V_{out},\ I_{in} = I_{out}/n,\ v_{pri} = n \cdot v_{sec} \tag{1}$$

Based on Eq. (1), it can be observed that when v_{pri} equals v_{sec}, only the voltage source v_C will be utilized to drive L_k, resulting in the generation of a triangular current waveform as shown in Figure 3(b). Consequently, the floating capacitor voltage V_b can be derived as follows:

$$V_b = 8 f_s L_k I_{in} \tag{2}$$

In Fig. 3(a), the v_C waveform in traditional triangular modulation is represented by 50% duty cycle square waveforms with an amplitude of V_b, as derived in Eq. (2). The corresponding gating signals for the LV bridge switches Q_1-Q_4 are depicted in Fig. 3(b). To transform the current waveform from triangular to trapezoidal, a zero-voltage stage (Q_1, Q_3 or Q_2, Q_4) needs to be introduced to v_C, creating a "current plateau" as illustrated in Fig. 3(a). This plateau can be achieved by introducing a phase shift of kT_s between the phase legs Q_1, Q_2, and Q_3, Q_4, as shown in Fig. 3(c). Alternatively, the phase shift *k* can be interpreted as the duty cycle of v_C, as illustrated in Fig. 3(a). The range of *k* varies from 0 to 0.5. Similar to the analysis conducted in triangular current modulation [1], the load-independent voltage gain derived from equation (1) remains valid in the trapezoidal current modulation.

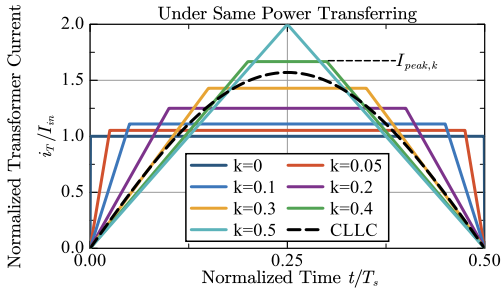

Fig. 4 Normalized transformer current i_T/I_{in} with different *k*.

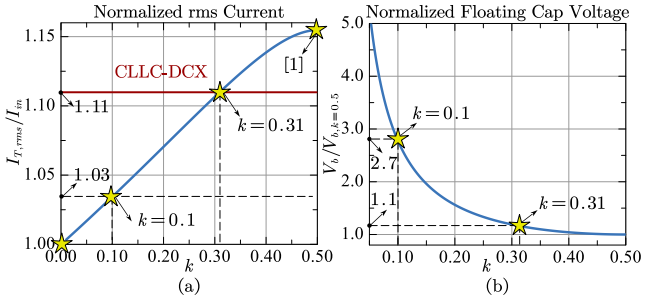

Fig. 5 (a) Transformer rms current $I_{T,rms}$, and (b) floating capacitor voltage V_b.

Fig. 4 illustrates the normalized transformer current i_T/I_{in} for various duty cycles (k) under the condition of the same power transfer. When $0 < k < 0.5$, the transformer current i_T exhibits a trapezoidal waveform. At $k = 0$, the current waveform transitions to the ideal square waveform. Conversely, triangular modulation can be regarded as a special case of trapezoidal modulation when k=0.5. Additionally, for comparison purposes, the resonant current from CLLC-DCX is represented as a dashed line, assuming the same power rating.

By employing the proposed trapezoidal current modulation, the peak current (I_{peak}), rms transformer current ($I_{T,rms}$), and voltage (V_b) can be re-derived as follows (detailed derivation for Eq. (1)-(5) and voltage ripple can be found in *Appendix*):

$$I_{peak} = \frac{1}{1-k} \cdot I_{in} \tag{3}$$

$$I_{T,rms} = \frac{1}{1-k} \cdot \sqrt{\frac{3-4\cdot k}{3}} \cdot I_{in} \tag{4}$$

$$V_b = \frac{2 f_s L_k}{(1-k)k} \cdot I_{in} \tag{5}$$

When k=0.5, these results align with the findings in [1] regarding triangle modulation. Fig. 5(a) presents the normalized rms current $I_{T,rms}$ from equation (4), based on I_{in}. Comparing it with the sinusoidal current ($1.11 \cdot I_{in}$) observed in CLLC-DCX, the rms current can be reduced by 8% and 11% for k=0.1 and 0,

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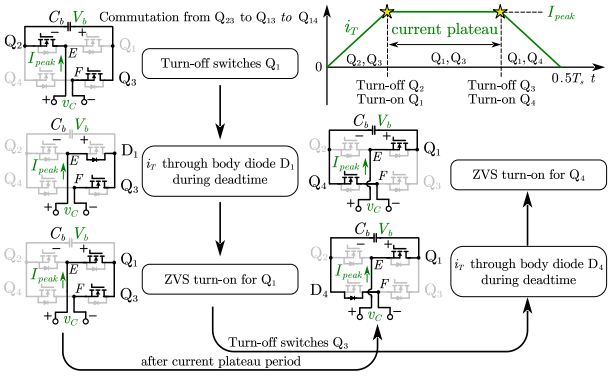

Fig. 6 ZVS analysis for LV bridge of EET-DCX with trapezoidal modulation.

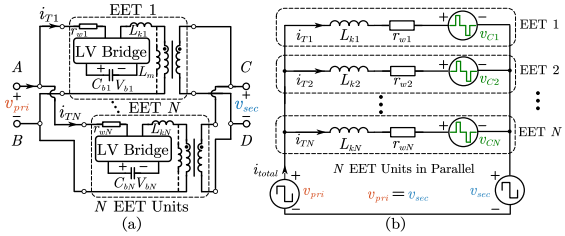

Fig. 7 Transformer-level parallel: (a) circuit diagram, (b) equivalent circuit.

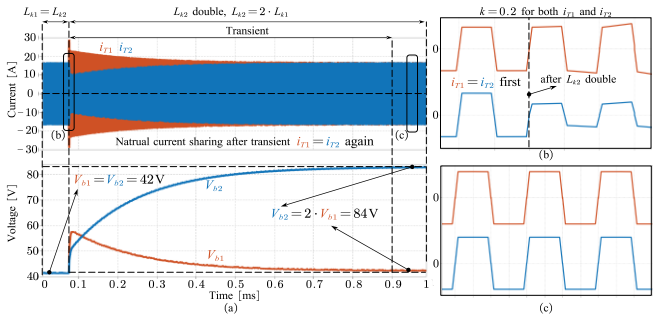

Fig. 8 Simulated waveforms: (a) currents and voltages in a large scale 1 ms, (b) currents when the transient L_{k2} doubled, (c) good current sharing after transient.

respectively. Notably, for k=0.1, the rms current is significantly reduced by 13% compared to the previous triangle modulation in [1] at k=0.5. At k=0.31, EET-DCX exhibits the same rms current as CLLC-DCX.

On the other hand, Fig. 5(b) illustrates the normalized voltage V_b based on $V_{b,k=0.5}$ from equation (2). The only drawback of trapezoidal current modulation is that V_b increases compared to triangular current modulation when k=0.5. For example, when k=0.31, 0.1, and 0.01, V_b increases by 1.1, 2.7, and 5 times, respectively. Therefore, there is a trade-off: as k approaches 0, the trapezoidal current becomes more like a square waveform with a smaller rms current, but it results in an increase in V_b across the floating dc capacitor. However, in practical scenarios, V_b is typically very small when the high-frequency transformer electromagnetic design is optimized to minimize the leakage inductance. For instance, when k=0.1, f_s=250 kHz, L_k=200 nH, and I_{in}=10 A, the value of V_b derived from Eq. (5) is approximately 10 V. This indicates that the increased V_b is acceptable when it leads to a reduction in rms current.

IV. Re-analysis for ZVS and Current Sharing

Fig. 6 illustrates a half-period current commutation process, showcasing the realization of zero-voltage switching (ZVS) for LV bridge switches Q_4 and Q_1. A similar mechanism applies to the other pair of switches, Q_2 and Q_3, during the other half period. Initially, during the transition from Q_2, Q_3 to Q_1, Q_3, switch Q_1 achieves ZVS as the current i_{peak} flows through the body diode D_1 before the switch turns on. Following the current plateau stage (zero stage Q_1, Q_3), switch Q_4 achieves ZVS using the same

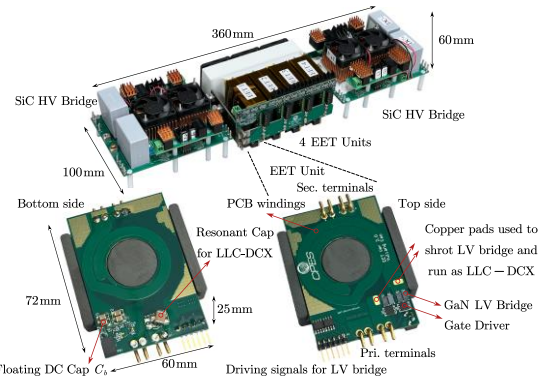

Fig. 9 The 12-kW prototype EET-DCX with four EET units.

TABLE I
Parameters of EET-DCX with Four EET Units

Variable	Value	Variable	Value
$V_{in(out)}$	300 V	C_b	20 µF
P	12 kW	f_s	250 kHz
L_k	184 nH	LV Switch	80V EPC 2029

process. It is important to note that achieving ZVS on the LV bridge is independent of the load since both i_{peak} and V_b are proportionate to the input current I_{in}, as determined by Eq. (3) and (5). Even under light load conditions, where i_{peak} decreases, the voltage across the LV bridge V_b also decreases, ensuring that the i_{peak} during the dead time is sufficient to achieve LV bridge ZVS.

Fig. 7(a) presents the transformer-level parallel configuration with multiple EET units, while the simplified equivalent circuit is depicted in Fig. 7(b). Each EET unit is associated with a winding resistance r_{wN}. Despite the introduction of a zero stage in v_{CN}, the fundamental component of v_{CN} still exhibits a 90-degree phase difference from v_{pri} or v_{sec}. Consequently, the impedance of the leakage inductance L_{kN} can be effectively canceled out by each LV bridge in series.

In Fig. 8, a simulation is presented with parameters k=0.2, f_s=250 kHz, V_{in}=V_{out}=300 V, $L_{k1(2)}$=200 nH, and I_{in}=I_{out}=30 A. The excellent current sharing is evident due to the equality of L_{k1} and L_{k2}, as observed from V_{b1}=V_{b2}=21 V (derived from Eq. (5)). At approximately 0.08 ms, a doubling of L_{k2} causes a temporary drop in current i_{T2}, as illustrated in Fig. 8(b). However, after a transient period, V_{b2} automatically adjusts to double its value, ensuring i_{T1}=i_{T2} is maintained, thereby confirming the natural current sharing characteristic of the proposed trapezoidal modulation.

V. Experimental Validation

To validate the analysis of trapezoidal modulation, a practical implementation of a 12 kW EET-DCX system was constructed, as depicted in Fig. 9. This system comprises four EET units operating in parallel. In comparison to the EET unit design described in [1], modifications were made to enable its operation as an LLC-DCX. Specifically, a resonant capacitor was introduced in series on the bottom side, and the entire LV bridge was shorted using two copper pads on the top side. Detailed parameters of the system can be found in Table I.

Fig. 10 presents the experimental results for each EET unit operating at full load of 3 kW. Fig. 10(a) showcases the outcomes of the LLC-DCX configuration, where the LV bridge was shorted, and an external resonant capacitor was incorporated. In Fig. 10(a)-(c), the results for trapezoidal modulation with k values of 0.5, 0.4, and 0.2 are displayed, respectively. As anticipated from the previous analysis, when k=0.5, the current waveform takes the shape of a triangle, while reducing k moves the waveforms closer to a square waveform, resulting in a smaller rms value as predicted by Eq. (4). Furthermore, as k decreases, V_b increases as indicated by Eq. (5).

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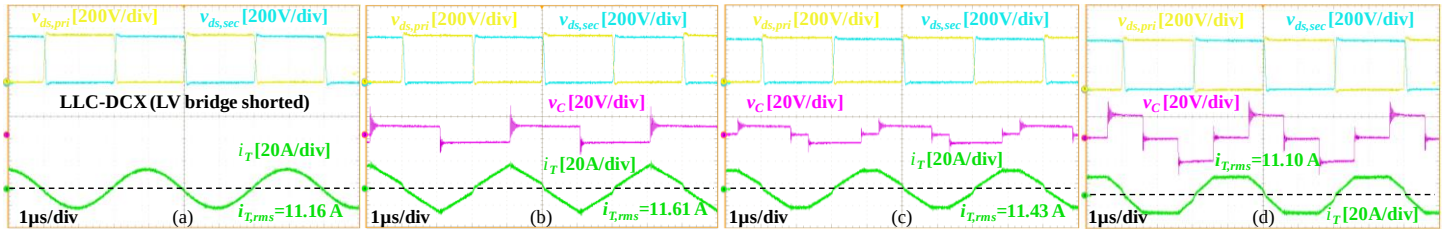

Fig. 10 Experimental results for each EET unit at full load 3 kW: (a) LLC-DCX configuration. LV bridge was shorted, and resonant capacitor was added. (b) k=0.5, previous triangular current modulation in [1], (c) k=0.4, (d) k=0.3. ***Video A* was attached to visualize the procedure when k is changed from 0.1 to 0.5.**

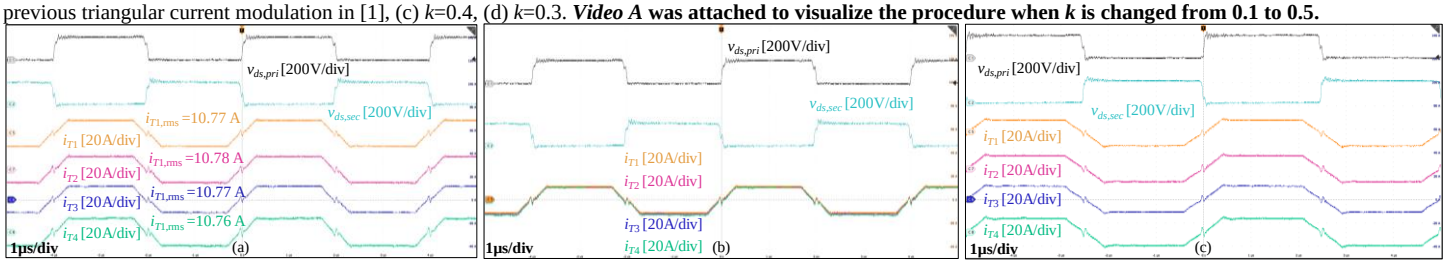

Fig. 11 Experimental results for current sharing at full load 12 kW with 4 EET units paralleled: (a) k=0.2, f_s=250 kHz with stacked waveforms, (b) k=0.2, f_s=250 kHz with overlapped waveforms, (c) k=0.2, f_s=200 kHz with stacked waveforms. ***Video B* was attached to visualize the procedure when f_s changes from 250 to 200 kHz.**

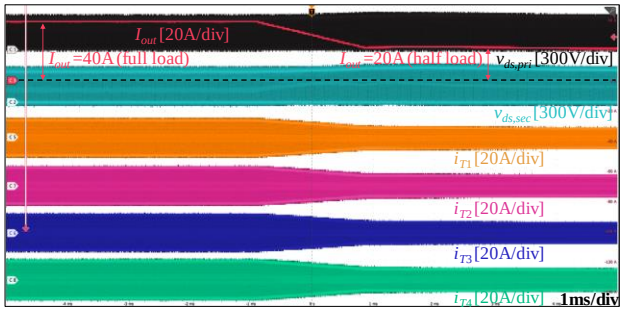

Fig. 12 Load changing test from full load (12 kW) to half load (6 kW).

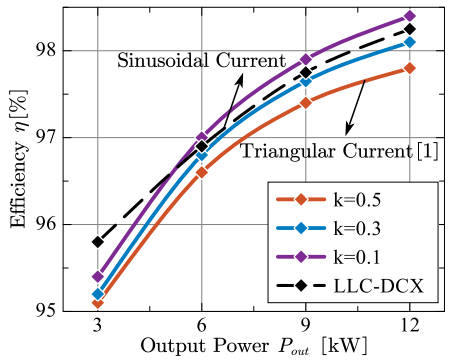

Fig. 13 EET-DCX Efficiency with different k.

Fig. 11 presents the experimental results of current sharing when operating at full load of 12 kW with four EET units in parallel. In Fig. 11(a) and (b), it can be observed that at a switching frequency of 250 kHz with k=0.2, the current sharing is excellent, with $i_{T1\text{-}4}$ closely matching each other after overlapping. Similarly, Fig. 11(c) demonstrates the favorable current sharing results when the switching frequency is adjusted from 250 to 200 kHz while maintaining k at 0.2. Unlike LLC-DCX, which necessitates resonant point tuning, EET-DCX employing trapezoidal current modulation can achieve optimal performance at any frequency.

It is worth noting that the small distortion on the transformer current is caused by the resonance between HV bridges device output capacitance and transformer leakage inductance. The measurement rms current $I_{T,rms}$ can be found in both Fig. 10 and 11(a) with k=0.5, 0.4, 0.3, and 0.2, respectively. Compared with the ideal value from Eq. (4), this distortion impact on the rms current can be ignored.

The load changing test, transitioning from full load of 12 kW to half load of 6 kW, is illustrated in Fig. 12. Notably, the current sharing remains satisfactory throughout the transient period, demonstrating the robustness of the system.

Fig. 13 presents the efficiency results for various values of k. To provide a benchmark, the efficiency of the resonant LLC-DCX (98.25% at 12 kW) is included. When k=0.5, the triangular current waveform still exhibits a higher rms current compared to the sinusoidal current of the LLC-DCX. However, as k approaches 0, for instance, when k=0.1, the EET-DCX achieves a higher efficiency (98.4% at 12 kW) due to the reduced rms current and total conduction loss. It is important to highlight that this reduction in conduction loss not only applies to the transformer windings but also encompasses the conduction loss of the HV bridge devices. This aspect is particularly advantageous in high-current, high-power applications, as the additional loss on the LV bridge becomes less significant in comparison.

V. Conclusion

This letter introduces a novel trapezoidal current modulation technique for EET-DCX, which offers significant advantages such as a considerable reduction in rms current while preserving key features like natural current sharing, load-independent voltage gain, and full load range zero-voltage switching (ZVS). When compared to state-of-the-art LLC/CLLC-DCX topologies, the proposed approach can achieve up to a 23% reduction in total conduction loss. This reduction in conduction loss enables more compact transformer designs. Additionally, thanks to the inherent current sharing characteristic, the power rating of EET-DCX can be easily scaled up by parallel connection of modular transformers. Notably, the proposed technique eliminates the need for resonant point tuning, simplifying system design and operation.

Finally, the effectiveness of the proposed trapezoidal current modulation technique and its corresponding analysis are validated through experimentation on a 12 kW EET-DCX prototype comprising four paralleled EET units. In order to provide a fair comparison with LLC-DCX, the EET unit is re-designed and re-configured to operate as an LLC-DCX, ensuring an unbiased evaluation. Remarkably, under full load conditions, EET-DCX with trapezoidal current modulation exhibits higher efficiency than LLC-DCX. This promising outcome demonstrates the significant potential of the proposed method to enhance the performance of DCX systems employed in high-power and high-density applications, such as electric vehicle charging systems and solid-state transformers.

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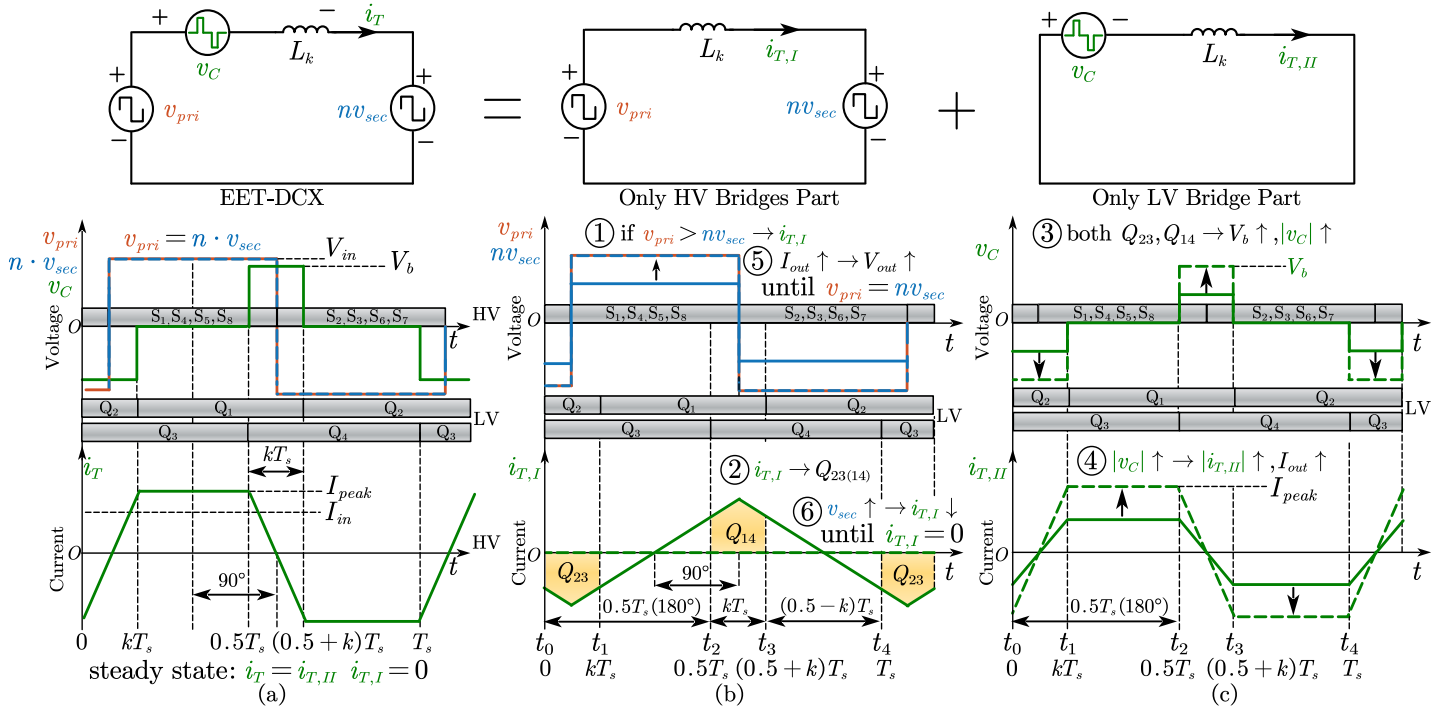

Fig. A1 Procedure of the robust load-independent voltage gain: (a) whole EET-DCX (b) only HV bridge part, and (c) only LV bridge part.

APPENDIX

To illustrate the robust independent voltage gain of EET-DCX in Eq. (1), Fig. A1 shows the whole procedure with a certain load. Based on superposition principle, EET-DCX shown in Fig. A1(a) can be decomposed of two parts: one is HV bridges part shown in Fig. A1(b), another is LV bridge part depicted in Fig. A1(c). The operation principle of this open-loop robust load-independent voltage gain (V_{in}=nV_{out}) can be explained as six steps:

***Step* 1:** Assuming V_{in} is larger than nV_{out} as shown in Fig. A1(b), the voltage difference (V_{in}-nV_{out}) will be applied to L_k directly, and the triangular current $i_{T,I}$ will have a 90-degree phase shift from v_{pri} or v_{sec}. Obviously, due to this 90-degree phase shift, there is no real power delivered to the receiving side by $i_{T,I}$.

***Step* 2:** Since the current $i_{T,I}$ in Fig. A1(b) is in phase of the voltage v_C in Fig. A1(c), it will always charge the floating dc capacitor C_b alternatively. For example, from t_0 to t_1, the current $i_{T,I}$ keeps negative as shown in Fig. A1(b), and at the same time LV switches Q_2 and Q_3 is ON. Therefore, the electric charge Q_{23} shown in Fig. A1(b) will charge C_b. As for another half period from t_2 to t_3, positive $i_{T,I}$ will generate electric charge Q_{14} to charge the floating dc capacitor C_b. To sum up, in one cycle, Q_{23} will be equal to Q_{14} and always increase the amplitude of v_C.

***Step* 3:** If V_{in} is larger than nV_{out}, Q_{23} and Q_{14} generated from current $i_{T,I}$ will always increase amplitude of v_C during the whole period.

$$i_{T,I} \rightarrow Q_{23}, Q_{14} \rightarrow V_b \uparrow, |v_{rc}| \uparrow \tag{A1}$$

***Step* 4:** As depicted in Fig. A1(c), with only one voltage source excitation v_C, trapezoidal current $i_{T,II}$ can be derived as

$$i_{T,II}(t) = \begin{cases} -I_{peak} + \dfrac{V_b}{L_k} \cdot t & t \in [0,\ kT_s] \\ I_{peak} & t \in [kT_s,\ 0.5T_s] \end{cases} \tag{A2}$$

where I_{peak} is the peak value of i_T, and the range of k is from 0 to 0.5. With an increase of V_b from Eq. (A1), the amplitude of current $i_{T,II}$ will become larger as shown in **Fig. A1(c)**. On the other hand, the power $P_{T,II}$ delivered to the receiving side by $i_{T,II}$ can be given as

$$P_{T,II} = \int_0^{T_s} n \cdot v_{sec}(t) \cdot i_{T,II}(t) \tag{A3}$$

Since v_{sec} is always in phase of $i_{T,II}$, with a larger $i_{T,II}$ shown in dash line in **Fig. A1(c)**, more real power $P_{T,II}$ will be delivered to the receiving side.

***Step* 5:** If the receiving power increases with a certain load, the corresponding output voltage V_{out} will increase until nV_{out} is equal to V_{in}.

$$I_{out} \uparrow \rightarrow V_{out} \uparrow, |v_{sec}| \uparrow \text{ until } n \cdot V_{out} = V_{in} \tag{A4}$$

***Step* 6:** Meanwhile, assuming V_{in} is constant, an increasing V_{out} will lead to a smaller current $i_{T,I}$ until nV_{out} is equal to V_{in}.

To sum up, the robust load-independent voltage gain (V_{in}=nV_{out}) of EET-DCX in Fig. A1 can be expressed as Eq. (A5).

$$\begin{cases} V_{in} > nV_{out} & i_{T,II} \rightarrow |v_{rc}| \uparrow \rightarrow I_{out} \uparrow \rightarrow V_{out} \uparrow \\ V_{in} = nV_{out} & i_{T,II} = 0 \rightarrow \text{const } V_b, I_{peak},\ I_{out},\ V_{out} \\ V_{in} < nV_{out} & i_{T,II} \rightarrow |v_{rc}| \downarrow \rightarrow I_{out} \downarrow \rightarrow V_{out} \downarrow \end{cases} \tag{A5}$$

When nV_{out} is equal to V_{in}, current $i_{T,I}$ will be equal to zero, and the voltage and current values V_b, I_{peak} should keep as constant, which means the EET-DCX has entered the steady state.

And then, the derivations of Eq. (3)-(5) are illustrated below. As shown in Fig. A1, in the steady state, i_T is in phase of v_{pri} or v_{sec}, and the input dc current I_{in} should be equal to the average current in half period from $0.5kT_s$ to $(0.5+k)T_s$.

$$I_{in} = \text{average current} = \frac{2}{T_s}\int_{0.5kT_s}^{(0.5+0.5k)T_s} i_T(t) \cdot dt \tag{A6}$$

In addition, from t_0 to t_1 or t_2 to t_3, the current commutation for i_T should be finished in kT_s as shown in Fig. A1. During this commutation, the value of current i_T will be changed from - I_{peak} to I_{peak} or I_{peak} to -I_{peak}. Therefore, another constraint between I_{peak} and V_b can be given as

$$2I_{peak} = \frac{V_b}{L_k} \cdot kT_s \tag{A7}$$

From Eq. (A2), (A6), and (A7), Eq. (3) and Eq. (5) can be derived first. After obtaining Eq. (3) and (5), the rms current of i_T in Eq. (4) can be derived based on the definition.

$$I_{T,rms} = \frac{1}{T_s}\sqrt{\int_0^{T_s} {i_T}^2(t)\,dt} = \frac{1}{1-k} \cdot \sqrt{\frac{3-4\cdot k}{3}} \cdot I_{in} \tag{A8}$$

where the time-domain expression $i_T(t)$ can be found in Eq. (A2). In addition, based on Fig. A1, the voltage ripple on dc floating Vb can be given as

$$\Delta V_b/V_b = \frac{k^2}{4{f_s}^2 L_k C_b} \tag{A9}$$

From Eq. (A9), compared to the triangular current modulation (k=0.5) in [1], the proposed trapezoidal current modulation can also reduce the voltage ripple (0<k<0.5).

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