Design of Ring-Oscillator-Based Injection-Locked Frequency Dividers With Single-Phase Inputs

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***Abstract*—Ring-oscillator-based injection-locked frequency divider has merits of compact and low power. The multi-phase injection can improve its locking range, but it needs specific multi-phase inputs, which limits the application of this technique. We present a symmetrical injection circuit to generate the multi-phase injection with only single-phase input. Two injection-locked frequency dividers, with divide-by-3 and divide-by-5 operations respectively, were fabricated in 0.18 μm CMOS technology to verify the proposed design. The locking range of divide-by-3 and divide-by-5 dividers are 1.6 GHz and 0.9 GHz, with 0.24 and 0.7 mW power consumption in 1 V supply voltage, respectively.**

***Index Terms*—Frequency divider, injection-locked, ring oscillator, multi-phase injection.**

I. Introduction

HIGH speed frequency dividers are critical building blocks in phase-locked loops (PLLs) for modern wireless communication [1]. The challenges of frequency divider design are high operation frequency, wide locking range, low power consumption, and low cost. The static frequency dividers prevail in CMOS technology, but they consume a lot of power when operating at high frequency [2]. In recent years, the injection-locked frequency dividers (ILFDs) have attracted much attention for their high frequency and lower power consumption [3]–[11]. Since the ILFDs are based on the injection-locked oscillators, there are two types of ILFDs. The first one is LC-oscillator-based ILFD, which can operate at very high frequency with low power consumption, but its locking range is narrow and the area is too large due to the LC tank. Secondly, the ILFD can be based on RC ring oscillator, which has the merits of low power, large locking range, and small area. Many literatures have been published to study the ring-oscillator-based ILFD [3]–[5]. [4] and [5] both demonstrated that multi-phase injection with a specific phase difference can maximize the locking range of the ring-oscillator-based ILFD. However, the multi-phase inputs are difficult to be obtained directly in conventional LC differential voltage-controlled oscillator (VCO). In addition, the locking range will become worse if the phase difference of inputs departs from the optimum value [4]. These defects prevent the application of multi-phase injection technology in ILFD.

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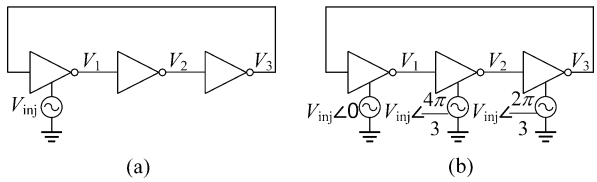

Fig. 1. Schematics of (a) conventional single-phase and (b) multi-phase ring-oscillator-based ILFDs.

In this letter, we propose a technique to avoid these problems. Since the multi-phase always exists in ring oscillator inherently, the multi-phase injection can be generated in the symmetrical injection circuit by using single-phase input. As a result, we can achieve the wide locking range with only single-phase input. The analysis of proposed design will be discussed. Two circuits adopting this technique, with division ratio of 3 and 5 respectively, have been implemented in 0.18 μm CMOS technology to demonstrate our proposed design.

II. Analysis of Proposed Design

To explain our proposed design, let us start with the conventional three-stage ring-oscillator-based ILFD, as shown in Fig. 1. Assuming that the gain of each stage is sufficiently large, only the phase condition of Barkhausen criteria needs to be taken into account. Without injection, the ILFD operates at free running frequency, and the load at each stage provides a $\pi/3$ phase shift to satisfy the phase condition. When the ILFD achieves the state of locking, the phase shift provided by the load will change. Meanwhile, the frequency of ILFD will shift to a new value, that is $\omega_{\rm inj}/3$ in divide-by-3 case. An extra phase shift must be generated by injection current to compensate the change of the phase shift provided by the load, so as to meet the phase condition again. For conventional single-phase injection, as depicted in Fig. 1(a), the locking range of the ILFD is narrow since the extra phase shift around the loop is generated by only one injection. As for multi-phase injection, the extra phase shift can be provided by multiple injection currents, as shown in Fig. 1(b). The locking range of this ILFD will be widened if the phase of the injections progress with the ring oscillator's intrinsic delays. However, as mentioned previously, the requirement of specific multi-phase inputs makes this technique impractical in low power application.

We analyze the proposed divide-by-3 ILFD, as shown in Fig. 2, to demonstrate our idea. The concept of this prototype can be applied to other ring-oscillator-based ILFDs. Each node $V_i(i = 1,2,3)$ is connected to every other node in the ring oscillator through an injection transistor to form a symmetrical injection circuit. The gate input signals of all injection transistors are $V_{\rm inj}$. $C_{{\rm p},i}$ represents the parasitic capacitance in

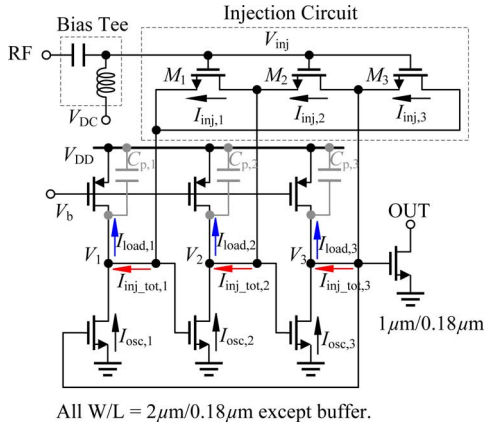

Fig. 2. Schematic of proposed divide-by-3 ILFD.

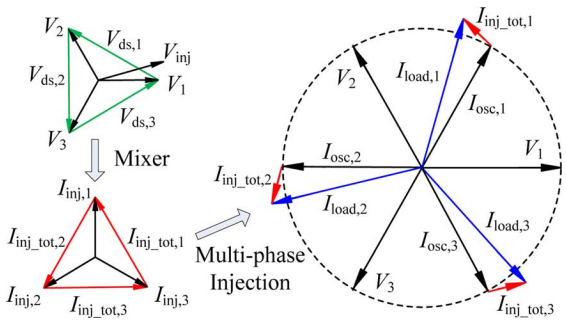

Fig. 3. Voltage and current phasors relationship of proposed divide-by-3 ILFD.

the node V_i. In the qualitative analysis, the injection transistor can be treated as a mixer. Assuming that the injection voltage is $V_{\rm inj} = V_{\rm DC} + A_{\rm inj}\cos(\omega_{\rm inj}t + \varphi_{\rm inj})$, where $V_{\rm DC}$, $A_{\rm inj}$, and $\varphi_{\rm inj}$ is the dc voltage, amplitude, and phase of injection signal respectively. The voltage at each oscillation node V_i is $\cos(\omega t + \varphi_i)$, where $\varphi_i = (i-1)(2\pi/3)$, as shown in Fig. 3 (upper left). So the drain-source voltage of M_i is $V_{{\rm ds},i} = \sqrt{2}\cos(\omega t + \varphi_{{\rm ds},i})$, where $\varphi_{{\rm ds},i} = (4i+1)(\pi/6)$. Note that both φ_i and $\varphi_{{\rm ds},i}$ form the angle of $2\pi/3$ with different i. Thus, the injection current generated by M_i through mixing can be described as

$$I_{{\rm inj},i} = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} a_{mn}\cos(m\omega_{\rm inj}t + m\varphi_{\rm inj}) \times \cos(n\omega t + n\varphi_{{\rm ds},i}) \quad (1)$$

where a_{mn} is an intermodulation transconductance coefficient of the mixer, and $\omega_{\rm inj} = 3\omega$ in the case of divide-by-3. Because other harmonics will be suppressed by the intrinsic low-pass filter in the loop of ring oscillator, we only need to consider the fundamental current, that is, $|m\omega_{\rm inj} \pm n\omega| = \omega$. For simplicity, only the terms with $m = 0$, $n = 1$, and $m = 1$, $n = 2, 4$, are taken into consideration. Therefore, (1) can be expanded as

$$I_{{\rm inj},i} = \frac{a_{01}}{2}\cos(\omega t + \varphi_{{\rm ds},i}) + \frac{a_{12}}{2}\cos(\omega t + \varphi_{\rm inj} - 2\varphi_{{\rm ds},i}) + \frac{a_{14}}{2}\cos(\omega t - \varphi_{\rm inj} + 4\varphi_{{\rm ds},i}). \quad (2)$$

For each $I_{{\rm inj},i}$ in (2), the parameters a_{01}, a_{12}, a_{14}, and $\varphi_{\rm inj}$ are the same, and only $\varphi_{{\rm ds},i}$ is different. $I_{{\rm inj},1}$, $I_{{\rm inj},2}$, and $I_{{\rm inj},3}$ have the same amplitude and form the angle of $2\pi/3$ with each other. To simplify the qualitative analysis, we assume that the current $I_{{\rm inj},i}$ flows from drain to source. As shown in Fig. 3 (lower left), the total current injected into the node V_i will be

$$|I_{{\rm inj\_tot},i}| = \sqrt{3}|I_{{\rm inj},i}| \quad (3)$$

and the angle between each $I_{{\rm inj\_tot},i}$ is also $2\pi/3$. Therefore, the phase of the total injection currents progress with the intrinsic phase in the ILFD. In other words, the injection can be considered as multi-phase injection, as depicted in Fig. 3 (right). Through the same derivations, it can be shown that multi-phase injection cannot be achieved in divide-by-2 operation in the proposed three-stage ILFD, which is confirmed through simulation.

We assume that the injection current $I_{{\rm inj},i}$ is much smaller than the oscillation current $I_{{\rm osc},i}$. By using the same method in [4], the one-sided locking range for our proposed divide-by-3 ILFD at the fundamental frequency can be derived as

$$\frac{\Delta\omega}{\omega_o} \le 4\left|\frac{I_{\rm inj}}{I_{\rm osc}}\right| \cdot \left(1 - 3\left|\frac{I_{\rm inj}}{I_{\rm osc}}\right|^2\right)^{-\frac{1}{2}}. \quad (4)$$

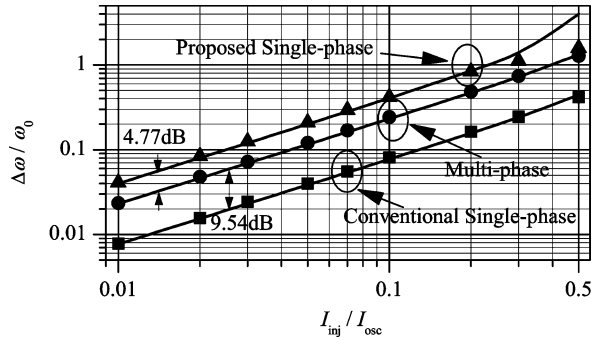

Fig. 4. Comparison of the locking range of divide-by-3 ILFDs: theory (solid line) and simulation (symbol).

Fig. 4 compares the locking range of three types of divide-by-3 ILFDs. The three ILFDs were simulated in Cadence Spectre by using the same dimension, power consumption, and ideal injection currents. Note that the theoretical results show good agreement with the simulation for small injection. Compared with multi-phase injection three-stage ILFD, the locking range of the proposed three-stage ILFD has been improved by 4.77 dB $(20\log(\sqrt{3}))$. In fact, the injection current $I_{\rm inj}$ is heavily limited by the nonlinear function of injection transistor, especially in high order superharmonic ILFDs. When the division ratio becomes larger, the locking range decreases quickly in ILFD [4], [5]. Fortunately, the number of injection transistors in our proposed N-stage ILFD is $N(N-1)/2$, which increases rapidly with N. Therefore, even while the division ratio is large, the injection efficiency will not degrade severely since more currents can be injected into the ILFD.

III. Experimental Results

Two circuits have been designed and fabricated in GLOBALFOUNDRIES 0.18 μm CMOS technology to demonstrate our proposed design. Figs. 2 and 5 show the schematics of divide-by-3 ILFD and divide-by-5 ILFD, respectively. In both ILFDs, the single-end delay cell is designed as a nMOS inverter with a pMOS current-source load. A simple open-drain nMOS inverter is used for the output buffer. Note that the bodies of all

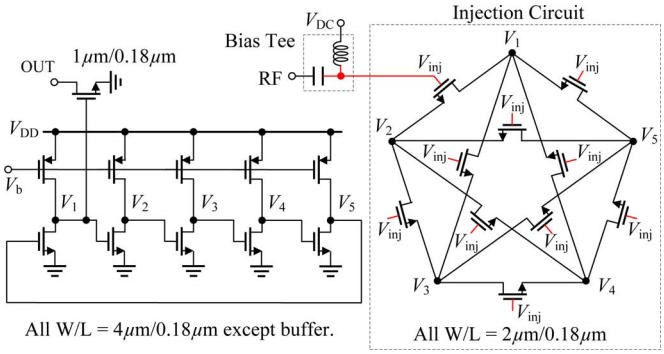

Fig. 5. Schematic of proposed divide-by-5 ILFD.

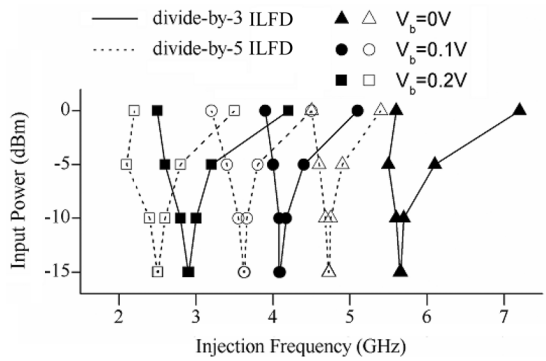

Fig. 6. Measured input sensitivity of proposed ILFDs when $V_{\rm DD} = 1$ V and $V_{\rm DC} = 0.3$ V.

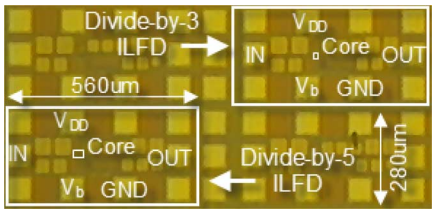

Fig. 7. Die photograph of proposed ILFDs.

nMOS (pMOS) transistors are connected to ground ($V_{\rm DD}$). The external bias voltages of pMOS load, $V_{\rm b}$, is used to tune ILFD's free running frequency. To realize a large modulation conductance of injection transistors, the dc voltage of injection signal, $V_{\rm DC}$, is set to 0.3 V as the optimize value. The supply voltage $V_{\rm DD}$ is set to 1 V, and can be further reduced to 0.8 V.

The input sensitivity of divide-by-3 ILFD and divide-by-5 ILFD operating at 1 V supply voltage are depicted in Fig. 6. When $V_{\rm b} = 0$ V, the locking frequency is from 5.6 to 7.2 GHz and the power consumption is 0.24 mW for divide-by-3 ILFD. In divide-by-5 ILFD, thanks to the 10 injection transistors, its locking frequency is from 4.5 to 5.4 GHz and the power consumption is 0.7 mW while $V_{\rm b} = 0$ V.

Fig. 7 shows the die photograph of proposed ILFDs. The core circuits of divide-by-3 ILFD and divide-by-5 ILFD occupy only 130 μm^2 and 800 μm^2 respectively. The performance of our ILFDs are compared with other similar RC ILFDs in CMOS technology, as summarized in Table I.

TABLE I
COMPARISON WITH OTHER RC ILFDS IN CMOS TECHNOLOGY

Ref.	Tech. (μm)	$V_{\rm DD}$ (V)	Div. Ratio	Locking Frequency* (GHz)	Power (mW)	FOM*** (GHz/mW)
[6]	0.18	1.0	3	2.51–3.50	0.4	8.75
[7]	0.18	1.8	3	4.85–5.7	12.51	0.46
[8]	0.18	1.8	3	8.28–11.48	12.5	0.92
[9]	0.18	1.8	3	1.2–4.9	0.74	6.62
	0.18	1.8	7	1.4–4.4	0.88	5
[10]	0.065	1.2	7	4.1–5.1	0.516	9.88
[11]	0.13	1.5	3	24.1–30.8	13	2.37
This work	0.18	1.0	3	5.6–7.2**	0.24	30
	0.18	1.0	5	4.5–5.4**	0.7	7.71

* Without tuning.
** $V_{\rm b} = 0$ V.
*** FOM = Maximum operating frequency / Power [3].

IV. CONCLUSION

In this letter, we improve the locking range in conventional single-phase injection ILFD by introducing symmetrical injection structure. Analysis reveals that the proposed design can realize multi-phase injection with only single-phase input. Two ILFDs, with division ratio of 3 and 5, respectively, were designed and implemented to verify our analysis. Measurement results show that our design can achieve a reasonable performance with low power and small area.

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