Design an LNA in the 65 nm CMOS process with at least 15 dB of voltage gain (measured in a 50Ω system) roughly following the procedure for simultaneous noise and power matching (inductive degeneration, inductor in series with input).

- Center Frequency≈ (12326MHZ
- Noise figure≤2.3 dB (use rf transistors as these include realistic parasitic and noise models).
- IIP3≥ -15 dBm and (one-tone) 1dB compression point -25 dBm.
- Supply Voltage =1.0V
- S11 ≤ -15 dB at the center frequency.
- |Zout| should be less than 30, but does not need to be matched.
- Total current should be as low as possible (attempt to reduce if all specs are met).
- Stability must also be considered.
- Layout, component pads and symmetry to be considered.

All inductors, resistors and capacitors must come from the process design kit. Limit on- chip capacitor size to 20 pF and on-chip resistors to 20 kΩ. Schematics should ONLY include kit components.

To include the effects of packaging, each DC suppl y (V bias, V dd, Gnd) must be loaded with a pad, a 3nH inductor with Q=30. Decoupling capacitors for on-chip AC grounds at the DC pads.

The report will include a layout floorplan of all schematic components in the LNA. You will not be required to run post-layout simulations but the layout should look as complete as possible with pads, interconnects (to meet DC current density requirements) and with symmetry and matching when required. Whenever possible, the final schematic should be corrected to include the effects of layout, i.e. inductor proxi mi ty can be model ed with coupling coefficients, include pad capacitance for inputs, outputs and DC supplies and account for critical interconnect resistances for DC supply lines, etc.

Y our report should contain a description of component characterization for transistors and inductors. It should also include some description of the design steps and design tradeoffs used in achieving the required specifications. You should also include a comparison of your results (e.g., noise figure, linearity, power dissipation and gain) to theory.

Remember, well written reports that get the point across quickly and concisely are best. Please include a front-page executive summary, e. g., in table form, of the final design and comparison to specifications and calculations. Make sure to include all final component values, circuit parameters, and bias information. Make sure figures are well labeled, and text on the figures can be read.

Notes for report submission

- All schematics must include ONLY kit components and I/O ports and have a sheet border with design details. Schematics must contain annotations on design states, transistor matching and DC currents. No DC, AC, transient or S-parameter Sources/Sinks are allowed in the schematic.
- All schematics will be tested on a separate test bench and have a sheet border with annotation of simulations states and switches.
- Be concise, use tables and/or plots to effectively present your results.