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FPGA-Based Low-Cost Architecture for R-Peak Detection and Heart-Rate Calculation Using Lifting-Based Discrete Wavelet Transform

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Abstract

This paper focuses on designing a field-programmable gate array (FPGA)-based architecture for R-peak detection and heart rate calculation using lifting-based discrete wavelet transform (DWT). An efficient and low-cost architecture for Daubechies 4 lifting-based DWT for a decomposition level of four is also proposed. The proposed architecture is folded after the first decomposition level to avoid repetitive blocks for different decomposition levels. The noise-removal and preprocessing of the electrocardiogram (ECG) signals are carried out using lifting-based DWT. The 16-bit fixed-point representation is employed throughout the design to reduce the hardware complexity. The entire design is evaluated in both MATLAB R2020a and XILINX VIVADO 2017.4. The proposed architecture is validated using three ECG databases, namely the MIT-BIH arrhythmia, the MIT-BIH supraventricular, and the QT database. A total of 122 distinct ECG datasets are tested on FPGA to determine the effectiveness of the proposed R-peak detection architecture. The R-peaks detected using the proposed technique show no noticeable error with respect to actual R-peaks. The FPGA implementation is performed using the Artix-7 board that utilizes 2197 LUTs and 486 flip-flops at an operating frequency of 44 MHz. The proposed architecture achieves sensitivity, accuracy, positive predictivity, and detection rate of 99.52, 99.43, 99.91, and 0.565%, respectively, in MATLAB, and 99.44, 98.88, 99.43, and 1.09%, respectively, in FPGA. In terms of both hardware utilization and R-peak detection rate achieved, the proposed architecture is suitable to use as a part of low-cost smart biomedical devices to perform continuous monitoring of ECG signals and automatic detection of heart rates.

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Keywords FPGA implementation · Electrocardiogram (ECG) · R-peak detection · Heart-rate · Lifting-based discrete wavelet transform

1 Introduction

In recent years, a spike in the number of sudden heart attacks and other cardiovascular diseases has drawn attention to the healthcare industry. Several smart biomedical devices that can automatically monitor heart rates, oxygen levels, and cardiac arrhythmias have been developed by the medical industry. But, most of the existing devices are very costly as they are imported from other countries. This demands an area-efficient, low-cost hardware architecture for automatic heart rate detection with high accuracy and low resource utilization. As a result, this research focuses on developing a hardware-efficient architectural design that can accurately detect R-peaks and calculate heart rate using the lifting-based discrete wavelet transform (DWT). A field-programmable gate array (FPGA) is a matrix of logic blocks that can be programmed based on the logic used. FPGA has a variety of applications in the real-time biomedical signal processing field because of its low power consumption, parallel processing, higher throughput, and flexible programming [21]. An electrocardiogram (ECG) is a biological test that can be used to monitor cardiac activity, calculate heart rates, and detect arrhythmias. The P-wave, QRS complex, and T-wave are three major components of the ECG signal. The QRS complex provides information about the amplitude and location (time) of an R-peak, and the R-R distance between two R-peaks is used to determine heart rate.

The most common R-peak detection algorithms implemented and evaluated on FPGA are Hilbert transform (HT) [21], Pan Tompkins (PT) [26], and wavelet transform [42]. HT is one of the popular R-peak detection approaches that require preprocessing steps like noise-removal, first-order differentiation, etc. [21]. The main disadvantage of the HT technique is that it requires a significant amount of hardware resources due to the multiple preprocessing steps. The QRS detection using the PT technique [26] involves complex signal processing operations and two types of thresholding techniques. Also, the Shannon energy envelope technique, which uses basic VHDL blocks for FPGA implementation, needs additional filtering and differentiation operations before R-peak detection in ECG signals [27]. Furthermore, the heart rate is calculated using a division block in [27], which is a fairly complex circuit for FPGA implementation. DWT is a popular digital signal processing technique used for extracting specific signal features, segregating signals into different time–frequency windows and classification of signals. It is widely used in a variety of applications like ECG signal processing, image processing [20], neural networks like spiking neural networks (SNN) models [36–38], etc. In [33, 43], the ECG signal is filtered using an integer Haar wavelet transform with a decomposition level of up to four. Since the Haar wavelet does not have any resemblance to an ECG wave, it will not be able to detect complex or irregular heart rhythms. Also, the proposed architectures in [33, 43] are not folded for different decomposition levels. For zero crossings and threshold selection, all four output coefficients are used in [33], thus increasing the number of factors for R-peak identification.

In this paper, a lifting-based DWT technique based on the Daubechies 4 wavelet is proposed to perform R-peak detection in ECG signals. An efficient and low-cost architecture for four-level Daubechies 4 lifting-based DWT is also proposed. The Daubechies 4 wavelet is chosen because it closely resembles an ECG beat, and it is always preferable to choose a wavelet that resembles the signal to be analyzed [10]. Lifting-based DWT is chosen over the conventional DWT approach for preprocessing ECG signals since it reduces computations of wavelet coefficients by a factor of two [19]. Without any additional preprocessing stage, the proposed DWT technique performs both noise-removal and preprocessing of the ECG signals. The proposed lifting-based Daubechies 4 architecture is compared with the existing ones in terms of the number of multipliers, adders, delay elements, and critical path delay and is found to utilize fewer adders and delay elements compared to others. The R-peak detection is carried out using only the fourth-level detailed wavelet coefficients. Heart rate is calculated from detected R-peaks without any division block to reduce the hardware. The complete architecture is evaluated using the MIT-BIH arrhythmia database (mitdb) [24], the MIT-BIH supraventricular arrhythmia database (svdb) [8], and the QT database (qtdb) [18].

The rest of the paper is organized as follows. A brief discussion on the lifting scheme and corresponding equations for implementing Daubechies 4 lifting-based DWT is included in Sect. 2. Section 3 illustrates the proposed methodology for R-peak detection and heart-rate computation, as well as the proposed architecture for Daubechies 4 lifting-based DWT. In Sect. 4, the performance of the proposed methodology on the MIT-BIH and the QT databases, synthesis report, and comparison with previous research work with respect to important design parameters are discussed. The proposed work is concluded in Sect. 5.

2 Theoretical Description of the Lifting Scheme

The wavelet transform provides a time–frequency representation of a signal [31]. It is appropriate for non-stationary signals like ECG, whose spectral components change over time. The DWT technique analyzes both low and high-frequency components by passing the signal through a bank of filters. The approximation coefficients (a_i) are obtained from the low-pass filter (LPF), and the detailed coefficients (d_i) are obtained from the high-pass filter (HPF) outputs after downsampling by a factor of two, where i denotes the number of decomposition levels [22]. The output signal from each filter is passed through a downsampler, which re-samples the signal at half of the input sampling rate by eliminating every alternate sample. Figure 1 shows a conventional DWT architecture describing two levels of decomposition. The conventional DWT architecture is inefficient because half of the output coefficients obtained after filtering are discarded due to downsampling, after the filtering step. The performance of the DWT architecture is improved by employing a polyphase matrix of the filter bank that avoids the calculation of wavelet coefficients, which are to be discarded later, by performing the downsampling before filtering. In the polyphase representation, the filter and the input signal are split into even and odd halves.

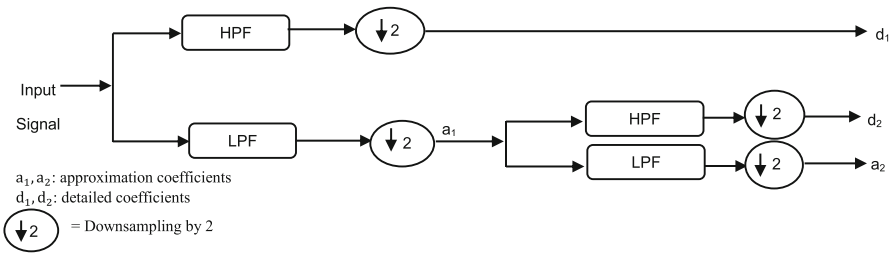

Fig. 1 A conventional DWT architecture describing two levels of decomposition

If y_n is the input signal and y_n^e and y_n^o are the respective even and odd parts of the input signal, a_n and d_n are the approximation and detailed coefficients, respectively, and $l(z)$ and $h(z)$ are the transfer functions of LPF and HPF, respectively, then the polyphase representation of the wavelet decomposition can be expressed as

$$\begin{bmatrix} d_n \\ a_n \end{bmatrix} = F(z) \begin{bmatrix} y_n^o \\ y_n^e \end{bmatrix} \tag{1}$$

where $F(z)$ is the polyphase filter bank, which is expressed as:

$$F(z) = \begin{bmatrix} l_e(z) & h_e(z) \\ l_o(z) & h_o(z) \end{bmatrix} \tag{2}$$

$h_e(z)$ and $h_o(z)$ are the respective even and odd components of the transfer functions of the HPFs, and $l_e(z)$ and $l_o(z)$ are the respective even and odd components of the transfer functions of the LPFs.

The lifting scheme proposed by Sweldon [32] calculates the DWT coefficients more efficiently than the conventional approach because it reduces the computational complexity by factorizing the polyphase matrix of the wavelet filter bank into elementary matrices using the Euclidean algorithm. Every FIR filterbank can be factored into a cascade of lifting steps, i.e., as the product of upper and lower triangular matrices and a diagonal normalization matrix. Using the Euclidean algorithm, the polyphase matrix $F(z)$ can be factored into lifting steps as follows [1]:

$$F(z) = \prod_{t=1}^{m} \begin{bmatrix} 1 & p_t(z) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ u_t(z) & 1 \end{bmatrix} \begin{bmatrix} N & 0 \\ 0 & \frac{1}{N} \end{bmatrix} \tag{3}$$

where $p_t(z)$ and $u_t(z)$ are the predict and update Laurent polynomials, respectively, t is the number of predict and update polynomials, and N is the normalization factor. The architecture for the lifting scheme is shown in Fig. 2. The LPF, $l(z)$, and HPF, $h(z)$, associated with Daubechies 4 wavelet are given by [12]:

$$l(z) = l_0 + l_1 z^{-1} + l_2 z^{-2} + l_3 z^{-3} \tag{4}$$

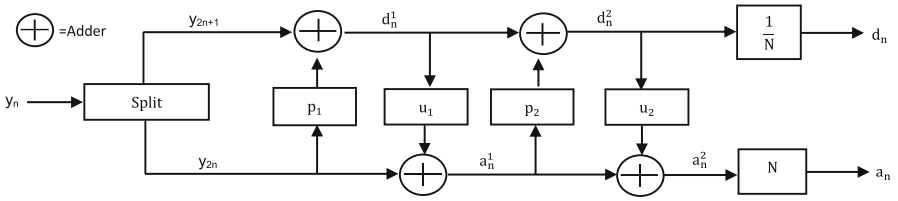

Fig. 2 The architecture of the lifting scheme

$$h(z) = -l_3 z^2 + l_2 z^1 - l_1 + l_0 z^{-1} \tag{5}$$

where $l_0 = \frac{1+\sqrt{3}}{4\sqrt{2}}$, $l_1 = \frac{3+\sqrt{3}}{4\sqrt{2}}$, $l_2 = \frac{3-\sqrt{3}}{4\sqrt{2}}$, and $l_3 = \frac{1-\sqrt{3}}{4\sqrt{2}}$ are the filter coefficients. On splitting the filters into even and odd parts, the corresponding polyphase matrix for the Daubechies 4 wavelet is given as [7]:

$$F(z) = \begin{bmatrix} l_0 + l_2 z^{-1} & -l_3 z^1 - l_1 \\ l_1 + l_3 z^{-1} & l_2 z^1 + l_0 \end{bmatrix} \tag{6}$$

The polyphase matrix for the Daubechies 4 wavelet filter factored into lifting steps using the Euclidean algorithm can be expressed as follows:

$$F(z) = \begin{bmatrix} 1 & -\sqrt{3} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ \frac{\sqrt{3}}{4} + \frac{\sqrt{3}-2}{4} z^{-1} & 1 \end{bmatrix} \begin{bmatrix} 1 & z \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \frac{\sqrt{3}+1}{\sqrt{2}} & 0 \\ 0 & \frac{\sqrt{3}-1}{\sqrt{2}} \end{bmatrix} \tag{7}$$

On substituting the factorized polyphase matrix, $F(z)$ into Eq. (1), we get the corresponding equations for the implementation of the lifting-based DWT based on the Daubechies 4 wavelet:

$$d_n^1 = y_{2n+1} - \sqrt{3} y_{2n} \tag{8}$$

$$a_n^1 = y_{2n} + \sqrt{3}/4 d_n^1 + \frac{\sqrt{3}-2}{4} d_{n+1}^1 \tag{9}$$

$$d_n^2 = d_n^1 + a_{n-1}^1 \tag{10}$$

$$a_n = \frac{\sqrt{3}+1}{\sqrt{2}} a_n^1 \tag{11}$$

$$d_n = \frac{\sqrt{3}-1}{\sqrt{2}} d_n^2 \tag{12}$$

where d_n^1, a_n^1 and d_n^2 are the intermediate values, y_n is the input signal with y_{2n} and y_{2n+1} as the even and odd parts of the signal, and n is the length of the input signal.

3 Proposed Methodology for R-Peak Detection and Heart-Rate Calculation of ECG Signals

A complete block diagram describing R-peak detection and heart-rate calculation of the ECG signals using the lifting-based DWT implemented in an FPGA is shown in Fig. 3. A detailed description of each block is presented next.

3.1 Pre-processing of ECG Signal Using Lifting-based DWT

DWT divides the input signal into different time–frequency windows depending on the number of decomposition levels. The energy of abnormal and normal QRS complexes in an ECG signal is concentrated within a frequency range of 5–22 Hz [45]. So the number of decomposition levels for the proposed lifting-based DWT is set to four for a sampling frequency of 360 Hz. Among the output coefficients produced after the lifting-based DWT, only fourth-level detailed coefficients, with a frequency range of 11.25–22.25 Hz, are used for the detection of QRS complexes and R-peaks. Additionally, the frequency range of the chosen DWT coefficient helps in noise removal without any extra filtering operation because the most prominent noises in ECG recordings are baseline wander and electrode motion noise with a frequency range below 10 Hz [9].

3.1.1 Proposed Architecture of Lifting-based DWT for Daubechies 4 Wavelet

A block diagram describing the proposed four-level Daubechies 4 lifting-based DWT architecture is shown in Fig. 4. In Fig. 4, the first block describes the lifting-based

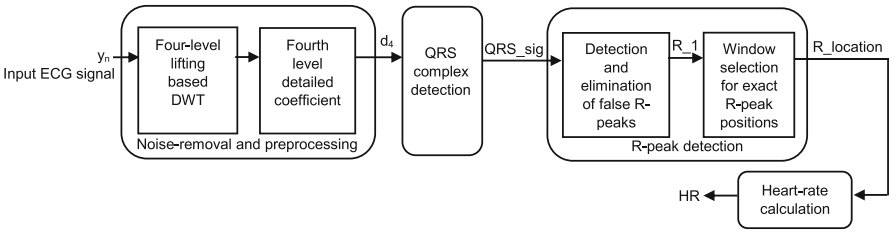

Fig. 3 Block diagram describing the proposed methodology for R-peak detection and heart-rate calculation

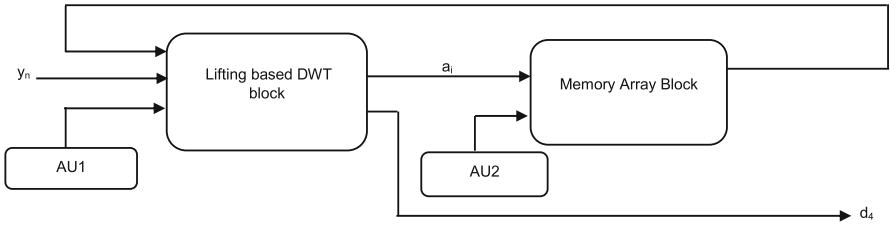

Fig. 4 Block diagram describing the proposed architecture for four-level Daubechies 4 lifting-based DWT

DWT technique that produces the approximation coefficients, a_i's, ($i = 1$ to 4), and the detailed coefficient for the fourth level, d_4. To reduce computation, the detailed coefficients of the first three levels are not calculated. After each decomposition level, the approximation coefficients are stored in a memory array of size N/2 × 16, where N is the total sample size of the input ECG signal and 16 represents the input bit-size, which is used as an input for the next decomposition level. The proposed lifting-based DWT architecture is folded after the first decomposition level. So, all four levels of decompositions are performed using a single lifting-based DWT block. The address unit AU1 is used to perform each level of decomposition, and AU2 is used to provide the address required to store the wavelet coefficients in the memory block, respectively.

A signal flow graph depicting the computation of wavelet coefficients using Eqs. (8–12) is shown in Fig. 5. The approximation and detailed coefficients are indicated as a_n and d_n, respectively. As illustrated in the signal flow graph, the first step is involved in the calculation of the intermediate step d_n^1. The second step performs the calculation of two intermediate values a_n^1 and d_n^2 simultaneously, and at the final step, the scaling of the intermediate values gives the approximation coefficients, a_n, and the detailed coefficients, d_n. So, the five equations required to construct the lifting-based DWT for the Daubechies 4 wavelet are reduced to only three steps in the proposed architecture. Figure 6 shows the equivalent architecture of the proposed lifting-based

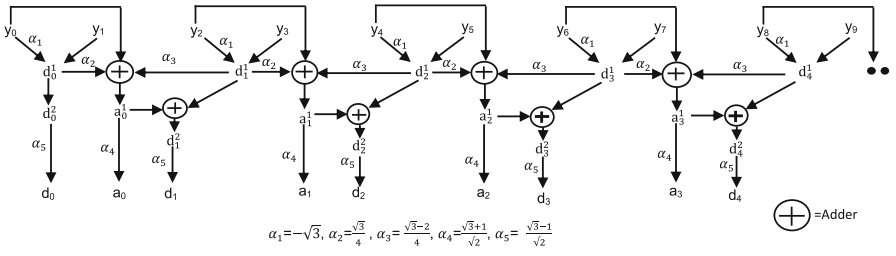

Fig. 5 Signal flow graph of the lifting-based DWT block based on Daubechies 4 wavelet

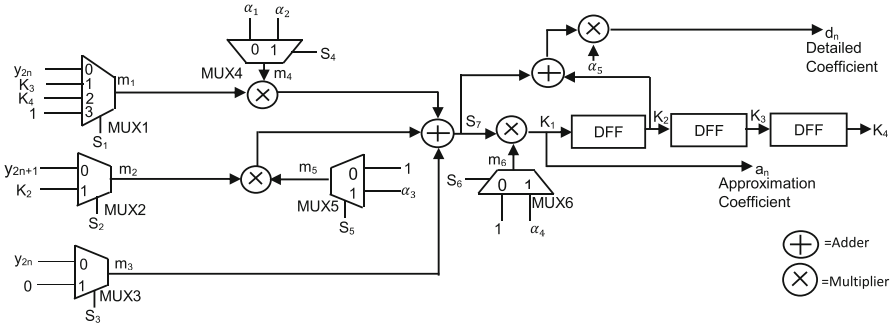

Fig. 6 Proposed lifting-based DWT block for Daubechies 4 wavelet, where m_1, m_2…, m_6 are the output from the multiplexers with select lines S_1, S_2,.., S_6, respectively, K_2, K_3, and K_4 are the output from the D flip-flops

DWT block using the signal flow graph. Table 1 explains the step-by-step operation of the proposed architecture for the calculation of the DWT coefficients. As shown in Table 1, a_n and d_n are produced in parallel at K_1 and d, respectively, at alternating clock pulses. Also, the select line S_k ($k = 1$ to 6) values repeat alternately after the third clock pulse. The obtained approximation coefficients are stored in the memory array to start the next level of decomposition.

3.1.2 Address Units

Each address unit consists of a 4:2 encoder, a 4:1 multiplexer, and an 11-bit loadable counter, as shown in Fig. 7. The proposed architecture consists of two address units, AU1 and AU2. In AU1, the encoder has four input signals, START_j ($j = 0$ to 3) which enable four different levels of decomposition. Initially, the START_0 signal is enabled. Depending on the START_j signal enabled, the multiplexer's output provides a load value (LOAD) to the loadable counter. After the loadable counter completes counting, it enables the next START_j and disables the previous START_{j-1} signal for performing the next level of decomposition. The inputs to the multiplexer are the varying sample values required for performing signal decomposition due to the subsampling in DWT. The AU1's output ADDRESS serves two major purposes. First, it divides the incoming input samples into y_{2n} and y_{2n+1}. The input signal is divided into even and odd parts by dividing the incoming sample value by two: y_{2n} represents the samples that are multiples of two, and the remaining are represented by y_{2n+1}. Second, if the ADDRESS value is odd, S_2, S_4, and S_5 get the value 0, and S_3 and S_6 get the value 1, and vice versa when the ADDRESS value is even. A similar architecture for AU2 is used for storing the approximation coefficient values in the memory array, which are used as inputs for the next level of decomposition.

All the blocks or elements used for the proposed four-level Daubechies 4 lifting-based DWT architecture are utilized at every clock pulse, which makes the architecture hardware-efficient. In [2], an area-efficient three-level lifting-based DWT architecture for bio-orthogonal wavelets [3] is proposed that produces the output wavelet coefficients serially and has a high critical path delay of two adders and one multiplier. The architecture in [2] employs seven multiplexers whose select line values are not repetitive and hence will require separate memory elements for storage. On the other hand, the select line values for the multiplexers used are repetitive in the proposed architecture and hence do not require any extra memory storage. In addition, a new pipelined architecture is proposed in Fig. 8, where pipelining registers, R, have been inserted to reduce the critical path delay of the proposed architecture in Fig. 6. The proposed pipelined architecture now has a critical path delay of one multiplier only and can operate at a higher frequency.

A comparison table of existing lifting-based and conventional DWT architectures with that of the proposed lifting-based pipelined architecture is shown in Table 2. The recursive lifting-based DWT architecture in [12] has a high critical path delay with four adders and a multiplier. Also, the number of registers and delay elements depends on the number of decomposition levels. The architecture of [13] is based on the algebraic integer quantization (AIQ) mapping of wavelet coefficients, which requires separate hardware for mapping and reconstruction. A folded lifting-based DWT proposed in

Table 1 Operation of the proposed lifting-based DWT architecture based on Daubechies 4 wavelet

CLK	S_1	S_2	S_3	S_4	S_5	S_6	m_1	m_2	m_3	m_4	m_5	m_6	S_7	K_1	K_2	K_3	K_4	d
0	0	0	1	0	0	1	y_0	y_1	0	α_1	1	1	d_0^1	d_0^1	×	×	×	d_0
1	0	0	1	0	0	1	y_2	y_3	0	α_1	1	1	d_1^1	d_1^1	d_0^1	×	×	–
2	1	1	0	1	1	0	d_0^1	d_1^1	y_0	α_2	α_3	α_4	a_0^1	a_0	d_1^1	d_0^1	×	d_1
3	0	0	1	0	0	1	y_4	y_5	0	α_1	1	1	d_2^1	d_2^1	a_0	d_1^1	d_0^1	–
4	2	1	0	1	1	0	d_1^1	d_2^1	y_2	α_2	α_3	α_4	a_1^1	a_1	d_2^1	a_0	d_1^1	d_2
5	0	0	1	0	0	1	y_6	y_7	0	α_1	1	1	d_3^1	d_3^1	a_1	d_2^1	a_0	–
6	2	1	0	1	1	0	d_2^1	d_3^1	y_4	α_2	α_3	α_4	a_2^1	a_2	d_3^1	a_1	d_2^1	d_3
7	0	0	1	0	0	1	y_8	y_9	0	α_1	1	1	d_4^1	d_4^1	a_2	d_3^1	a_1	–

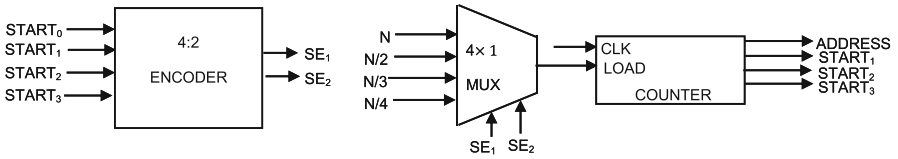

Fig. 7 Address unit of proposed lifting-based DWT based on Daubechies 4 wavelet

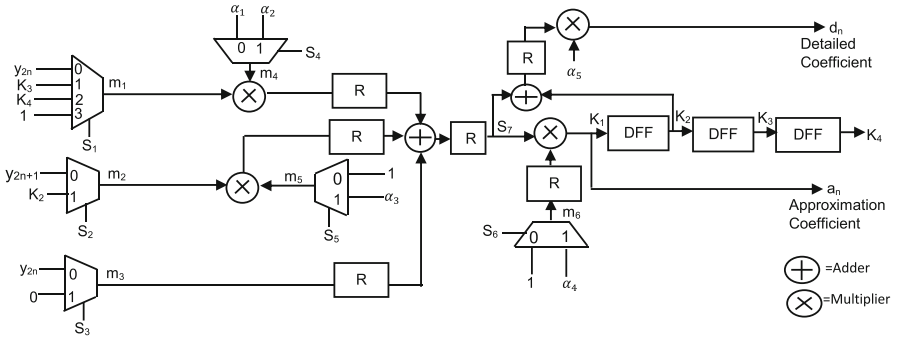

Fig. 8 Proposed pipelined lifting-based DWT block based on Daubechies 4 wavelet

Table 2 Comparison of existing lifting-based and conventional DWT architectures

Methodology	Type of wavelet	Critical path	Number of adders	Number of multipliers	Number of delay elements	Multiplexer	Th
Recursive architecture [12]	Daub4	$4(T_a + T_m)$	4	6	i	–	2
Folded AIQ mapping [13]	Daub4	$3T_a$	9	0	8	–	1
Folded architecture [34]	Daub4	$T_a + T_m$	4	5	2^{i+1}	–	2
Modified lifting-based [28]	9/7	T_m	4	8	21	–	2
Multiplier-less [30]	5/3	$2T_{a+}$Right Shift + 2's compliment	6	6 (Shifter)	6	–	2
Distributed Arithmetic [5]	9/7, 5/3	T_a	18	0	12	32	2
Proposed	Daub4	T_m	2	4	3	3	2

Ta and Tm are critical path delay of adder and multiplier, respectively, Th is the throughput, Daub4 = Daubechies 4 wavelet, and i is the number of decomposition levels

[34] has delay elements that depend on the number of decomposition stages used. A modified lifting-based DWT architecture based on the 9/7 filter [28] and a multiplier-less lifting-based DWT architecture based on the 5/3 filter [30] have also been studied and compared with the proposed one. The distributed arithmetic architecture in [5] employs both 9/7 and 5/3 wavelets and is based on the conventional DWT approach. Table 2 shows that the proposed architecture has the lowest number of arithmetic units, multiplexers, and delay elements that are independent of the number of decomposition levels. Apart from the conventional DWT architecture in [5], which has a large number of adders, multiplexers, and delay elements, the proposed architecture has the shortest critical path delay. Since the proposed lifting-based DWT architecture has low resource utilization, it can be used for optimized image processing [20], SNN [36–38], and other neuromorphic computing architectural designs [35, 39, 40] as well. In [37], the credit assignment problem in neuromorphic computing is solved by segregating signals into dendritic compartments where the proposed lifting-based architecture can be an effective signal segregation technique. A self-adaptive multi-compartment (SAM) spiking neuron model for spike-based learning with working memory is proposed in [36], and a real-time hardware-efficient scalable architecture for the implementation of large-scale multi-compartment biologically meaningful neural networks is proposed in [35]. The proposed DWT technique can be utilized to classify noisy spike patterns in [36] by extracting required features. A spike-based framework with minimum error entropy is proposed in [38] for building an online meta-learning scheme in SNN architectures, and a fault-tolerant neuromorphic spike routing system to avoid multiple fault nodes is proposed in [39]. A large-scale cerebellar design is proposed in [40] to encompass the cerebellum's anatomical structure in a large-scale SNN model. The proposed wavelet transform technique can be used for visualizing errors in various layers of an SNN model to develop more accurate error estimation [38] and fault-tolerant systems [39], as well as to reduce the overall cost of complete SNN systems due to its low resource utilization.

3.2 QRS Detection Block

The QRS detection block detects the QRS complexes once preprocessing of the ECG signal using the lifting-based DWT technique is completed. Because the frequency of d_4 is similar to that of a QRS complex, only one thresholding step is used to eliminate any remaining P, T-wave peaks, or unwanted large noise peaks. Then, QRS complexes are detected using an adaptive threshold of 0.18ε, where ε is the absolute highest amplitude value in the fourth level of detailed coefficients. The values of d_4 above the adaptive threshold are considered potential QRS complexes and are referred to as QRS_sig.

3.3 R-Peak Detection and Heart-Rate Calculations

The QRS_sig is passed through the R-peak detection blocks to detect the R-peak within each detected QRS complex. The R-peak detection starts with sample value zero and finds the maximum amplitude of the QRS_sig within each QRS complex until the next

zeroth sample is found. This step avoids the detection of more than one R-peak within a QRS complex which may occur because of notched R-peaks. Once all the R-peaks are detected, the false ones are eliminated based on the following conditions: (a) If R_xR_{x+1} (x denotes the R-peak position) interval is less than 200 ms, the R_{x+1} peak is eliminated as QRS complexes cannot occur more closely than this refractory period; (b) If R_xR_{x+1} interval is less than 360 ms, it is most certainly a T-wave and so the R peak with the lower amplitude is removed and the next RR interval is verified.

After the elimination process, the detected R-peaks are named R_1. But, the detected R-peaks are different from the real R-peaks in the input ECG signal because of an offset [6]. The true R-peaks are detected from the input signal by finding the maximum value over a window length of 60 samples around the detected R_1 peaks. The maximum length of the QRS complex for any patient is 160 ms, which is around 60 samples at a sampling frequency of 360 Hz [15]. This last step helps in the accurate detection of the R-peak positions in the ECG signal. Heart rate is then computed using shift and compare operations instead of any division block to reduce hardware complexities.

4 Results and Discussion

4.1 Performance Analysis

The entire R-peak detection architecture is implemented on the Artix-7 FPGA evaluation board. The target chip for the selected FPGA kit is XC7A200TFBG676-2. In the VIVADO XILINX 2017.4 tool, the architecture is implemented on the FPGA using the Verilog hardware description language. The proposed architecture is first evaluated in MATLAB R2020a using the mitdb and then implemented on the FPGA evaluation board using the mitdb [24], svdb [8], and the qtdb [18]. The MATLAB code for the proposed R-peak detection technique using lifting-based DWT is made available on Github, and the link to access the same is provided in the Declarations section of the paper. The ECG signal is converted into a 16-bit fixed-point representation with 12 fractional bits in MATLAB and stored in a text file. In XILINX, a ROM block is initialized using a text file. The address for the ROM block is generated using AU1. In FPGA, a total of 3000 samples at a sampling frequency of 360 Hz are used for the input ECG signal. The proposed R-peak detection technique is tested on three different databases, the mitdb, the svdb, and the qtdb, to verify its effectiveness. With a sampling frequency of 360 Hz, the mitdb contains 48 half-hours of two-channel ECG recordings from 47 different subjects. All of the 48 ECG recordings were tested for a period of 3000 samples in FPGA and a period of 21,600 samples in MATLAB. The svdb, with a sampling frequency of 128 Hz, contains 78 half-hour ECG recordings, and the qtdb contains 100 fifteen-minute ECG recordings. A total of 42 and 32 distinct ECG data were tested from the svdb and the qtdb, respectively, for a period of 3000 samples on the FPGA board. Out of a total of 650,000 samples in each ECG recording, the samples that are either affected by noise or contain abnormal ECG beats are chosen for evaluation. The svdb is chosen for testing the proposed architecture as supraventricular contractions are one of the most prevalent arrhythmias among people with cardiac diseases. The performance of the proposed technique is evaluated

using three parameters, namely true positive (TP), false positive (FP), and false negative (FN), which calculate the total number of correctly identified R-peaks, falsely detected R-peaks, and missed R-peaks, respectively. The sensitivity (SEN), detection rate (DER), accuracy (ACC), and positive predictive value (PPV) can be calculated using the above three parameters:

$$\mathrm{SEN} = \frac{\mathrm{TP}}{\mathrm{TP} + \mathrm{FN}} \times 100\% \tag{13}$$

$$\mathrm{DER} = \frac{\mathrm{FN} + \mathrm{FP}}{\mathrm{TP}} \times 100\% \tag{14}$$

$$\mathrm{ACC} = \frac{\mathrm{TP}}{\mathrm{TP} + \mathrm{FN} + \mathrm{FP}} \times 100\% \tag{15}$$

$$\mathrm{PPV} = \frac{\mathrm{TP}}{\mathrm{TP} + \mathrm{FP}} \times 100\% \tag{16}$$

Table 3 shows the performance of the proposed lifting-based DWT technique in MATLAB using the mitdb. Table 4 shows the performance of the proposed technique when implemented on an FPGA utilizing the mitdb, svdb, and qtdb. A total of 122 distinct ECG data sets were tested on FPGA. As seen from the results, the detection rates for FPGA implementation and MATLAB are close enough with a slight variance due to the difference in the number of samples used for testing. Figure 9 depicts R-peaks detected in XILINX for record numbers 107, 207, 223, 111, and 203 of the mitdb. According to the XILINX results, the input ECG signals, the detected QRS complexes, the initial R-peaks detected, and the final R-peak locations detected are stored in the array named rom, QRS, R_1, and R_location, respectively. Because of the presence of noise, the inverted R-peaks of 207 result in the detection of a false peak at a sample value of 535. But on the other hand, the proposed technique accurately detects abnormal R-peaks in 107, R-peaks with varying amplitude in 223, notched R-peaks with large T-waves in 111, and abnormal R-peaks with baseline wander in 203 without any false detection. In [26], all of the R-peaks detected for 107 are slightly shifted from the actual ones, but the proposed technique detects R-peaks at their exact locations as shown in Fig. 9b. As seen from the results, the evaluated R-peak values and the actual R-peak values are mostly the same or have very little variation. As a result, the R-peak detection error of the proposed technique is negligible.

4.2 Synthesis Report and Performance Comparison

The synthesis report obtained for the proposed technique implemented using the Artix-7 evaluation board is shown in Table 5. The proposed pipelined architecture achieves a maximum operating frequency of 44 MHz. The comparison of the proposed lifting-based R-peak detection technique with the existing software implemented R-peak detection techniques in terms of SEN%, ACC%, DER%, and PPV% is shown in Table 6. The proposed methodology has the highest PPV% value, because of a relatively lower number of FP detected, and a better detection rate than that of [23]. Even though

Table 3 Performance of the MATLAB implementation of proposed lifting-based R-peak detection technique using mitdb

ECG record number	Total beats	TP	FN	FP	SEN%	DER%	ACC%	PPV%
100	74	74	0	0	100	0	100	100
101	70	70	0	0	100	0	100	100
102	73	73	0	0	100	0	100	100
103	70	70	0	0	100	0	100	100
104	74	74	0	0	100	0	100	100
105	83	83	0	0	100	0	100	100
106	69	66	3	0	95.65	4.54	95.65	100
107	71	71	0	0	100	0	100	100
108	58	60	0	2	100	3.33	96.77	96.77
109	91	91	0	0	100	0	100	100
111	69	69	0	0	100	0	100	100
112	85	85	0	0	100	0	100	100
113	58	58	0	0	100	0	100	100
114	55	54	1	0	98.18	1.85	98.18	100
115	63	63	0	0	100	0	100	100
116	79	79	0	0	100	0	100	100
117	50	50	0	0	100	0	100	100
118	73	73	0	0	100	0	100	100
119	65	65	0	0	100	0	100	100
121	60	59	1	0	98.33	1.69	98.33	100
122	87	86	1	0	98.85	1.16	98.85	100
123	49	49	0	0	100	0	100	100
124	50	49	1	0	98	2.04	98	100
200	86	86	0	0	100	0	100	100
202	53	53	0	0	100	0	100	100
203	86	86	0	0	100	0	100	100
205	89	89	0	0	100	0	100	100
207	61	61	0	0	100	0	100	100
208	105	105	0	0	100	0	100	100
209	92	92	0	0	100	0	100	100
210	91	91	0	0	100	0	100	100
212	90	90	0	0	100	0	100	100
213	111	111	0	0	100	0	100	100
214	76	76	0	0	100	0	100	100
215	113	111	2	0	98.23	1.80	98.23	100

Table 3 (continued)

ECG record number	Total beats	TP	FN	FP	SEN%	DER%	ACC%	PPV%
217	72	73	0	1	100	1.37	98.64	98.64
219	74	74	0	0	100	0	100	100
220	72	72	0	0	100	0	100	100
221	79	78	1	0	98.73	1.28	98.73	100
222	75	75	0	0	100	0	100	100
223	80	80	0	0	100	0	100	100
228	71	71	0	0	100	0	100	100
230	79	79	0	0	100	0	100	100
231	63	63	0	0	100	0	100	100
232	63	63	0	0	100	0	100	100
233	103	96	7	0	93.20	7.29	93.20	100
234	92	92	0	0	100	0	100	100
Total	3552	3538	17	3	99.52	0.565	99.43	99.91

Table 4 Performance of the FPGA implementation of the proposed lifting-based R-peak detection technique using mitdb, svdb, and qtdb

Databases	TP	FN	FP	SEN (%)	DER (%)	ACC (%)	PPV (%)
mitdb	1130	6	9	99.47	1.327	98.68	99.20
svdb	631	4	4	99.37	1.267	98.74	99.37
qtdb	393	2	1	99.49	0.7	99.24	99.74
Total	2154	12	14	99.44	1.09	98.88	99.43

the method proposed in [16] has a higher SEN% than the proposed method, in [16], the evaluation has not been performed on all the 48 records from mitdb. In Table 7, the FPGA-based performance of the proposed methodology is compared with that of the existing hardware-based R-peak detection methodologies. The proposed technique has the highest SEN% of any except [23]. The comparison of the existing FPGA-based R-peak detection techniques in terms of resource utilization is tabulated in Table 8. In terms of resource utilization, the proposed architecture uses the lowest number of registers, flip-flops, and LUTs except [14, 33]. The low resource utilization of [14, 33] comes at the expense of very low detection rates. The high detection rate of [23, 27] comes at the expense of higher resource utilization. In terms of the detection rates achieved, the proposed architectural design results in the lowest resource utilization with respect to wavelet transform and other commonly used R-peak detection techniques.

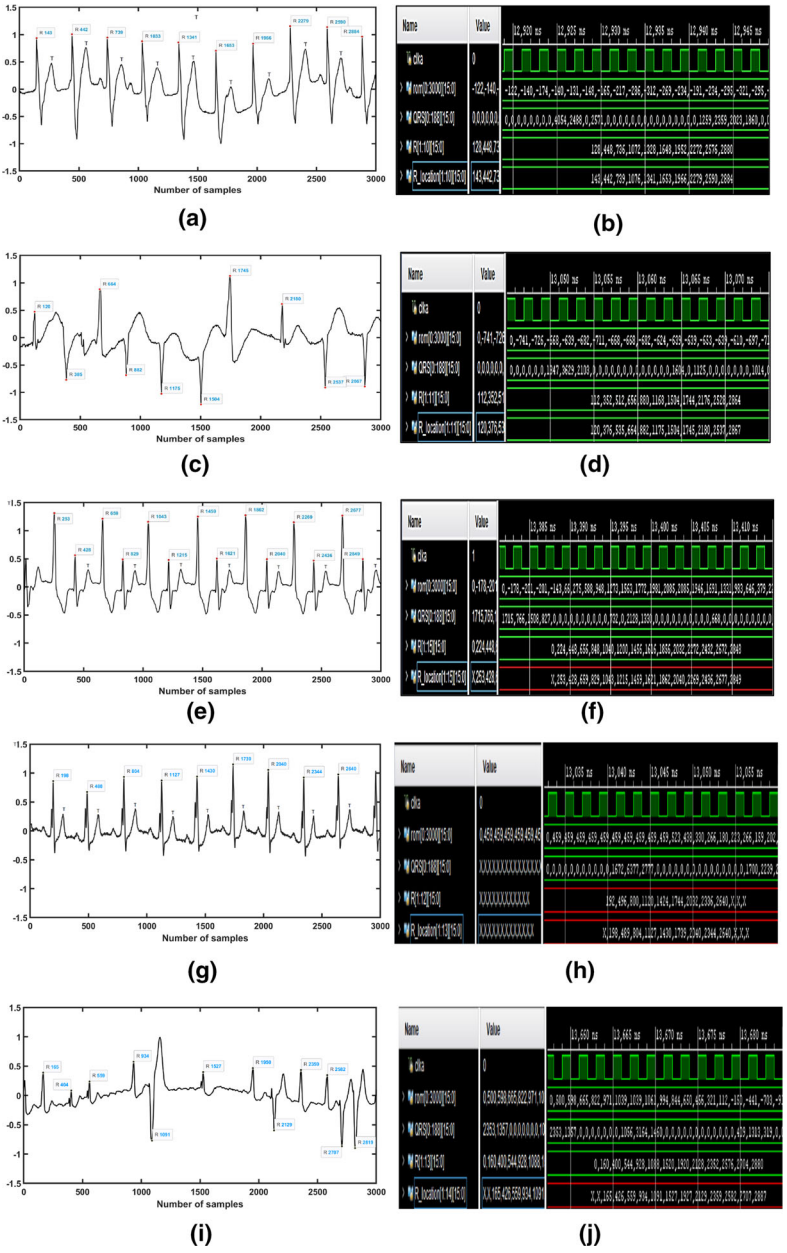

Fig. 9 **a** Actual R-peaks in record number 107 from mitdb, **b** R-peak detected (R_location) in XILINX for record number 107 with an average heart-rate of 70.9, **c** Actual R-peaks in record number 207 from mitdb, and **d** R-peak detected (R_location) in XILINX for record number 207 with an average heart-rate of 78.6 **e** Actual R-peaks in record number 223 from mitdb, **f** R-peak detected (R_location) in XILINX for record number 223 with an average heart-rate of 105, **g** Actual R-peaks in record number 111 from mitdb, and **h** R-peak detected (R_location) in XILINX for record number 111 with an average heart-rate of 70 **i** Actual R-peaks in record number 203 from mitdb, **j** R-peak detected (R_location) in XILINX for record number 203 with an average heart-rate of 40

Table 5 Synthesis report of the proposed R-peak detection and heart-rate calculation architecture in Artix-7 FPGA board

Resource Utilization	Used	Available	Utilization (%)
Slice LUTs	2197	134,600	1.63
Slice Registers	585	269,200	0.22
Register as Flip-Flop	486	269,200	0.18
BRAM	2	365	0.55
Bonded IOBs	150	400	37.5
BUFGCTRL	4	32	12.5
Maximum operating frequency	44 MHz		

Table 6 Comparison of existing software-based (MATLAB) R-peak detection techniques with the proposed one in terms of detection rates

Methodology	Database used	SEN (%)	ACC (%)	DER (%)	PPV (%)
Shanon energy envelope [27]	mitdb	99.95	99.84	0.16	99.89
Bio-orthogonal wavelet transform [16]	mitdb	99.86	99.86	0.002	–
Center derivative and intermediate value theorem [23]	mitdb	99.58	99.26	0.74	99.68
Proposed	mitdb	99.52	99.43	0.565	99.91

5 Conclusions

An FPGA-based low-cost R-peak and heart rate detection architecture using the lifting-based DWT is proposed in this research paper. The majority of the existing methodologies used for the R-peak detection require pre-filtering or other signal processing operations. Whereas signal decomposition using lifting-based DWT performs both noise-removal and preprocessing of ECG signals without any additional preprocessing steps. In comparison to existing lifting-based DWT architectures for Daubechies 4 wavelet, the proposed architecture requires fewer adders and delay elements. The proposed architecture's critical path delay is also comparable to the existing architectures. The R-peaks detected using the proposed technique show negligible error with respect to the actual R-peaks of the input signals. Both MATLAB and FPGA-based evaluations using mitdb, svdb, and qtdb were performed for the proposed architecture. The proposed architecture achieves a sensitivity of 99.52% and 99.44%, an accuracy of 99.43% and 98.88%, a detection rate of 0.56% and 1.09%, and a positive predictive value of 99.91% and 99.43% in the case of MATLAB and FPGA-based implementations, respectively. With the proposed Daubechies 4 lifting-based DWT architecture, the R-peak detection technique achieves a good detection rate while using a minimum number of resources.

Table 7 Comparison of existing hardware-implemented R-peak detection techniques with the proposed one in terms of detection rates

Methodology	Database Used	SEN (%)	ACC (%)	DER (%)
PT [26]	mitdb	99.48	99.31	0.68
Integer Haar wavelet transform [33]	Self-acquired	98.76	–	–
Integer Haar wavelet transform [43]	Self-acquired data	98.31	98.15	1.88
Center derivative and intermediate value theorem [23]	mitdb	99.83	99.39	0.61
DWT and multilayer perception (MLP) [41]	mitdb	98.3	95.0	1.7
Empirical mode decomposition [29]	nsrdb + svdb + afdb	94.76	–	–
Biorthogonal spline wavelet transform [4]	mitdb	99.31	98.5	1.49
Filtering, contrast enhancement, detection block [11]	mitdb	98.82	–	–
Kalman filter [44]	mitdb	99.23	98.63	–
Biorthogonal wavelet transform [17]	mitdb	99.31	98.9	1.02
Energy derivative [25]	mitdb	99.2	98.5	1.46
Integer Haar wavelet transform [14]	qtdb	98.12	–	–
Proposed	mitdb + svdb + qtdb	99.44	98.88	1.09

nsrdb = normal sinus rhythm database, afdb = atrial fibrillation database

Table 8 Comparison of resource utilization of the existing FPGA-based R-peak detection techniques with the proposed technique

Methodology	Registers	Flip-flops	LUTs
PT [26]	1061	–	4900
Shanon energy envelope [27]	5728	–	88,456
Integer Haar wavelet transform [33]	–	501	557
Center derivative and intermediate value theorem [23]	3587	31,577	31,577
DWT and multilayer perception (MLP) [41]	2650	2763	7598
Biorthogonal spline wavelet transform [4]	1320	1298	2102
Kalman filter [44]	4421	–	21,111
Integer Haar wavelet transform [14]	503	–	2004
Proposed	584	486	2197

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Data Availability The ECG records are available online at Physionet ATM: (https://archive.physionet.org/cgi-bin/atm/ATM).

Code Availability https://github.com/anushkagon11/MATLAB_Code_for_ECG_R_Peak_Detection.git

Declarations

Conflict of interest The authors declare that there is no conflict of interest.

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