In this project, you are to design a fully-differential single-stage operational transconductance amplifier (OTA) to be used in the front-end of an 8-bit pipelined A/D converter. The conceptual diagram of the amplifier and its utilization as a switched-capacitor (SC) sample and hold circuit is shown in Fig. 1 where ϕ_1 and ϕ_2 are two non-overlapping clock phases and ϕ_{1a} is the advanced version of ϕ_1 only in its falling edge. The amplifier structure is shown in Fig. 2, and the common-mode feedback and bias circuits are illustrated in Figs. 3 and 4, respectively. The design specifications of the SC sample and hold amplifier are summarized as follows:

- Open-loop DC gain ≥ 50 dB
- Output voltage swing ≥ 1.0 $V_{pp,\,diff}$ with total harmonic distortion (THD) ≤ −45 dB, sampling frequency of 40 MHz, 1.298828125 MHz sinusoidal input, and 4096 FFT points
- Settling time with 0.2% settling error ≤ 10 ns
- Power supply voltage: 1.2 V
- S/H and load capacitors: C_H = 1 pF, C_L = 1 pF

The key design objective is minimizing the power dissipation while meeting all design requirements. The circuit is to be simulated in HSPICE using 90 nm TSMC CMOS technology. You can use ideal switches in both switched-capacitor S/H and CMFB circuits to realize the switches controlled by different clock phases, but as a ***bonus*** you may also use actual MOS devices for the switches. Note, in AC simulations you are to use an ideal CMFB circuit. Moreover, as a ***bonus***, you may check the circuit performance at different process corner cases including slow, nominal, and fast models for both nMOS and pMOS devices as well as temperature variations spanning from –40°C to 85°C. In overall, as a bonus, you are to report all the simulated results in a table at least in three different cases: TT @ 27°C, SS @ 85°C, and FF @ –40°C.

Document your results in a ***written report***. It should be ***concise*** summary of your work and should highlight the most important features of the design. Explain clearly how you designed the circuits and ***demonstrate convincingly*** how your design meets all requirements. You may add appendices to expand upon significant aspects of the design, or provide supporting calculations and simulation results. Treat the appendices as references within the main text of the report. You can also do this project in a team work up to two persons and present a single report.

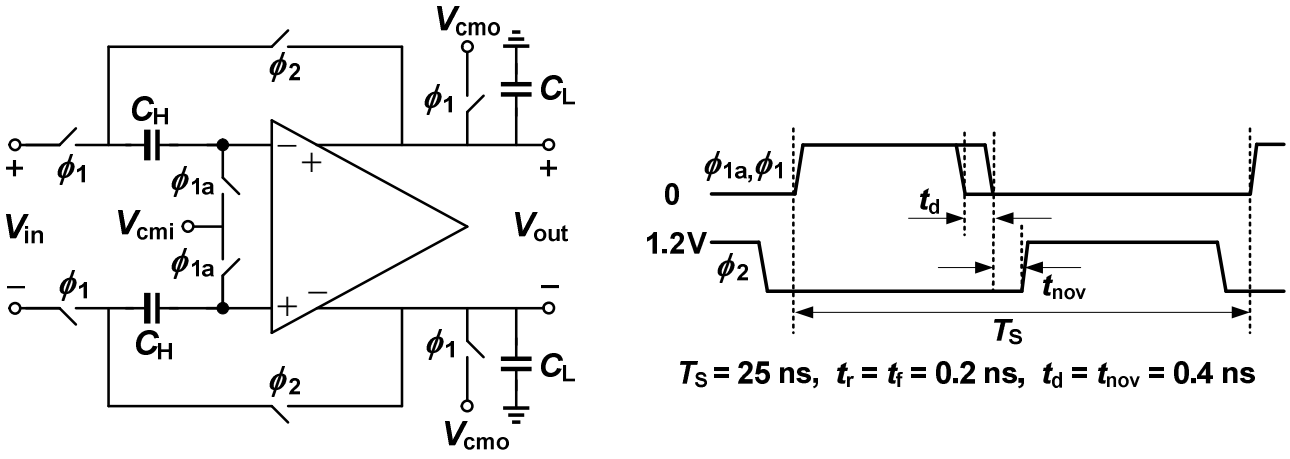

Fig. 1: A switched-capacitor sample and hold circuit.

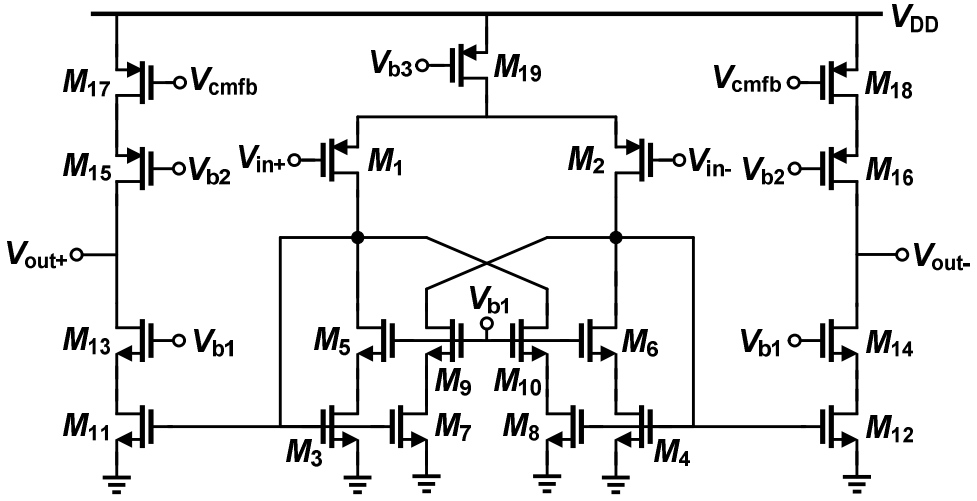

Fig. 2: A fully-differential single-stage OTA.

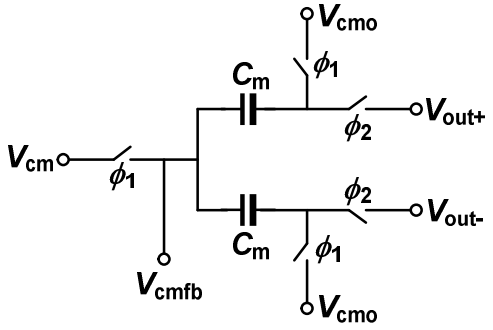

Fig. 3: CMFB circuit.

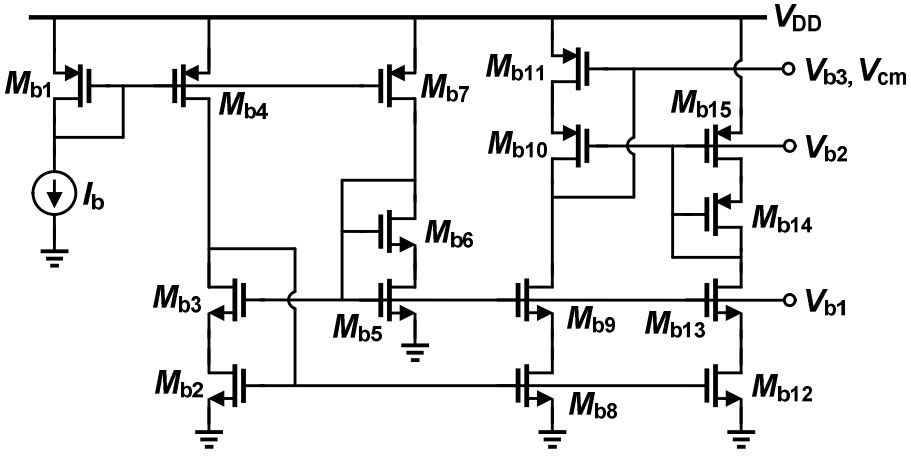

Fig. 4: Bias circuit.