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A low-power and area-efficient quaternary adder based on CNTFET switching logic

Shirin Fakhari[1] · Narges Hajizadeh Bastani[2] · Mohammad Hossein Moaiyeri[1]

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Abstract
Due to the increasing short channel effects in scaled CMOS circuits, the need for alternative technologies has substantially been increased. Moreover, the limitation in space consumed by interconnects and increased power density in nanoscale binary circuits have challenged the scaling process to achieve more efficient and denser circuits. Accordingly, designing efficient nanoscale multiple-valued circuits is of great importance. In this paper, a low-power and area-efficient quaternary adder based on CNTFET switching logic is proposed. The proposed design significantly reduces the number of transistors, area and power consumption, while maintaining output driving capability and full swing operation. The proposed design is comprehensively simulated using HSPICE and the Stanford CNTFET model. Furthermore, the layout of the proposed circuit is drawn using the physical design tool for CNTFET-based circuits. The results confirm significant improvements regarding of area, average power consumption, PDP, static power dissipation and sensitivity to process variations compared to its state-of-the-art counterparts. Also, the proposed quaternary full adder is exerted as the building block of a 4-digit quaternary ripple carry adder, and the simulation results indicate its superiority regarding of energy efficiency.

Keywords Nanoelectronics · CNTFET · Quaternary logic · Switching logic · Full adder · Multiple-valued logic (MVL) · Nanotechnology

1 Introduction

One of the most important challenges in recent ultra-dense integrated circuits is to reduce the energy consumption and consequently heat generation. Accordingly, area-efficient systems with high speeds and ultra-low power consumption are required. Integrating digital circuits and scaling in the past decades has met these multifaceted needs. However, CMOS technology has encountered many challenges in the scaling process, including intensively increased power density, high leakage currents, reduced gate control, short channel effects and high sensitivity to process variations. As a result, the need for using new nanoscale technologies has been raised [1, 2]. Carbon nanotube field effect transistor (CNTFET) is contemplated to be an appropriate alternative to MOSFET transistors because of its inherent similarity to the MOSFET but higher carrier mobility, smaller parasitic capacitors, and therefore lower latency and power consumption. Moreover, another advantage of CNTFET is the equality of the electron and hole mobilities [3]. Also, the unique feature of CNTFET is the ability to determine the threshold voltage by changing the diameter of the CNTs [4], which is very useful in designing multiple-valued logic circuits.

On the other hand, the main problem with the binary system is the limitation of the number of interconnects inside and outside of the chip. By increasing the density of chips, the placement and routing problems of digital logic elements has been deteriorated. Furthermore, increasing the number of pins leads to problems in the packaging process such as increasing temperature. Making use of higher radices can alleviate these problems. Multiple-valued logic is a promising option for increasing the information stored and transmitted in a chip [5, 6]. Multiple-

✉ Mohammad Hossein Moaiyeri
h_moaiyeri@sbu.ac.ir

[1] Faculty of Electrical Engineering, Shahid Beheshti University, G.C., Tehran 1983963113, Iran

[2] Department of Computer Engineering, Yadegar-e-Imam Khomeini (RAH) Shahre Rey Branch, Islamic Azad University, Tehran, Iran

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valued logic is a hybrid of binary logic and analogue signal processing which provides noise benefits of a digital signal while processing more informational in the analogue manner [7]. While binary logic can be used to represent static manner, higher radices such as quaternary logic can be used to represent dynamic behavior in the real world. The quaternary logic provides fair estimates of the transition between two states since it indicates two levels of logic between the highest and lowest levels [8]. Moreover, quaternary circuits provide efficient interactions with binary circuits as the quaternary digits (qits) can be easily converted to bits and vice versa.

The most important part of any microprocessor is the arithmetic unit, which mainly parts in the power consumption and latency of the processor. Since adder is the most important functional unit in the arithmetic unit, improving its performance can enhance the efficiency of the whole processor. In this paper, an efficient CNTFET based quaternary adder is proposed, which significantly reduces the number of transistors and consequently leads to a smaller area and significantly lower energy consumption in comparison to its latest counterparts.

This rest of the paper is structured as follows: The backgrounds of research are reviewed in Sect. 2. The proposed CNTFET-based quaternary adder is investigated in Sect. 3. Section 4 contains the simulation results and comparisons, and finally, Sect. 5 concludes the paper.

2 Backgrounds of research

In this section, the backgrounds of this study are briefly reviewed.

2.1 Carbon nanotube field-effect transistor (CNTFET)

Carbon nanotubes (CNTs) are graphene sheets wrapped up to form nanotubes [9]. Nanotubes are categorized into single-walled nanotubes (SWNTs) and multi-walled nanotubes (MWNTs). The structure of an SWNT is characterized by a pair of indices (n, m) called the chirality vector. The diameter of a CNT, which dominantly determines its important electrical characteristics, is calculated by Eq. (1) [10].

$$D_{CNT} = \frac{a\sqrt{n^2 + m^2 + nm}}{\pi} = 0.0783 \times \sqrt{n^2 + m^2 + nm} \tag{1}$$

When $|n - m|$ is a multiple of three, the SWNT is metallic (highly conducting). Otherwise, it is a semiconductor [10]. MWNTs and metallic SWNTs can be used as chip interconnects, while the semiconducting SWNTs are used as the channel in the carbon nanotube transistors. Figure 1 shows the schema of a typical CNTFET device.

The gate width of a CNTFET is calculated by Eq. (2) [11].

$$W_{gate} \approx Max(W_{\min}, N.pitch) \tag{2}$$

where, W_{min} is the minimum possible gate width, limited by the lithography, N is the number of CNTs underneath the gate and pitch is the distance between the centers of two adjoining SWCNTs under the same gate.

The threshold voltage of a CNTFET as a function of its CNTs' diameter is obtained from Eq. (3) [12].

$$V_{th} \approx \frac{E_g}{2.e} = \frac{\sqrt{3}}{3}\frac{a.V_\pi}{e.D_{CNT}} \approx \frac{0.43}{D_{CNT}} \tag{3}$$

where, a is the distance of carbon–carbon atoms ($\simeq$ 0.249 nm), Vπ is the carbon π–π bond energy in the

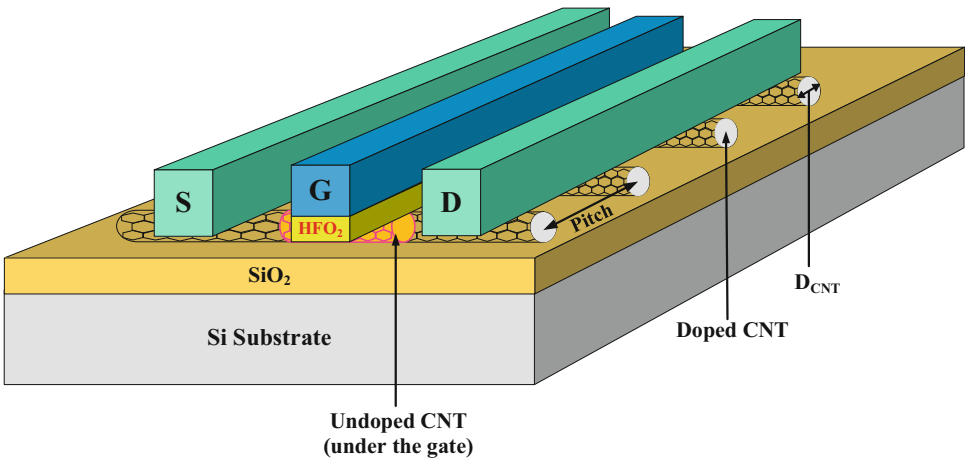

Fig. 1 The structure of a CNTFET

tight bonding model ($\simeq$ 3.033 eV), e is the electron charge, and D_{CNT} is the diameter of the carbon nanotube.

It is notable that the MOSFET-like CNTFET is used for designing the proposed circuit, as this type of CNTFET is more suitable for ultra-energy-efficient digital applications and is more similar to MOSFET in terms of device structure [13].

2.2 Previous CNTFET-based quaternary full adders

The quaternary logic contains four logics, which can be represented by the symbols '0', '1', '2' and '3'. These logic values are usually equivalent to the voltage levels 0 V, 1/3 V_{DD}, 2/3 V_{DD} and V_{DD}, respectively.

As full adder is one the most important basic elements of arithmetic units, energy and area efficient quaternary full adders can significantly enhance the performance of quaternary processing units [14]. A quaternary half adder

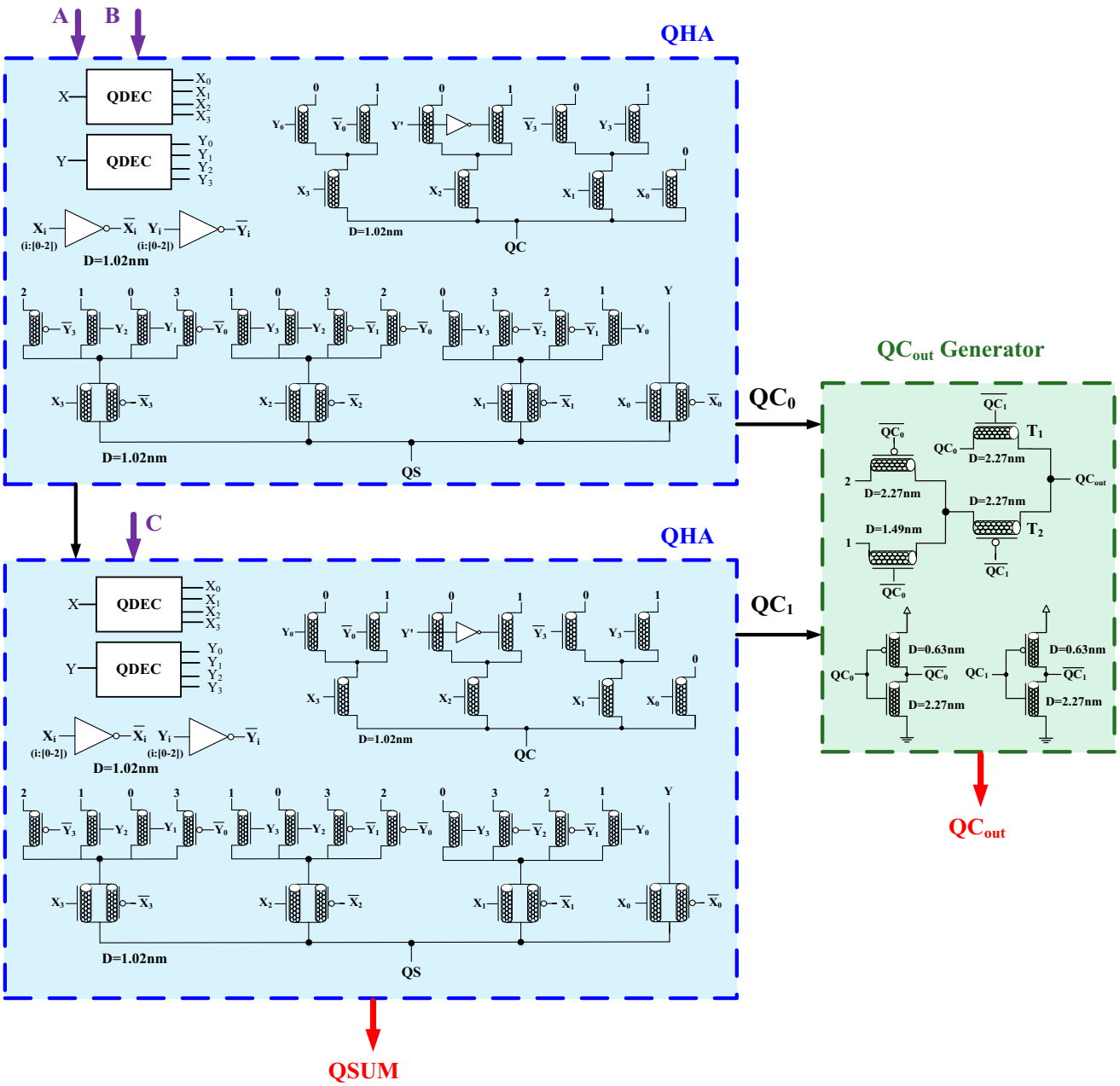

Fig. 2 The proposed quaternary full adder

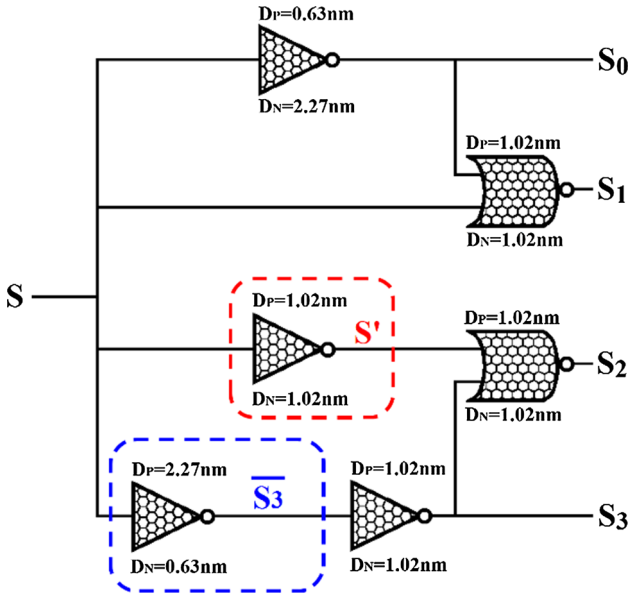

Fig. 3 The quaternary decoder circuit

Table 1 The truth table of the quaternary half adder (QHA)

X	Y	QS	QC
0	0	0	0
0	1	1	0
0	2	2	0
0	3	3	0
1	0	1	0
1	1	2	0
1	2	3	0
1	3	0	1
2	0	2	0
2	1	3	0
2	2	0	1
2	3	1	1
3	0	3	0
3	1	0	1
3	2	1	1
3	3	2	1

(QHA) based on quaternary multiplexers has been introduced in [15]. This design includes a network of quaternary multiplexers that transfers the desired input to the output, according to the half adder's functionality. This design works based on transmission gates, which direct their inputs based on some control signals generated by the quaternary decoders. These decoders convert each of the quaternary input signals into four binary signals.

A quaternary full adder (QFA) has been introduced in [16], based on quaternary-to-binary and binary-to-quaternary converters. This QFA is composed of three modules. The first module takes the quaternary inputs and converts them into two equivalent binary bits. The second module takes these six binary signals and compresses them into four bits, which are two bits for Sum and two bits for Carry. Finally, the third module takes the binary numbers generated from the previous step and creates two quaternary digits. This design has 154 CNTFETs, including 150 transistors with four different threshold voltages and four CNTFET capacitors.

The QFA, presented in [17], is composed of two cascaded quaternary half adders [15] and a simple carry generator unit. This design operates based on quaternary transmission gate networks and pass-transistor multiplexers, whose control signals are generated by some binary decoder blocks. This QFA uses 200 CNTFETs with three different threshold voltages.

Another QFA based on cascaded quaternary half adders and a carry generator unit has been presented in [18]. In the QHA of this design, a decoder is exerted to determine the value of each input. The quaternary decoder has one input and seven outputs. In the next stage, the suitable transistor is chosen, and the correct path connects to the output. This design has 194 CNTFETs with four different diameters.

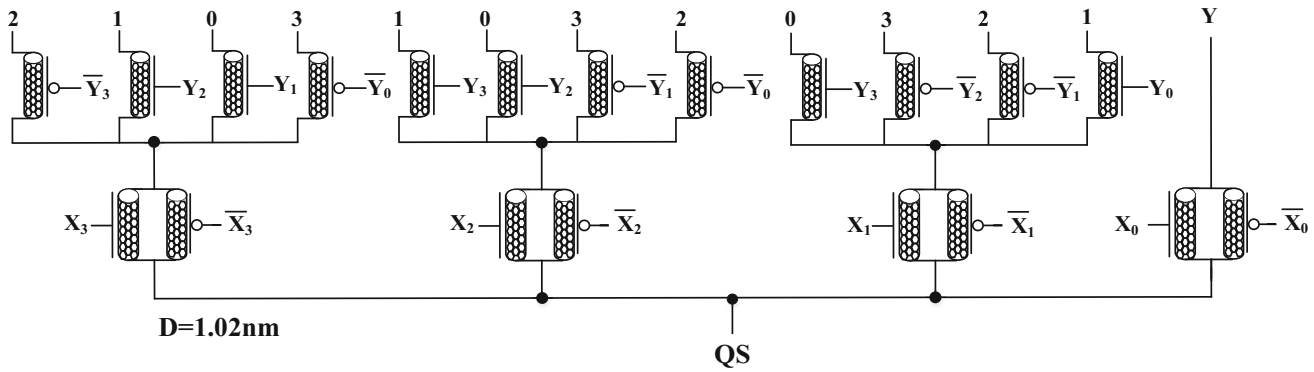

Fig. 4 Proposed quaternary sum generator unit of the quaternary half adder

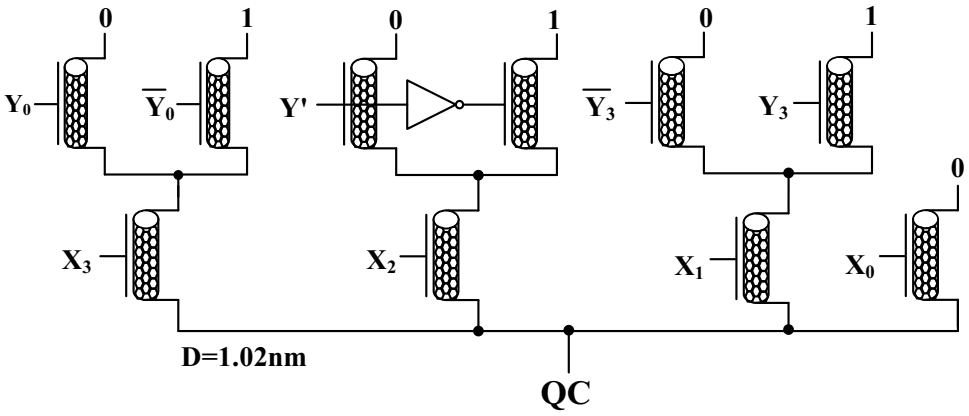

Fig. 5 Proposed quaternary carry generator module

Table 2 QCout functionality based on QC_0 and QC_1

QC_0 (carry of the first QHA)	QC_1 (carry of the second QHA)	QCout (carry of the quaternary full adder)
0	0	0
1	0	1
0	1	1
1	1	2

3 Proposed CNTFET-based quaternary full adder

The proposed quaternary full adder, which significantly reduces the number of transistors and power consumption, is shown, in Fig. 2.

This QFA is composed of two optimized quaternary half adders (QHAs) and an efficient quaternary carry generator unit. In this design, pass transistor logic (PTL) is used effectively to reduce the number of transistors. As a result, the area and power consumption are decreased, while maintaining the output driving capability and full swing operation. In this design, according to Eq. 3, for the CNTFETs with diameters of 0.63, 1.02, 1.49 and 2.27 nm, the threshold voltage values would be nearly 0.7, 0.42, 0.3 and 0.2 V, respectively.

The general structure and functionality of the quaternary decoder (QDEC) circuit, shown in Fig. 3, has been described in detail in [15]. This quaternary decoder is used more efficiently in the proposed design. In the two successive inverters in the bottommost branch of this circuit, the output node of the first inverter is actually the binary invert of the 4th output of the decoder ($\bar{S}_3$). Therefore, the required complement signals $\bar{X}_3$ and $\bar{Y}_3$ in each half adder can be taken from the corresponding node in each decoder. This leads to eight fewer transistors in the proposed design. Also, the S' node which is the unskewed binary invert of the decoder input, is required in the carry generator part of each half adder module.

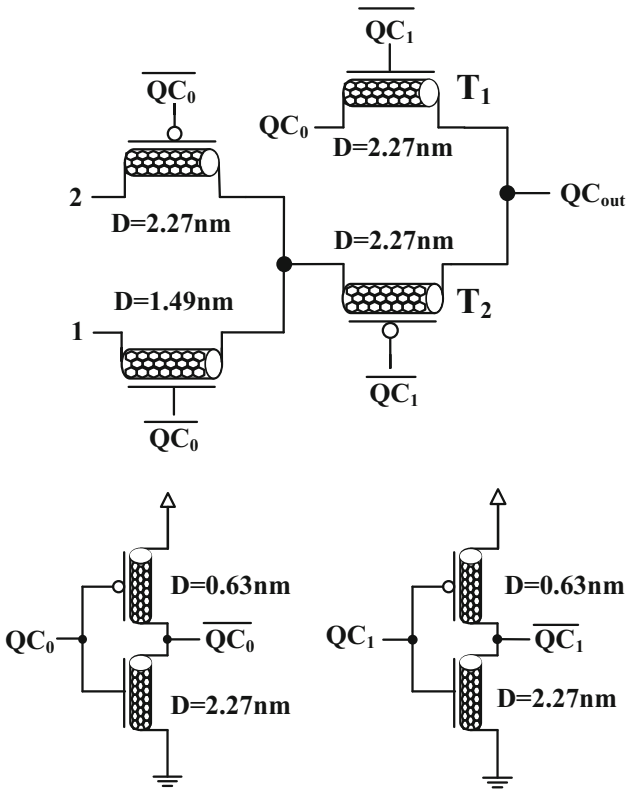

Fig. 6 Proposed QCout generator unit

The truth table of a quaternary half adder (QHA) with X and Y inputs and QS (quaternary sum) and QC (quaternary

C_{out}) outputs is shown in Table 1. According to Table 1, the QS and QC signals can be generated in two by multiplexing quaternary logic levels in two stages, based on the decoded quaternary inputs (X_{0-3} and Y_{0-3}) as described in [15].

Figure 4 shows the Sum unit of the proposed efficient quaternary half adder. In this design, pass transistors are used properly at the first stage as it is not necessary to transfer the inputs by the transmission gates. According to the four available logical levels, '0' and '1' are passed by n-type CNTFETs, and '2' and '3' are passed by p-type CNTFETs without any voltage drop. This efficient use of pass transistors results in a significant reduction in the number of transistors (12 transistors), lower switching power consumption (smaller capacitors) and lower static power dissipation (lower I_{OFF}) compared to the structure presented in [15] while maintaining the full swing operation.

A simple module is used to generate the quaternary carry (QC) signal in the proposed half adder circuit, which is shown in Fig. 5. This structure significantly reduces the complexity of the QHA circuit. As shown in Table 1, in the QC module, only '0' and '1' logical levels exist. Therefore, only n-type CNTFETs can be used to pass the desired logics to the output with full voltage swing. It is notable that the Y' signal is the unskewed binary invert of

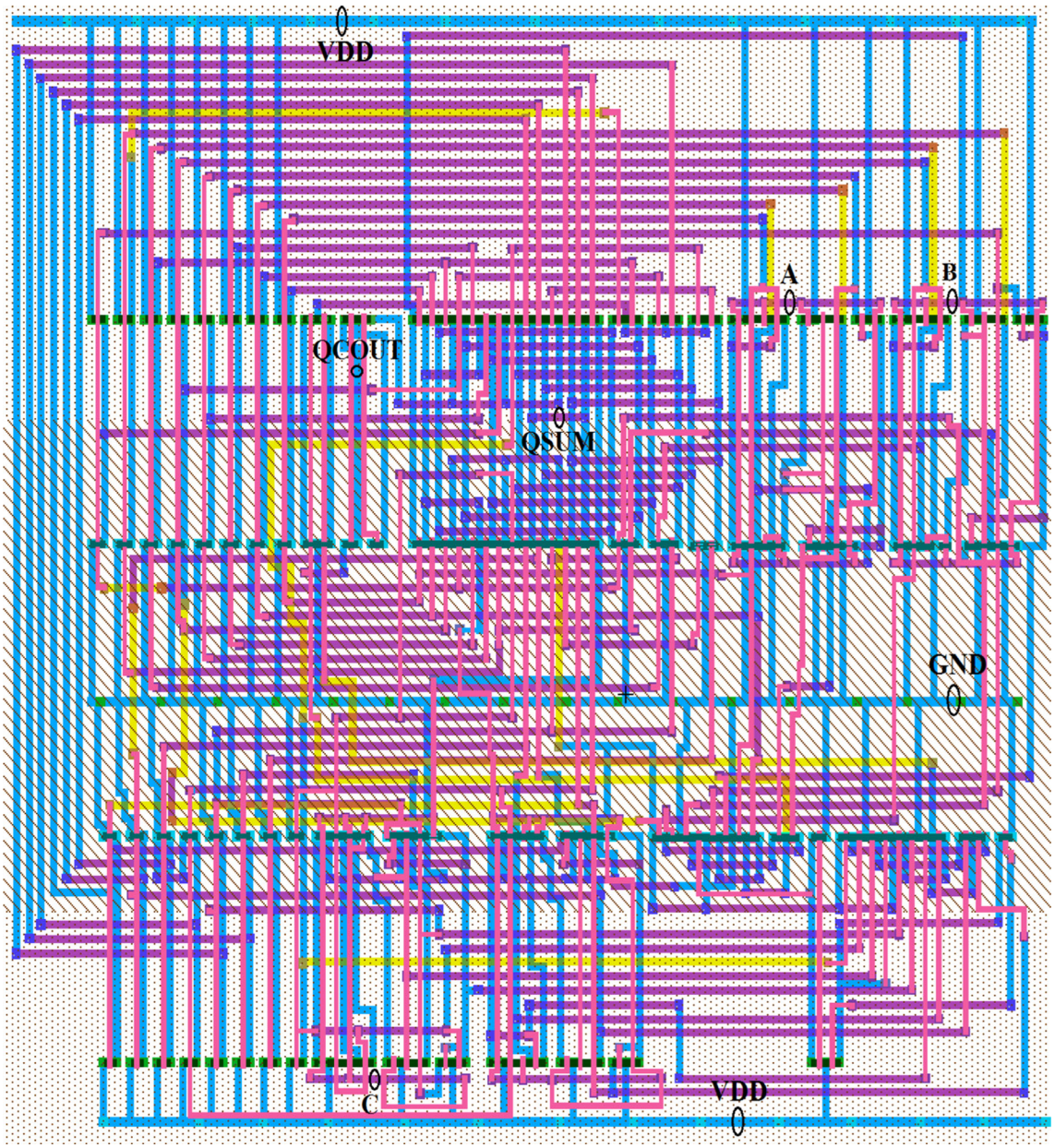

Fig. 7 The layout of the proposed quaternary full adder

Table 3 Some MOSFET-like CNTFET Model Parameters

Parameter	Brief description	Value
Sub_pitch	Sub-lithographic pitch	4 nm
L_{eff}	The mean free path in p+/n+ doped CNT	15 nm
L_{ch}	Physical channel length	32 nm
L_{geff}	The mean free path in the intrinsic CNT	100 nm
L_{dd}	The length of doped CNT drain-side region	32 nm
L_{ss}	The length of doped CNT source-side region	32 nm
T_{ox}	The thickness of high-k top gate dielectric	4 nm
K_{ox}	The dielectric constant of high-k top gate dielectric material (HfO_2)	16
K_{sub}	The dielectric constant of substrate (SiO_2)	4
C_{sub}	The coupling capacitance between the channel region and the substrate (SiO_2)	40 aF/μm
phi_M	The work function of S/D metal contacts	4.6 eV
phi_S	CNT work function	4.5 eV
Efi	The Fermi level of the doped S/D CNT	6 eV

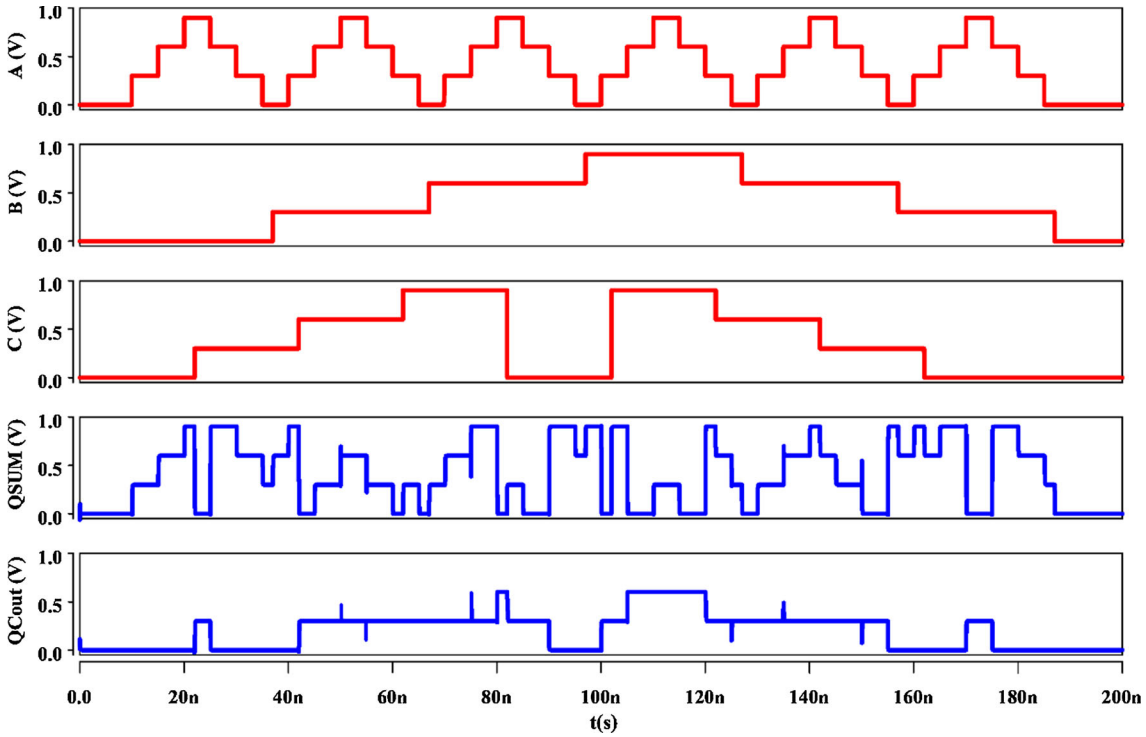

Fig. 8 The transient response of the proposed quaternary full adder

Table 4 Performance comparison of the quaternary full adders

QFAs	Delay (ps)	Average power (μW)	PDP (aJ)	Static power (μW)	Number of transistors
Proposed	131	0.215	28.03	0.11	160
Design of [16]	71.4	50.77	3625	41.6	154
Design of [17]	85.8	7.68	658.9	3.51	200
Design of [18]	213	1.76	374.9	2.25	194

Y input, which is generated inside its corresponding decoder circuit. The proposed QC module has only 12 transistors, which is 28 transistors fewer compared to the QC module of [15].

Table 5 Comparison areas of the designs

Proposed design (μm^2)	Design of [16] (μm^2)	Design of [17] (μm^2)	Design of [18] (μm^2)
26	36	30	28

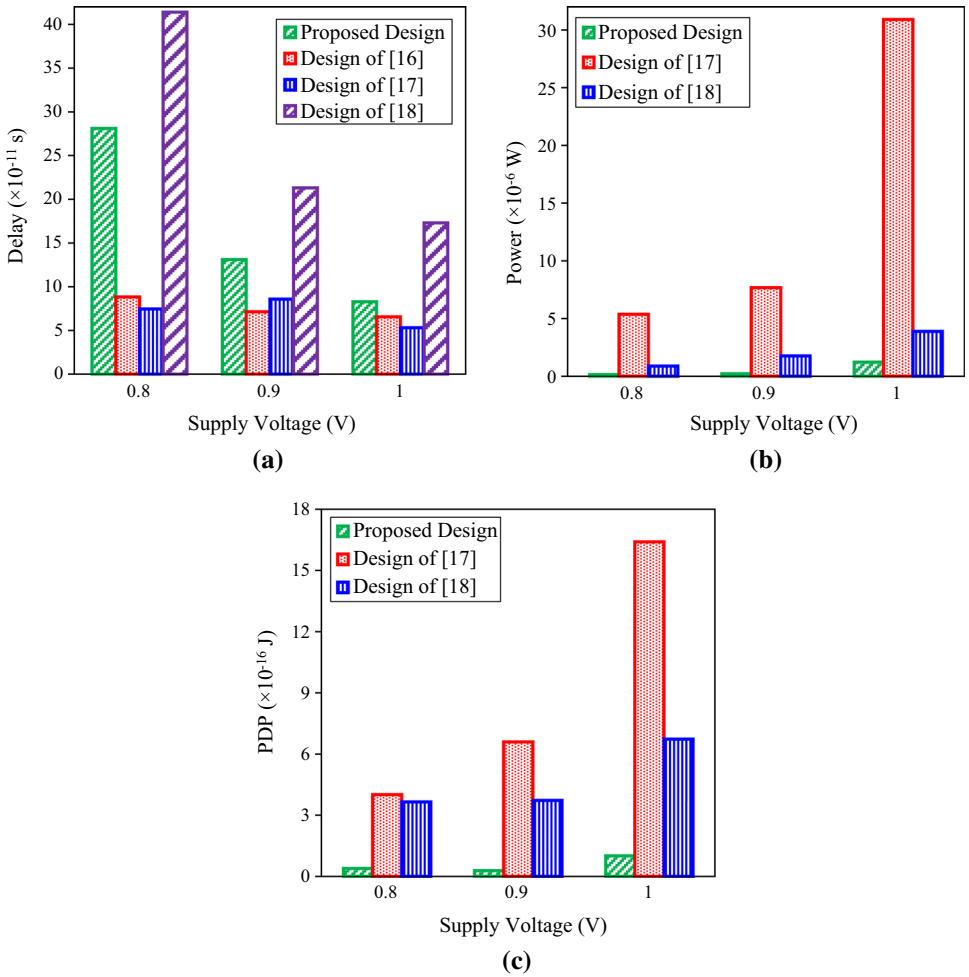

Fig. 9 Performance parameters of the quaternary full adders at different supply voltages. **a** Delay, **b** power, **c** PDP

As shown in Fig. 2, by cascading two proposed quaternary half adders, the Sum output of the quaternary full adder (QSUM) is generated at the sum output of the second QHA. However, to generate the output carry of the quaternary full adder (QC_{out}) based on the carry digits of QHAs (QC_i), additional circuitry is required. Table 2 indicates the relation between the carry digits of the quaternary half adders and the output carry of the quaternary full adder. According to Table 2, an efficient QC_{out} generator module is proposed based on CNTFET pass-transistors, which is shown in Fig. 6.

In this design, the inverters provide 0 → 0.9 V and 0.3→ 0 V inversions. To prevent ON state static power dissipation in these inverters when the input is 0.3 V ('1'), the diameters of the p- and n-type CNTFETs are adopted as 0.63 and 2.27 nm, respectively. The proposed QC_{out} generator module consists of three mutually exclusive paths. When QC_1 = '0', T_1 switches ON and the QC_0 signal is transmitted to QCout. Also, when QC_1 = '1', T_2 switches ON and QC_{out} is obtained based on the value of the QC_0 signal. According to the threshold voltage of pass transistors, when QC_0 = '0', the logic '1' is transmitted to the output, and when QC_0 = '1', QC_{out} becomes '2'.

One of the most prominent advantages of the proposed design is that by cascading the proposed full adder (QFA) to make larger adder structures, the output signals of the preceding level QFA do not enter to the drain node of any transistor in the next level QFA. This prevents the RC chains from being extended too long and consequently avoids long propagation delay in larger structures.

The layout of the proposed QFA, designed using Electrical and the physical design rules for CNTFET circuits [19], is shown in Fig. 7.

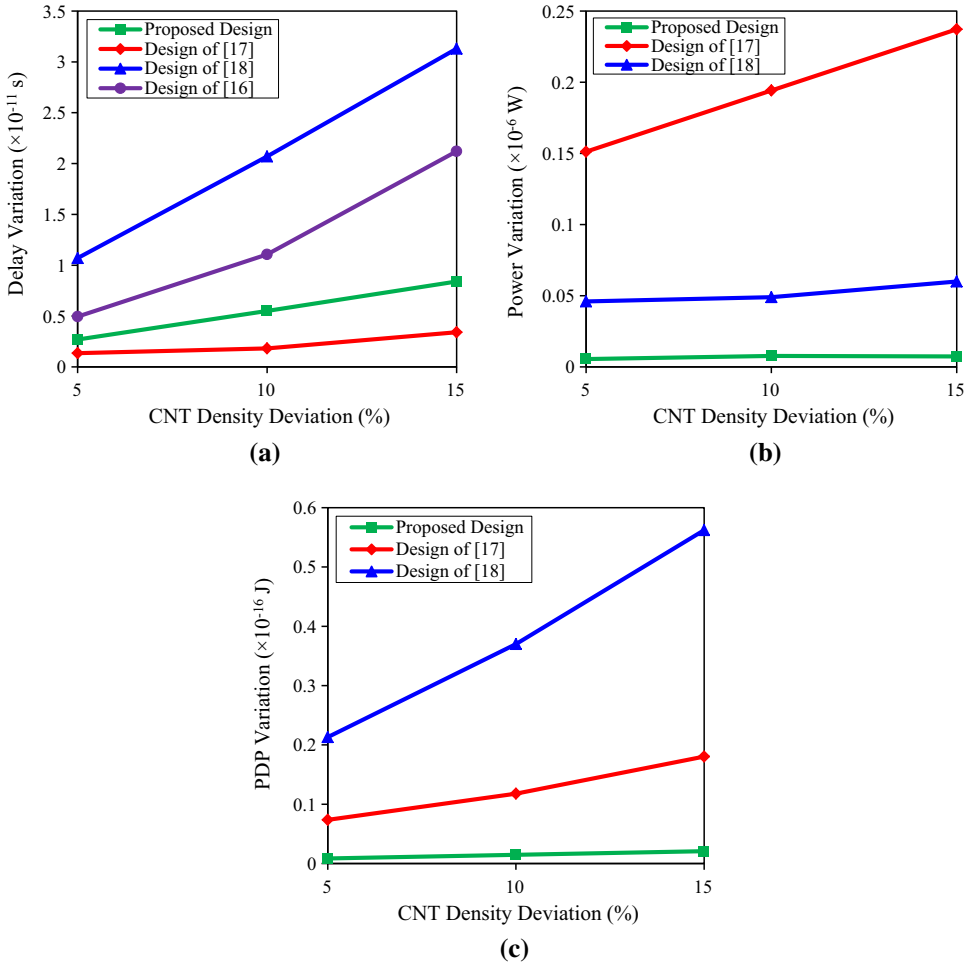

Fig. 10 Parameter variations of the quaternary full adders in the presence of CNT density variation. **a** Delay variation, **b** power variation, **c** PDP variation

4 Simulation results and comparisons

To evaluate and compare the designs, comprehensive simulations are conducted using the Synopsis HSPICE tool and the Stanford CNTFETSPICE model [12, 20, 21]. This standard model includes all non-idealities and parasitic elements. It is designed for MOSFET-like CNTFETs with one or more nanotubes in the channel area. It also considers all non-idealities, such as the inter-CNT charge screening effect, Schottky barrier effect at the contacts and doped source-drain extension regions. Some of the important parameters of this model and their values are listed in Table 3.

The transient response of the proposed quaternary full adder circuit is shown in Fig. 8, which authenticate its correct operation. Evaluation criteria including propagation delay, average power consumption, power-delay product (PDP), static power dissipation, transistor count, occupied area and sensitivity to major process variations are considered for comparisons. Table 4 shows the results at 0.9 V with 0.7fF load capacitor. According to the results, the proposed circuit has significantly lower average power consumption, PDP and static power compared to all designs, and has a considerably lower delay than [18]. It also has considerably fewer transistors than its counterparts, except [16]. Although the design presented in [16] has six fewer transistors than the proposed design, it occupies a larger area due to the use of capacitors as its constructive elements.

Table 5 shows the area of the CNTFET-based quaternary full adders under investigation. As expected, the proposed design occupies a smaller area compared to its counterparts due to its fewer transistors. It is noteworthy that, as predicted before, the design of [16] has the largest area, due to the use of large CNTFET capacitors with a high number of nanotubes.

The proposed circuit has improved average power, PDP, and static power on average by 94, 95, and 97%, respectively, compared to the other related designs. The main reasons for these improvements are the significant reduction in the number of transistors and the proper use of pass transistors that leads to smaller switching capacitors in the circuit while maintaining the full-swing operation.

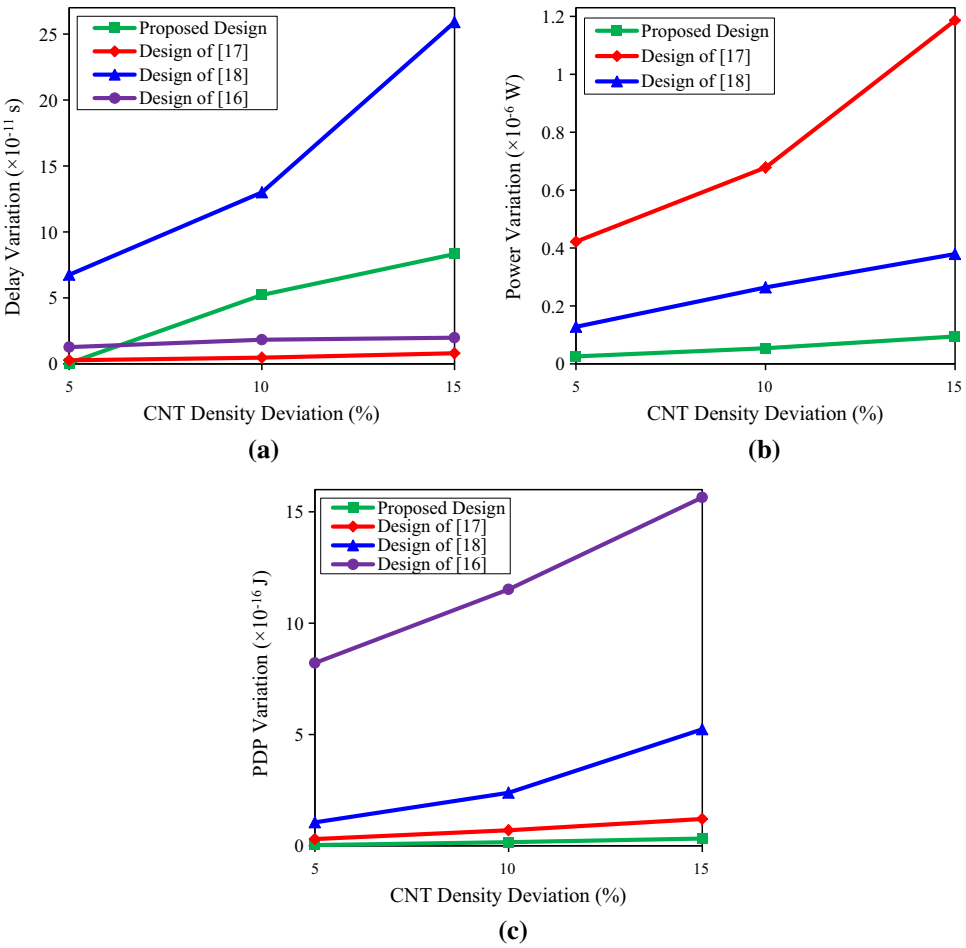

Fig. 11 Parameter variations of the quaternary full adders in the presence of CNT diameter variation. **a** Delay variation, **b** power variation, **c** PDP variation

Table 6 Performance parameters of the 4-qit QRCAs

4-qit QRCA	Delay (ps)	Power (μW)	PDP (fJ)
Proposed design	280	1.77	0.50
Design of [16]	190	184.8	35.11
Design of [17]	140	38.5	5.39

Another important factor in the evaluation of a digital circuit is its ability to function properly in the presence of supply voltage variations. Therefore, the performance parameters of the circuits are evaluated at 0.8, 0.9 and 1 V, and the results are shown in Fig. 9.

According to the results of Table 4, the power consumption of the design [16] is significantly higher than the other designs. Therefore, this design is not considered in the charts of the power and PDP against supply voltage variations (Fig. 9(b, c)). The results indicate that the proposed design operates with high performance and outperforms its counterparts regarding power consumption and energy efficiency at different supply voltages.

One of the most important challenges in nanoscale circuits is sensitivity to process variations, which can lead to unwanted parametric variations and negative impacts on the performance of circuits. Thereupon, the effects of random process variations on the diameter and the density of nanotubes, as two major process variations in CNTFET circuits [22], are evaluated in the quaternary full adders under investigation. According to Eq. 3, the changes in the diameter of the nanotubes cause threshold voltage changes in the transistors. Furthermore, changing the nanotubes density directly effects on the ON current, driving capability of the circuits and the value of the gate and parasitic capacitors. To investigate these process variations, Monte Carlo simulations have been conducted considering 5–15% variations with the Gaussian distribution at the $\pm 3\sigma$ level. The results of these simulations are presented in Figs. 10 and 11. According to the results, the power consumption and PDP of the proposed design have the least variations compared to other designs, specifically due to the lower number of transistors and lower variety of the diameters in the proposed circuit.

To verify the performance of the proposed circuit as a building block of larger computational blocks, a four

quaternary digit (qit) quaternary ripple carry adder (QRCA) circuit is considered. To estimate the worst-case delay, a C++ code has been developed to generate all of the possible inputs that lead to signal propagation on the critical path of a 4-qit QRCA. All of the quaternary full adder circuits are simulated in this platform, and the results are presented in Table 6. Based on the results, in spite of relatively longer delay of the proposed circuit than the other circuits, the power and PDP are dramatically reduced. It should be noted that the scheme [18] did not function properly for some of the inputs, and hence its results have not been reported in this section.

5 Conclusion

In this paper, an efficient quaternary full adder (QFA) based on CNTFET switching logic. In this design, pass transistor logic (PTL) is used effectively to reduce the number of transistors. Hence, the area and power consumption is decreased, while maintaining output driving capability and having full swing operation. An advantage of our PTL design is that by cascading the proposed QFA to make larger adder structures, such as QRCA, the output signals of the preceding level QFA do not enter to drain of any transistor in the next level. This prevents the RC chains from being extended too long and avoids very long propagation delay. Comprehensive simulations have confirmed significant improvements regarding average power consumption, PDP, static power and sensitivity to process variation, compared to its most recent CNTFET-based counterparts. The simulation results also have proven that the proposed circuit has outperformed the other existing QFAs regarding of energy efficiency when it is used as the building block of larger arithmetic circuits.

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Shirin Fakhari received her M.Sc. in Electrical Engineering from Shahid Beheshti University, Tehran, Iran in 2018. Her research interests mainly focus on VLSI design based on nanoelectronics and multiple-valued logic.

Narges Hajizadeh Bastani received her Ph.D. in computer architecture from Science and Research Branch of Islamic Azad University, Tehran, Iran in 2017. She is currently an assistant professor in Department of Computer Engineering of Shahre Rey Branch of Islamic Azad University. Her research interests include VLSI design based on nanoelectronics, multiple-valued logic and approximate computing.

Mohammad Hossein Moaiyeri received his Ph.D. in computer architecture from Shahid Beheshti University, Tehran, Iran in 2012. He is currently an assistant professor in Faculty of Electrical Engineering of Shahid Beheshti University. His research interests mainly focus on nanoelectronic circuit design, Low-power VLSI design, VLSI implementation of MVL and fuzzy logic and mixed-signal integrated circuits design.