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Protection of low voltage DC microgrids: A review

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ABSTRACT

The technological escalation in DC power generation from renewable energy sources has attracted the attention of researchers to the concept of DC microgrids (DCMGs). However, the design and development of tailor-made schemes to fulfil the complete protection requirements in a DCMG remain a challenge. Practical inexperience, lack of standards, and differences in the behaviour of the DC system compared to AC aggravate the issue. This paper throws light on the latest advancements and research prospects in DCMG protection by traversing through the developments in DC protection standards, fault detecting and locating techniques, the impact of faults on the power electronic converters, the role of converters in fault handling, and DC circuit breaking.

1. Introduction

The war of currents had been settled long ago. However, the increased penetration of renewable energy sources, predominantly solar, together with the increase in DC loads and advancements in power electronic converters, has led to the resurrection of DC in the electrical power distribution system in the form of DCMGs. They can be configured in different topological structures [1,2] as shown in Table I, and can be implemented at different voltage levels based on the field of application, as listed in Table II. At present, the DCMG is gaining importance due to its own merits [3,4] over the AC microgrid such as the elimination of synchronization concerns, high power flow capacity, reduction in the number of converters required leading to lesser heat, and drop in cable loss due to the absence of skin effect [5]. However, despite the attractive advantages, there are several areas of concern with the DCMG that need to be addressed [6], such as stability concerns [5], complexity in the design of controllers, and protection issues.

This paper reviews the latest developments in the protection of Low Voltage DC (LVDC) microgrids. DC voltages below 1500 V are considered LVDC, within which voltage levels of 120 V and below fall under the Extra Low Voltage DC category. The remaining sections of this paper are organized as follows. Section 2 describes the short circuit current calculations in DC systems. Section 3 lists the international standards established for DC systems and discusses the areas where new or modified standards are required for DCMGs. The protection strategies for DCMGs are explained in Section 4. It reviews the fault detecting techniques along with online and offline fault-locating methods proposed for DCMGs. The impact of internal and external faults on power electronic converters is discussed in Section 5. This section also reviews fault tolerant and fault current limiting converters. Section 6 analyses the grounding methods used in DCMGs and their impact on fault detection. Section 7 elaborates on the different topologies of DC circuit breakers and fault current limiting devices. The conclusions and potential research areas in DCMG protection that are identified as a result of this work are presented in Section 8.

2. Short circuit current calculations

Formulating accurate mathematical models for the computation of short circuit (SC) currents is essential for the selection, sizing and design of any protection system. The maximum SC current is a deciding factor in selecting the rating of electrical equipment, and the minimum short-circuit current governs the rating and setting of protective devices [22]. The SC current calculations are also required for determining the severity of arcing faults [23] and for the design of fault current limiters (FCLs) required in assisting the CBs [24].

According to International Electrotechnical Commission (IEC) standard [25], a method for computing the SC current in DC systems is defined with reference to auxiliary installations in power plants and substations where the contribution of fault current is possibly due to converters, batteries, capacitors and DC motors. Fig. 1 represents the typical SC current contributions from each of these sources. As the nature of SC current from different sources differ, it is necessary to formulate detailed calculations for each of them separately and then superpose their effects to arrive at a generalized mathematical model. Fig. 2 represents the standard approximation function covering the

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Table I
Comparison of DCMG Architectures.

Features	Architecture				
	Radial	Ring	Ladder	Meshed	Zonal
System cost	Low	Medium	High	Very High	Highest
Design of protective system	Easy	Moderate	Difficult	Very Difficult	Complex
Reliability of supply	Low	High	High	Very high	Excellent
Number of interconnections with the AC grid	One	One	Multiple	Multiple	Multiple
Redundancy	Very Low	Moderate	High	High	High
Applications where suited	LVDC distribution, Residential, Traditional shipboard Power systems	Data center/ telecommunications	Data center/ telecommunications	Data center/ telecommunications	Shipboard Power systems

Table II
Voltage Levels in DCMG Applications.

Application	LVDC Voltage levels	Advantages	Disadvantages
Residential [7], Telecommunications [7,8]	48V	• Extra-low Voltage level • Safe withstand voltage level even under saline humid environment	• For large power appliances, the current drawn will be high leading to significant power loss and enhanced DC circuit breaking requirements.
DC charging- Indian electric cars [9]	48V/72V		
Spacecraft [8]	28V, 120V		
Aircraft [10,11]	270V, 540V (±270)	• Low isolation distances are sufficient, which is particularly suitable in densely populated areas	
Data Centres	380V [12,13], 400 V [7]		
Commercial [7]	400V		
Industrial [14,15]	600,750V	• Lesser losses in the lines • Suitable for geographically wider networks	• Higher electrical stresses • Higher insulation requirement • Chances of potential-induced degradation when PV modules are interconnected for higher voltages. • Strict scheduled maintenance requirements
DC charging- Global electric cars [16,17]	up to 800V		
Shipboard Power Systems [18, 19]	>1 kV with zonal topology; upto1 kV otherwise		
Traction [20,21]	600, 650, 750, 1200, 1500 V		

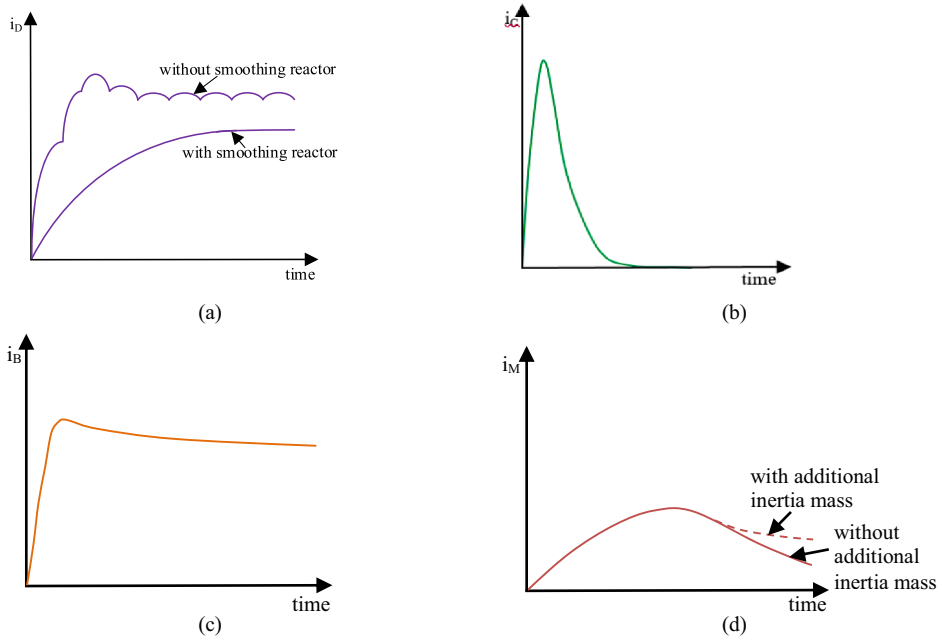


Fig. 1. Typical SC current waveforms of different sources (a) 3-phase Diode bridge rectifier with and without smoothing reactor. (b Capacitor (c) Battery (d) Motor with and without inertia mass [22] i_D – Diode current, i_C – Capacitor current, i_B – Battery current, i_M – Motor current.

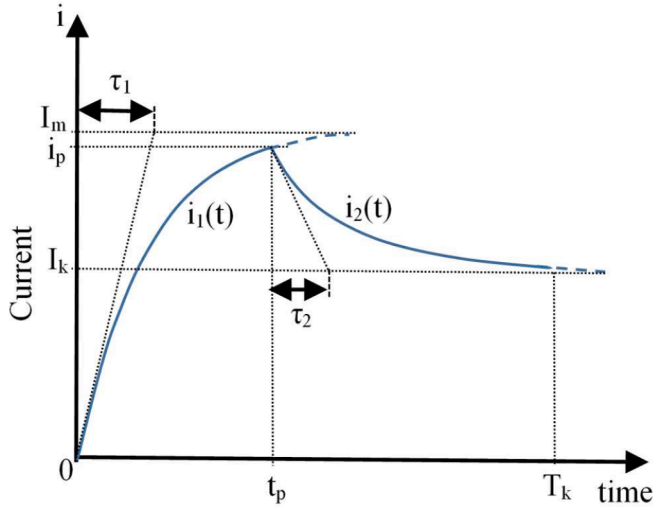


Fig. 2. Standard approximation of the SC function [22].

independent current variations from the different sources as proposed by IEC, mathematically represented by (1)-(3). It shows the mathematical model of the SC current contributions from the different sources, neglecting the effect of fault impedance and shunt load resistances.

$$i_p = I_m\left(1 - e^{-\left(t_p/\tau_1\right)}\right) \tag{1}$$

$$i_1(t) = I_m\left(1 - e^{-(t/\tau_1)}\right) i_1(t) = i_p \frac{\left(1 - e^{-(t/\tau_1)}\right)}{\left(1 - e^{-\left(t_p/\tau_1\right)}\right)};\ for\ 0 \le t \le t_p \tag{2}$$

$$i_2(t) = \left(i_p - I_k\right)\ e^{-\left(t - t_p\right)/\tau_2});\ for\ t > t_p \tag{3}$$

In Fig. 2, conventionally, I_k is taken as the value of SC current, 1 s after the occurrence of SC, τ_1 and τ_2 are the time constants of rising and decaying parts of the current, i_p is the peak value of SC current occurring at time t_p and T_k is the duration for which the SC current persists until it is completely interrupted by the breaker. Accurate SC current calculation methods facilitate the predetermination of injury resulting from an SC fault. Development of detailed mathematical models that can completely describe the variations in SC currents, at the SC location, throughout the fault duration is essential.

In AC/DC interconnected systems fault currents can be contributed from either side [26]. The contribution of fault current from the DC side becomes significant if its transmission capacity is large and is connected to a weak AC system. Even though simplified techniques for estimating DC SC currents are proposed in the literature [27,28], SC current computations for DCMGs with renewable energy sources and dynamic loads in grid-connected and islanded modes of operation are yet to be standardized. The following section describes the standards developed for DC systems and examines their applicability to DCMGs.

3. Standards for DCMGs

In order to enable extensive inclusion of the DCMG into the existing AC grid, framing standards that define the selection, rating, design, and operation of each component in the DCMG for various operating conditions are inevitable. Standards for DC systems have been formulated by the Institute of Electrical and Electronics Engineers (IEEE) and the IEC, as listed in Table III.

For the integration of LVDC microgrids into the smart grid environment, standards such as IEEE 1547 [29] are defined for AC microgrids. Revisions of this standard are also established, namely IEEE 1547–2018 [30], which focuses on the technical specifications for the interconnection and interoperability between utility electric power systems and Distributed Energy Resources (DERs) and its testing, and IEEE 1547a-2020 [31] which widens the ranges for trip settings. Development of corresponding standards are essential for the DCMG.

Some modifications proposed in existing standards are given below:

IEC61660–1 standard provides a method for calculating the short-circuit currents in DC auxiliary installations in power plants and substations [25]. This standard is designed for radial DC systems; however, with modifications, it can be used to estimate SC currents within tolerable errors in meshed dc networks as well [35]. During a short circuit, the capacitors in a meshed DC network discharge through the inductive power circuit leading to LC oscillations. These conditions should be explored for possible inclusion in the standard. Also, in IEC 61,660 standard, the rectifier source is an infinite source with large inertia. However, in DCMGs, rectifier-based sources are small generators with low inertia. Therefore extreme care should be taken in the fault-curent computations of DCMGs to mitigate the error in actual and estimated values. A possible solution is to introduce appropriate correction factors in the computations.

International power quality standards IEEE 1159 and IEC 61,000, developed for AC systems, have majority of the definitions applicable to DC microgrids as well. Voltage variations, transients, noise, notching and voltage fluctuations are issues similar to those in AC microgrids. However, power quality issues such as harmonics, offset and power frequency are terms that are not defined for a DC microgrid. Also, power quality issues in DCMGs generally shift to higher frequencies due to the operation of switched-mode power converters, bandwidth of the controllers and fast dynamics of DC faults [36]. Modifications to IEEE Std1159 and IEC 61,000 power quality standards, to account for the above, will enable the same to be used in DC microgrids.

Standardisation in DCMGs is essential in the following areas:

The voltage levels in DCMGs [8] for different applications, such as residential, transportation, medical, industrial etc., are not standardized. Voltage standardization will depend on the safety, cost, energy efficiency, compatibility with existing system components, and range constraints [37]. Also, the permissible tolerances in voltage levels and transient voltage disturbances are also not well defined [12]. It is interesting to note that in applications such as shipboard power systems, regulations and standards are in the nascent stage [19]. Power metering equipment in DC requires unique standardisation due to the fundamental differences in power and energy measurement methods in AC and DC. Updating product standards of DC utilization equipment such as lighting, motor drives, and electric vehicle equipment is essential for accelerating the commercialization of DC power. Standardisation is also required with respect to interconnection methods and locations of DERs, islanding, microgrid control, conductor sizing, interrupting current and safety considerations [37]. Investigating the suitability of existing DC standards in a DCMG environment could lead to promising results in developing new standards for DCMG installations.

At present, even with lack of fully established standards considerable effort has been put forth to establish protection schemes in a DCMG. The techniques for detecting and locating faults in a DCMG are discussed in the following section.

4. Protection strategies for DCMGs

In developing protection strategies for DCMGs the initial attempts were to extend the concepts of protection schemes used in the conventional AC grid to the DCMG systems. However, due to the fundamental difference in AC and DC fault current patterns, techniques exclusively suited for FD in DC systems are necessary. Several techniques have evolved, both conventional and new, as illustrated in Fig. 3.

4.1. Fault detection and protection

4.1.1. Methods based on the techniques used in the conventional AC system

Out of the methods already in force in the AC grid, differential protection is the one whose basic concept can be directly applied in the

Table III
Standards for DC Systems.

Standard	Title	Description
IEEE P2030.10/D07	IEEE Draft Standard for DCMGs for Rural and Remote Electricity Access Applications [13]	• Covers the design and operation of rural and remote stand-alone DCMGs of extra-low voltage levels • The primary considerations are reduction in cost, improved stability, and safety.
IEEE P2030.10.1	Standard for Electricity Access Requirements with Safety Extra Low Voltage (SELV) DC for Tier II and Tier III of Energy Sector Management Assistance Program (ESMAP) Multi-tier Framework for Household Electricity Supply	• Defines requirements for energy access outlined in Tier 2 (product kits) and Tier 3 (fixed installations) of the Energy Sector Management Assistance Program (ESMAP) Multi-Tier Framework for Household Electricity Supply.
IEEE P2030.10.2	Standard for Electricity Access Requirements for DC low power not exceeding 60V	• Specifies the general requirements of systems supplied from low-voltage DC sources and energy storage devices not exceeding 60V
IEEE 946-2020	IEEE Recommended Practice for the Design of DC Power Systems for Stationary Applications [32]	• Provides guidance for determining the quantity, type, and rating of storage batteries, static battery chargers/rectifiers, distribution, protection and control equipment, and their interconnections • Describes the factors to be considered based on the load, and calculation of SC current contributions of the different components • The main considerations are to improve the performance, reliability, and safety of stationary DC power systems
IEEE 1709-2018	IEEE Recommended Practice for 1 kV to 35 kV Medium-Voltage DC Power Systems on Ships [33]	• Specifies the analytical methods, interface interconnections, desired performance parameters, and testing conditions for ship-based Medium Voltage DC (MVDC) power systems
IEEE C37.14-2015	Standard for Low-Voltage DC Power Circuit Breakers Used in Enclosures [34]	• This standard covers the preferred ratings and testing requirements of enclosed DC power circuit breakers of the following types: a) Stationary or draw-out type of single or two-pole functional construction b) Having rated maximum voltages of up to 3200 V c) Manually operated or power-operated d) With or without overcurrent trip devices
IEC 61660-1	Short-circuit currents in DC auxiliary installations in power plants and substations-Part 1: Calculation of SC Currents	• Describes methods for calculating short-circuit current contributions of rectifiers (of 3-phase AC bridge connection for 50 Hz), stationary lead-acid batteries, smoothing capacitors, and DC motors with independent excitation, in DC auxiliary systems of power plants and substations.
IEC 61557-1:2019	Electrical safety in low voltage distribution systems up to 1000 V AC and 1500 V DC	• Equipment for testing, measuring or monitoring of protective measures
IEC 61992	Railway applications – Fixed installations – DC switchgear	• IEC 61992 series specifies requirements for DC switchgear and control gear and is intended to be used in fixed electrical installations with nominal voltage not exceeding 3000 V DC, which supply electrical power to vehicles for public guided transport.

DC system. The existing literature reveals several strategies proposed for the DC system which are based on differential protection [38–42]. In some cases, differential protection in the DC system is assisted by directional overcurrent protection [43].

4.1.2. Methods developed for DCMG systems

Differential protection, even though effective in DC systems, cannot be considered as the sole solution for the protection requirements in a DCMG, particularly because it is costly and requires communication assistance. Hence the development of new strategies that are specifically suited for the DC system is inevitable [44]. Protection methods based on current, voltage, impedance, communication and intelligent techniques have been proposed for DCMGs. Table IV gives a comparison of the various techniques proposed in literature.

4.1.2.1. Monitoring the variation patterns of parameters. Detecting faults based on threshold levels of voltages or currents may not be sufficient to discriminate a fault from sudden load changes or transients. Montoring the parameter variations can lead to more accurate fault classification. An Event Classification based protection scheme based on fault current magnitude and pattern was proposed in [45]. The challenge is that fault-current magnitude and pattern for a fault occurring at a particular point in an interconnected feeder may be identical to that of a fault occurring at another feeder for a different value of feeder length. The task of discriminating such cases is made possible by introducing a current derivative method and introducing Artificial Inductive Line Impedances. In [46] the rate of change of current is used for fault identification in a shipboard microgrid. Literature [47] uses the first and second-order derivatives of current for FD. The second derivative is used to solve the selectivity issue that arises when only the first derivative is considered. Monitoring current pattern and direction on either end of a line in a DCMG can be used to detect high impedance faults [48]. FD can also be carried out by measuring effective resistance or inductance measurements up to the fault path [49,50]. The calculated value may have a positive or negative sign indicating the direction of the fault.

4.1.2.2. Protection based on power electronic converter control. Converters with fault current limiting capability can participate in the protection scheme by assisting in fault current control. Upon detecting a fault, the current limiting mode is activated and the fault current is prevented from rising to excessive levels. However, not all converters have current-limiting capability. Section 5.3 elaborates this concept further.

4.1.2.3. Handshaking protection. It refers to the use of AC side circuit breakers together with fast-acting DC isolators in Voltage Source Converter (VSC) driven DC microgrids. Used in grid-connected mode and enables to classify and isolate faults. It requires shutdown of the system momentarily, disconnection of faulty lines, and restoration of the healthy system. It does not require communication channels and is cost-effective due to the absence of DC Circuit breakers. Also, the restoration time is unaffected by the size of the microgrid [51]. However, it is not suitable as primary protection, especially when multiple sources are loads are present, and is preferred only as a backup protection due to its selectivity issue [52].

4.1.2.4. Protection Co-ordination. For a grid-connected microgrid, a static switch at the point of interconnection can isolate the microgrid in the event of a fault. The DCMG is resynchronized to the main grid only after the fault is cleared [53]. A combination of several relaying

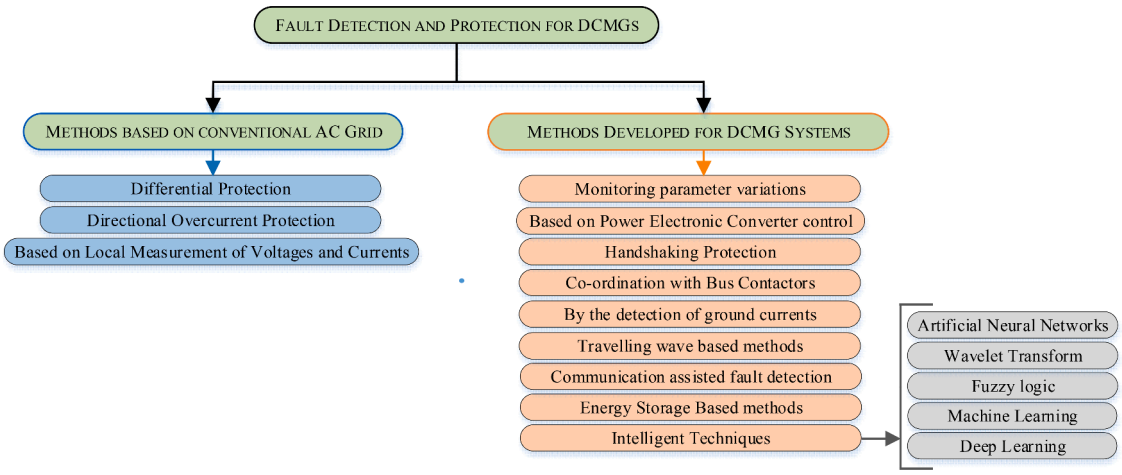


Fig. 3. Protection methods for DCMG systems.

Table IV
Protection Techniques for DCMGs.

Strategy	Methods used	Features	Advantages	Disadvantages
Conventional AC grid based techniques	Overcurrent schemes	• Instantaneous, Definite time and Inverse time characteristics	• Simple in operation	• Does not offer selectivity
	Differential schemes	• Offers unit protection; within the defined zone	• Very high speed of operation • Resistant to variations in fault resistance	• Synchronised measurement is required • High Cost
	Distance protection	• Offers protection to the power lines • Based on Reactance, Impedance, Admittance measurements upto fault point of the line	• Simple algorithm • Easy to provide backup protection	• Affected by fault resistance
Techniques developed for the DC system	Monitoring the parameter variation patterns	• Based on measurement of local system parameters	• Does not require communication channels	• Slow in operation
	Power Electronic Converter control	• Uses fault current limiting capability of converters	• Imparts protection without the need for DC circuit breakers.	• All converters do not have fault current limiting capability • All converters may not be able to control the fault current adequately.
	Handshaking Protection	• Uses AC side circuit breakers together with fast-acting DC switches in a grid-connected DC microgrid	• Does not require communication channels • Cost-effective option for backup protection	• Requires shutdown of the healthy part of the system momentarily • Not suited for primary protection
	Travelling wave (TW) based methods	• Based on analysis of frequency components of travelling waves generated by the fault	• Fast and accurate fault-locating capability	• Not suitable for LVDC systems where distances are short, as the reflected waves may not be significant.
	Co-ordination of Power Converter with Bus Contactors	• Power converters enter current limiting mode • Can isolate the fault in 10-20ms	• Does not require communication between the elements	• Characteristic tripping curves must be formulated and set for the contactor. • May not be able to detect high impedance faults
	Communication based methods	• Uses Power line carrier protection, spread-spectrum radio, fibre-optic cable, phone lines, and copper pilot wire	• High speed • Availability of advanced communication techniques	• Communication system should remain healthy at all times, or else the entire protection system fails
	Energy Storage based methods	• Storage device supplies the additional current required to drive the relay in the event of loss of communication	• Enhances resilient operation against communication outages • Can utilize already existing energy sources in the microgrid	• Optimisation is required to limit the size and cost of storage devices
	Intelligent Techniques	• Uses intelligent tools such as Artificial Intelligence, Fuzzy logic, Wavelet Transform, Machine Learning, Deep learning etc.	• Can be used to detect High impedance faults • Can deal with system uncertainties and chaos	• Difficulty in Training and selection of performance parameters. • Computational burden is more

Table V
Performance comparison of different storage devices.

Storage device	Charging time	Energy density (Wh/kg)	Power Density (W/kg)	Charging/ discharging efficiency	Cyclic Life	Advantages	Disadvantages
Lead Acid Battery	8 – 10 hrs	30-50	250	60-70%	1000	• Simple design and cheap • High energy density	• Weight-to-energy ratio is poor • Battery life is reduced by repeated deep cycling • High Cost • Requires protection against over-charging and under-charging
Lithium Ion Battery	10mins to < 3 hrs	75-200	1000 to 3000	95%	2000-3000	• High energy density • Resilient to high and low temperatures	
Supercapacitor	< 30s	<15	Upto 10,000	85-98%	10^6 cycles	• Faster charge/ discharge capability (larger power density) • Not suited for long-term storage	• Usable power spectrum is less as supercapacitor voltage discharges linearly with charge • Voltage limited to around 2.7V
Flywheel	10 s -10 mins	10-50	1000 to 5000	90-95%	10^5 - 10^6 cycles	• Environment friendly • Lifetime is independent of the depth of discharge • Short response time	• Short self-discharge time • Requires steps to eliminate frictional losses • Mechanical limitations arise with increase in storage capacity

techniques and its co-ordination along with time grading of relays is required within the DCMG. Non-unit protection schemes (NUPS) are required for imparting protection coordination. However, NUPS with relatively small time margins for upstream and downstream protections devices may lead to difficulty in achieving the required levels of protection discrimination, especially in a compact, converter based system like a DCMG. Therefore unit protection scheme with non-unit backup is implemented in cases where coordination with downstream devices has stringent time requirements, and in all other cases NUPS can be resorted to, in order to make the protection system cost-effective [54].

4.1.2.5. Detection of ground faults. Ground faults in DC systems cause a voltage offset which enables easy detection of such faults. However, locating ground faults, especially high-resistance ground faults, is challenging as the offset is uniform throughout the system [55]. In a battery-integrated DCMG, the battery fault current varies considerably, whereas the converter current does not differ much after 1 ms of the fault. Thus fault current from the battery can be directly used for selectivity [56]. For circuits with parallel paths, such as meshed networks, circulating currents are created that cause residual ground fault protection to malfunction. Circulating currents of magnitudes exceeding thresholds can arise due to differences in cable lengths of the various paths or due to tripping of a pole. L. Mackay et al. states that, for the net circulating current to be zero, the ratio of conductance of a branch to the total positive pole conductance should be equal to the similar ratio computed with respect to the negative pole [57].

4.1.2.6. TW based methods. TW methods offer high-speed protection and have been proposed for DC systems in the high and medium voltage ranges [58]. It is generally used for the detection and location of DC line faults. Here, the travelling wave is a step wave at the point of fault which becomes distorted during its propagation along the line. Feature extraction methods based on waveshape and arrival time of the TWs have been proposed to detect and locate faults along the line. The estimated fault distance can be corrected using the second reflected wave front in case the first wave is undetected [59]. TW in conjunction with graph theory [60] and Wavelet Transform (WT) [61] has also been proposed in the literature. Even though TW based fault detecting schemes independent of system voltage have also been proposed [62], the applicability of this method for an LVDC microgrid still needs to be investigated. This is because the distances are small, and hence the reflected waves may not be significant.

4.1.2.7. Communication based FD for grid-connected mode of operation. Communication-assisted methods enable faster fault clearing. Protection schemes in the conventional AC system used power line carrier communication (PLCC), spread-spectrum radio, fibre-optic cable, phone lines and copper pilot wire [63]. Cost and reliability are two critical considerations that govern the choice of the communication medium. Utilising existing infrastructure, such as PLCC, is cost-effective. However, additional measures should be incorporated to enable the transfer of protection signals if a power line is faulted.

Communication-based protection schemes using Intelligent Electronic Devices (IEDs), which trace the current contributions of the main grid, generator and inverter upon the occurrence of a fault, are proposed in literature [64]. Wireless Communication based protection employing differential protection as the default protection and adaptive protection for the critical elements is proposed in [65]. Here, the Signal to Noise Ratio (SNR) is used to detect a communication failure. Communication delays and time synchronization are the major technical difficulties in unit protection schemes. The cost will no longer be a limitation in a Smart Grid scenario where the communication infrastructure will already be inbuilt [66].

4.1.2.8. Energy storage based protection (During loss of communication). The grid contributes a large fault current to the DCMG due to its high capacity. The fault current profile of a DC microgrid operating in islanded mode is significantly lower than that in grid-connected mode [67], and depends on several factors such as location of the fault, the presence of fault-current limiting power electronic converters, type and number of grounding points [68] etc. Therefore, for detecting faults in the islanded mode of operation, either the relays should adaptively change their settings upon islanding detection or some additional mechanism must act during a fault which can drive the current to the original fault level causing relays to trip without the need for changing the relay settings. Communication-assisted protection techniques enable adaptive relaying. However, a suitable backup scheme is required to take over the situation in case of a communication failure.

In AC microgrids, energy-storage based protection methods have been proposed in the literature to play a significant role in enabling fault ride-through in the event of communication failure [69,70],. When a grid-connected DCMG enters into islanded mode the energy storage devices can feed the increased fault current and thereby facilitate relay tripping even with relay settings of grid-connected mode. Such a development with an optimized supercapacitor is discussed in [71], where the non-critical pulsed loads are temporarily disconnected for further reduction in the supercapacitor size.

Table V lists the features of commonly used storage devices for DCMG. By judicious choice and proper control strategy, storage devices can support the protection schemes in the islanded mode of operation. However, protection blinding and over-discharging of batteries during

Table VI
Fault Detection: Signal Processing and Intelligent Techniques.

Methods	Features	Advantages	Disadvantages
Signal processing methods	• Involves digital processing of electrical signals for fault detection	• Accurate analysis is possible	• Large Computational burden
Artificial Neural Networks	• Can be used to group or classify data • Capability to learn from a set of training data	• Fast response times of the order of nanoseconds • Tolerant to degradation or loss of a small portion of the neural network	• Outputs from the neural network cannot be easily reasoned or explained. • Deciding the structure of the network and training set data selection requires human expertise
Fuzzy Logic	• Based on classifying data into crisp data sets, at the same time allowing partial belonging to a set where the degree of belonging is indicated by a membership function	• Fuzziness can replicate the behaviour of the actual system • Useful in systems with too many uncertainties, which are difficult to determine and model	• In some cases, it is difficult to model the fuzziness, so neural networks are clubbed with fuzzy logic
WT based methods	• WT is an excellent tool for extracting transient variations from the current signals [89,96-98]. • Continuous WT can extract more details from a signal but causes heavy computational burden. • Discrete WT reveals relevant information in less computation time and hence is used for protection applications of the power system	• Excellent tool for extracting the transient variations • Suitable for detecting high-impedance faults	• Selection of the mother wavelet function, its order and level of decomposition significantly affects the accuracy and extent of information that can be extracted [46]. • No prominent guidelines are available for choosing the above parameters. • Trade-off between computational burden and maximum feature extraction is required
Machine Learning	• High performance • Easiness of application to complex and non-linear systems	• Ability to detect faults of highly chaotic nature	• Selection of training parameters is crucial in achieving fault discrimination capability. • Generation of the number of training datasets is difficult

faults which in turn contributes to the fault current are impacts of energy storage devices on DC Protection [72]

4.1.2.9. Identifying DC Arc faults. DC arcs are more detrimental to the system as it sustains for a longer duration than an AC arc of the same voltage level. Also, the nature of the arc depends on the arc environment. Being a highly non-linear phenomenon, its detection is challenging. A series arc causes a slight decrease in the current value, which makes it impossible to be detected with traditional overcurrent relays.

Arc fault detection (AFD) is mainly based on feature extraction in time, frequency and time-frequency domains. As the variations in arc current subside during the initial stages of arc occurrence, changes in the circuit current during the initial stage of arc inception can be used for AFD [73]. Arcing results in infrared, optical and high-frequency electromagnetic radiations [74]. Analysis of these emitted waves can give insight into the properties of the arc, which could be used for FD. It is found that the emitted high-frequency electromagnetic radiations depend on the atmospheric pressure, type of conductor material and the current carried [75]. High-frequency spectral pattern analysis with judicious filtering can reveal relevant arc information [76], which is useful for detecting DC arc faults. Techniques using neural networks [77], WT [78–80] and Machine Learning (ML) [81,82] have also been proposed for DC arc detection in order to overcome the difficulties in modelling the arc owing to its highly non-linear nature.

Existing literature states that even with diversified test conditions, including changes in source and loads, the voltage and current patterns are confined within consistent ranges for a DC arc fault. A. Shekhar et al. propose detection of series arcs by measuring the load-side voltage drop and parallel arcs by a change in the current [83]. Measuring the current gradient in time and frequency domains is proposed for series AFD in DCMGs [84].

Due to the randomness and dynamic nature, it is difficult to model the arc with mathematical equations alone. Very few research contributions have been made in developing an arc model for a DC system, such as in reference [85] which proposes a DC arc model suitable for analysing the three types of faults, namely, constant-gap speed, fixed gap distance and accelerated gap faults. The preliminary calculations for estimating the incident energy in a DC arc flash are proposed in [86]. Here a steady-state arc current is assumed so that the resistance part of the circuit impedances alone is considered in the analysis. Literature [87] reviews the characteristic equations and models that have been proposed for analysing the DC arc. It also studies the incident energy estimates for free-burning open-air arcs as well as for arcs occurring in a box such as that within a CB. DC arc models must be able to quantify the arc hazards accurately. While inaccurate estimation leads to safety issues, inflation in predicted risks results in an associated increase in cost [88].

The effects of arc fault on the circuit voltages and currents are random and subside rapidly. Hence its detection based on these parameters is difficult except when accompanied by fast-acting intelligent processing techniques. Alternatively, investigations in optical field variations can lead to promising results for identifying arc faults. As an electric arc is always accompanied by heat, thermal pattern recognition techniques may also lead to successful AFD.

4.1.2.10. Intelligent techniques for FD. Several intelligent techniques based on Artificial Intelligence and WT and ML are being developed to enhance the fastness, accuracy and fault discrimination capabilities. Such methods enable FD using training and learning algorithms, eliminating the need for developing complex mathematical models of the system. Table VI shows the properties of the same. High-resistance faults have always been a matter of concern due to the difficulty in discriminating them from normal current conditions. WT technique is instrumental in this regard. Literature [89] proposes Discrete WT with a medium sampling frequency to detect the fault using resonance in an RLC-based relay. As the proposed fault-detection method is independent of the fault current magnitude, it gives considerable performance for low and high-resistance faults. In an LVDC system, faults with resistances less than 1Ω (usually pole-to-pole faults) are considered low resistance faults, and those with resistances from 1Ω to 25Ω are high resistance faults (usually ground faults). Fault resistances above 25Ω are rare and not severe in LVDC systems; therefore, slower fault detection techniques are sufficient [90].

ML approach used for detecting series faults in High-Temperature Superconducting (HTS) cables is discussed in [91], where the magnetic field profile was analysed for fault identification. ML technique is suitable particularly for the detection of arc faults. As the nature of load affects the voltage and current patterns [92] the training parameters must accommodate variations in load conditions so as to obtain acceptable accuracy levels of FD. Wavelet and ML approach together

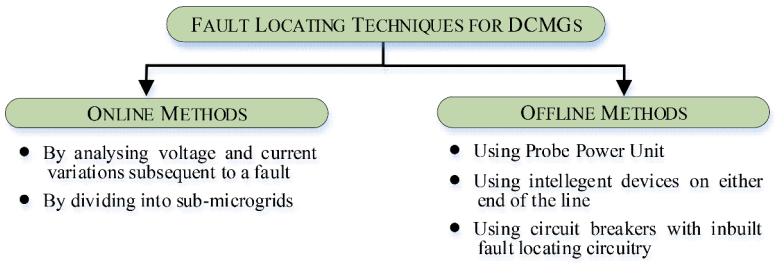


Fig. 4. Classification of Fault Locating Techniques.

also comprehend each other in DC arc FD [93]. Deep Learning Based methods have also been proposed for fault detection in microgrids [94]. Deep Learning methods offer are robust, noise resistant and can perform with 100% accuracy and sensitivity [95].

Combination of model based and local data based techniques is suggested as a future scope of DCMG protection. Methods which account for the SNR and high impedance of faults can improve the reliability of the protection system [99]. Existing literature suggests that in order to ensure efficient, safe and economic operation of the DC grid a coordinated strategy of control and protection could be more effective than considering traditional protection schemes by themselves [100].

4.2. Fault locating techniques

Locating the exact point of occurrence of the fault is important, especially in the case of permanent faults, for fast restoration of supply. Minimizing the location error and FL time are the main objectives of any FL technique. In the case of DC lines, there are two types of FL strategies, as shown in Fig. 4, namely, online and offline [101]. An online FL method operates by analysing the electrical parameters immediately after the fault and before the breaker is tripped. Offline FD methods use an auxiliary device that comes into operation after the CB has cleared the fault. It mainly uses probe current injection followed by analysing the reflected wave through signal processing for accurately locating the fault.

4.2.1. Online methods

4.2.1.1. Based on voltage and current variations. R. Mohanty and A. K. Pradhan proposed a method of locating a fault in a DC Ring Bus microgrid based on the oscillations in the current subsequent to the fault and identifying the faulted section by analysing the transient power variations during the first cycle of the fault [102]. In [103], DC current magnitudes and directions, together with DC voltage levels, are used for locating a fault in an LVDC radial last-mile distribution network. By identifying the current directions at each bus/feeder and classifying it as upstream or downstream, the point to which the fault current is driven is determined, and thereby the fault is located. Fault location can be done without the use of end equipment also. The work in [90] locates a fault by comparing derived and measured values of fault currents. As it uses the Newton-Raphson method within its FL algorithm, it is computationally intensive. However, it offers good accuracy for cases with fault resistance up to 25Ω. Further studies can be carried out to extend this method for locating faults with larger fault resistances.

4.2.1.1. By dividing into sub-microgrids. The concept of dividing the DCMG into Sub-Microgrids (SMGs) has also been proposed in the literature. Fault-locating algorithms are used to isolate the faulty SMG from the rest of the system. M. Monadi et al. in [104] presented such a protection scheme in a radial MVDC microgrid with DC circuit breakers used only at the point of coupling of the VSCs of the Distributed Generators (DGs) and in between SMGs. It proposes a protection scheme with an overcurrent relay at each source/DG, differential protection for each feeder and a Restrictive Signal Generator (RSG) for identifying the fault zone. Once a fault is detected by the overcurrent relay or differential relay, the RSG disconnects it from the rest of the system.

4.2.2. Offline methods: Based on probe power unit (PPU)

J. Park et al. proposed a protection scheme for detecting as well as locating the fault [105]. It is based on overcurrent and differential current techniques and uses an IED installed on either side of each link. Once the CB on either sides trip, a reclose algorithm based on a Power Probe Unit (PPU) comes into operation. A typical PPU-based FL schematic is shown in Fig. 5. It is used to detect the fault location by injecting a probe current into the faulted line using the PPU. Another fault location technique for an LVDC microgrid PPU is presented in [106]. Unlike the approach in [105], it uses an attenuation constant of the damped probe current response. Faults close to the PPU are detected with the help of external resistance and inductance, which corresponds to about 0.5 km length of the cable. The fault distance is calculated using PPU, and the actual fault location is then obtained by subtracting the added length from the calculated fault distance. SNR is also considered in the analysis. In [101] a fault location module is installed at each end of a DC line which computes the fault distance by sampling the discharge current through the line.

Instead of separately installing FL circuitry at either ends of the line, Solid State Circuit Breakers (SSCBs) themselves can be modified with additional in-built accessories to impart FL capability to the breaker [107]. As the circuit elements are shared between both the functions, this approach is more cost-effective than adopting separate FL circuitry. Unlike FD, locating a fault is not subjected to strict time constraints. Therefore offline techniques are sufficient. However, the accuracy of these techniques should not be affected by the status of energy storage elements after the fault.

5. Faults and power electronic converters

As power electronic converters are an indispensable part of a DCMG it is essential to analyse faults with respect to the converters as well. There are two perspectives on analysing the interaction between faults and power electronics converters in the DCMG. One aspect is to analyse how the converter operation would be affected by faults occurring inside and outside the converter. Studying the fault mechanism is vital to ensure the timely protection of the converter before the fault can damage it. The second aspect is to analyse the possibility of using the current

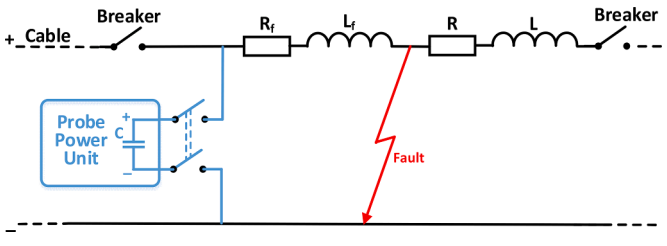


Fig. 5. Locating a fault with PPU.

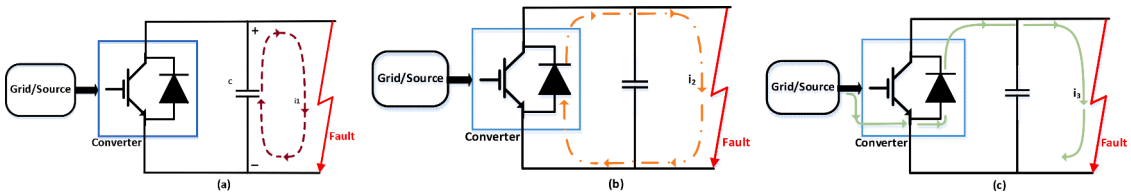


Fig. 6. Fault at the converter output (a) Capacitor discharge phase (b) Diode Freewheeling stage (c) Grid/Source current contribution stage.

limiting capabilities of power converters to reduce the impact of faults whereby the convertors themselves participate in protecting the microgrid.

5.1. Impact of faults on power electronic converters

5.1.1. Fault mechanism for a fault at the converter output

When a fault occurs at the output of a converter, say in a dc cable, the fault mechanism consists of the capacitor discharge phase followed by the diode freewheeling phase, and the source current contribution stage (Fig. 6). The first stage is the capacitor discharge phase, during which the stored energy in the output filter capacitor of the converter discharges into the fault, through the resistance and inductance of the cable up to the fault path.

Once the capacitor has fully discharged, the current then freewheels through the converter diodes. This period is most critical as the fault current is about ten times the nominal current which is high enough to damage the diodes in the converter. Hence faults should be detected and isolated before the converter enters the diode freewheeling stage. Thus the maximum theoretical time available for the protective system to clear the cable fault is the time taken for the completion of the capacitor discharge phase of the converter after the fault. The other alternative way proposed as a potential solution to protect these diodes is to modify the structure of the converters [108].

During the capacitor discharge phase, if R_f, L_f and C are, respectively, the resistance, inductance and capacitance in the path of the fault current i_1, then,

$$\frac{d^2 i_c}{dt^2} + R_f C \frac{di_c}{dt} + \frac{1}{L_f C} i_c = 0 \tag{4}$$

$$damping\ ratio\ \xi = \frac{R_f}{2}\sqrt{\frac{C}{L_f}} \tag{5}$$

The location of the fault (R_f, L_f) decides the shape of the fault current pattern during the capacitor discharge phase, as evident from (5). This concept can be used for detecting and locating the fault.

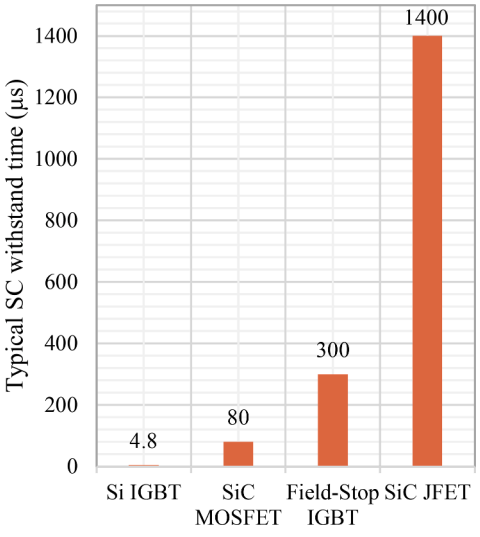


Fig. 7. Typical Short-circuit withstand times of switches.

The behaviour of different types of power electronic converters during faults and the contribution of the converter output capacitor and inductor to the fault current for line-to-line (LL) and line-to-ground (LG) faults is studied in [109]. In [110], a general calculation algorithm for the peak fault current considering fast and slow dynamics is used for FD, which is able to detect the fault during the capacitor discharge phase itself.

5.1.2. Faults occurring within converters

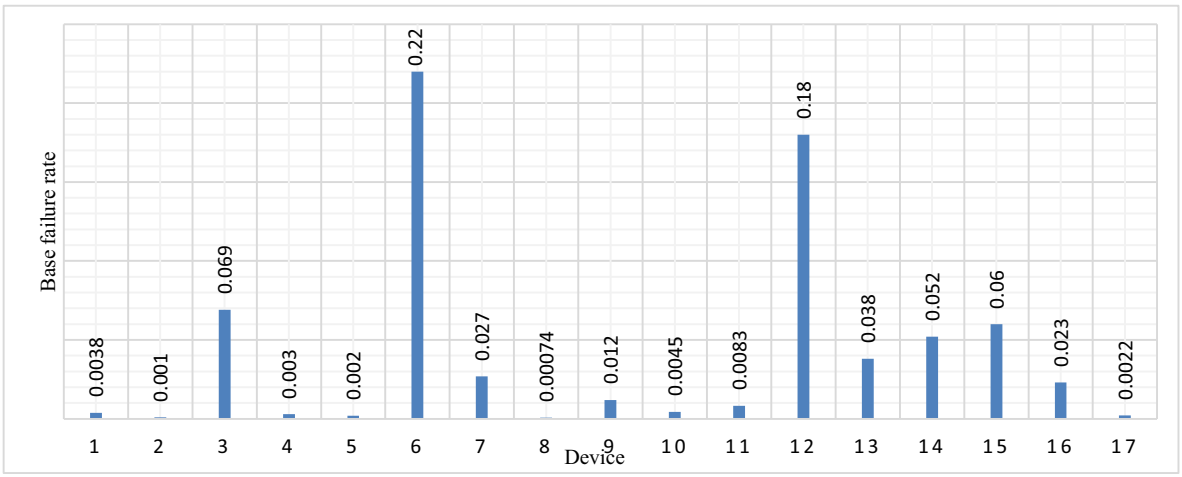
Failure of power converters is an important issue that needs to be addressed. Semiconductor devices, especially power switches, are most prone to faults. The failure of the converter switches can occur as a Short Circuit Fault (SCF) or as an Open Circuit Fault (OCF). SCF is the most severe switch fault as it drives a huge current through the switch. Short-circuit withstand capability of converter switches is a crucial factor in this regard. The SC capability of 1.2 kV Si IGBT is around 4.8 µs which can be enhanced using low-voltage depletion-mode power MOSFET [111]. Increasing the SC withstanding time by 7 to 7.5 times is possible using such additional components but at the cost of increasing the on-state voltage drop. A Silicon Carbide (SiC) JFET of the same voltage rating can withstand SC energy of about 44.6 J/cm^2 before it fails against a SiC MOSFET for which the value is 13.5 J/cm^2 [112]. Typical SC withstand-time of various switching devices are shown in Fig. 7 [111–113].

Even though SC switch faults are detrimental, the converter is usually protected by the gate protection mechanism, usually built into the switch, which withdraws the gating pulses and blocks the operation of the switch upon detecting an SC. Alternatively, a fuse may be connected in series with the switch, which blows off and isolates it in the case of an SC fault. In both cases, the SC problem eventually turns out to be an open circuit fault. An open circuit switch fault is not as severe as an SC fault. However, it affects the operation and leads to stresses in the other elements of the converter, eventually leading to converter failure if left unattended.

In order to foresee the probability of failures, condition monitoring of converter components is crucial. Keeping operating conditions aside, the base failure rates are depicted in Fig. 8 [114] for different power electronic devices numbered from 1 to 17. Apart from semiconductor devices, the health of capacitors in converters also requires attention [115]. However, as capacitor deterioration is a gradual process, offline techniques would be sufficient for its condition monitoring. Challenge also lies in overcoming the difficulty in modelling the thermal behaviour and the damage pattern of converters, which are non-linear [116]. Device reliability and condition monitoring must go hand-in-hand. Exploring the reasons for device failures is a continuous process and will form the basis for condition monitoring over an extended period of time.

5.2. Fault-tolerant converters

Fault-tolerant strategies enable the converters to continue operation with full or reduced capacity, even after the occurrence of faults within the converter. Techniques for fault diagnosis and fault tolerance in DC-DC Converters are developed over a wide range of operating voltages



Diodes-Low Frequency
1. General purpose Diode
2. Switching Diode
3. Fast Recovery Diode
4. Schottky power Diode
5. Avalanche and Zener Diodes

Diodes-High Frequency (Microwave, RF)
6. Silicon impact ionization avalanche transit-time diode (Si IMPATT) <35GHz
7. Schottky Barrier Diode (200MHz to 35GHz)

Transistors-Low Frequency, Bipolar
8. NPN and PNP (<200MHz)

Transistors- Low Frequency, Si FET
9. MOSFET
10. JFET

Transistors-Unijunction
11. All Unijunction Transistors

Transistors-Low Noise, High Frequency, Bipolar
12. Bipolar Microwave RF Transistor

Transistors- High Power, High Frequency, Bipolar
13. Power, Microwave, RF Bipolar transistors (average power ≥1W)

Transistors- High Frequency GaAs FET
14. GaAs low noise Driver and Power FETs (>1Ghz and <10GHz)

Transistors-High Frequency Si FET ,<300mW (average), >400MHz
15. MOSFET
16. JFET

Thyristors-SCRs, TRIACs
17. All Types

Fig. 8. Base failure rates of circuit components.

[117]. The fundamental techniques used for fault-tolerant operation are:

i) Converter Redundancy
ii) Converter Reconfiguration
iii) Using Control Strategies

Table VII shows the switch FD and fault-tolerant strategies proposed in the literature for DC-DC converters. Adding redundancy to converter

Table VII
Fault detection and Fault-tolerant operations in various DC-DC Converters.

Paper	Converter Type	Switching frequency	Fault type	Fault Detection	Detection time	Fault Tolerant operation	Remarks
[120]	Non-isolated DC-DC converters (Boost)	15kHz	Switch Fault OCF, SCF	Yes	Typically 20 μs . Maximum time: within 2 switching periods (for OCF)	No	• Parallelly running primary and backup algorithms. Uses gate signal and inductor current slope direction.
[121]	Non-isolated DC-DC converters (Boost)	Not specified	OCF, SCF	Yes	Typically within 1 switching period. Maximum time: within 2 switching periods	Yes	• Fault tolerance is attained by triggering a bidirectional switch which connects a redundant switch to the circuit, replacing the faulted switch. • DSP development board which includes FPGA chip is used
[122]	Non-isolated DC-DC converters (Boost)	20kHz	OCF, SCF	Yes	Less than 1 switching period	Yes	• Uses Predictive approach • During fault tolerant operation using Pulse Width Modulation (PWM) control the converter is unable to perform the boost action
[123]	Two stage (Buck, Buck-Boost) converter	10kHz	OCF	No	NA	Yes	• Switching frequency changed to 25 kHz in the faulty (reconfigured) mode. Capable of supplying full power post-fault.
[124]	Boost Converter	Not specified	Parametric faults i.e., fault in circuit parameters L and C	Yes	Not Specified	No	• Uses Luenberger observer for FD • Fault identification observer uses adaptive parameter identification technique for locating the faulty component
[125]	Input-parallel output-series Interleaved Boost Converter (IBC)	25kHz	OCF	Yes	Within 2 switching cycles	Yes	• Uses immersion and invariant observer for FD • Two redundant switches enable post-fault reconfiguration for fault tolerant operation

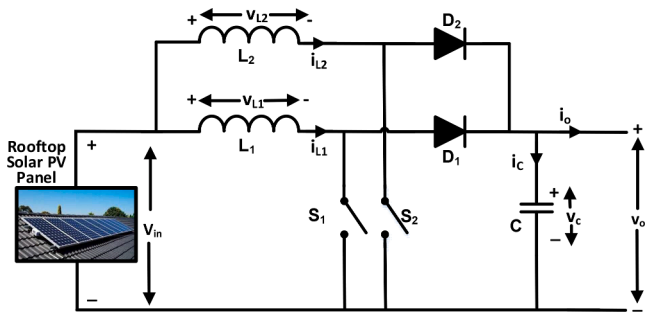


Fig. 9. Circuit diagram of a Two-phase IBC.

Fig. 10. Two-phase IBC waveforms: Gate pulses to Switches (a) S1 and (b) S2, and Inductor currents through (c) L_1 and (d) L_2.

components and reconfiguring the converter topology using control strategies have been proposed in the literature for imparting fault tolerance to converters [118,119].

Interleaved DC-DC converters are gaining popularity due to their inbuilt redundancy, which offers fault tolerance due to the presence of multiple parallel paths. As an example, a 2-phase IBC is shown in Fig. 9 whose triggering pulses and inductor currents are shown in Fig. 10. The phase-shifted triggering of its parallel phases enables ripple reduction in the input and output currents. However, failure of one phase results in a significant increase in the current magnitude and ripple in the healthy phases. Fault-tolerant operation thereby requires re-adjusting the phase difference between the gating signals to ensure symmetrical operation of the remaining healthy phases. Fault diagnosis strategies adopted for interleaved dc-dc converters are detailed in Table VIII.

5.3. *Power electronic converters for limiting the impact of faults*

Power converters themselves can be used to limit the fault current. Such strategies can create a breakthrough in eliminating the need for separate FCLs thereby reducing the cost and size of the system. However, not all power converters have fault-limiting properties. Fully controllable converters such as back-to-back VSCs, DC-DC buck-boost type converters, isolated DC-DC Converters, full bridge Modular Multilevel Converters (MMC) and current-fed dual active bridge have inherent current limiting ability [136]. Amongst these, the first two types are simple, economical, and therefore suited for microgrid applications. MMCs are suitable for high-voltage, high-current applications, and they may not be economical for low-voltage applications such as microgrids. Fault current limiting strategies proposed in the literature for DC-DC converters are listed in Table IX. It must be noted that fault current limiting action of converters imposes challenges in FD which should be addressed separately.

6. Grounding and its impact on FD

The type of grounding has a significant impact on fault detection, protection, and equipment and personnel safety. There are two types of grounding in an electrical network.

i) Equipment grounding
ii) System Grounding

Equipment grounding or earthing refers to the grounding of conducting enclosures of equipment for safety of personnel against electric shock. DC voltages up to 90 V is treated as safe voltage as per industrial practice, but the actual value may be well below 60 V, especially with strict legal interventions and considering the case of personnel having metallic implants in the human body [142].

System grounding refers to connecting a reference point of a current-carrying conductor to the ground. Systems may also be kept ungrounded. DCMG topology can be unipolar or bipolar (Fig. 11) and grounding is done at the positive or negative pole, or at the midpoint of the system.

The different ways in which this ground connection can be made are:

i solid grounding
ii resistance grounding
iii diode grounding
iv thyristor grounding

A comparison of these grounding techniques is listed in Table X [143, 145]. Grounded and ungrounded systems have their own advantages and drawbacks with respect to steady-state faulty current, transient current and the capability to ride through the fault.

Depending upon the nature of the fault, ground fault currents may be constant or intermittent, with long periods which may be fixed or random or in the form of pulses or spikes [146]. In the grounded TN system, earth fault causes SC and hence there is no need for separate earth fault protection. Overcurrent protection alone is sufficient. However, in an ungrounded IT system, an earth fault does not give rise to an SC, and hence overcurrent protection cannot substitute earth fault protection [144–146]. For a grid-connected DCMG, the grounding configuration on the AC side has a considerable impact in selecting the DC side grounding [147,148]. The type of grounding affects the transients experienced by the power electronic converters, especially those forming the interface between AC and DC systems [149]. In a PV-based system, the magnitude of the total leakage current flowing to the ground is decided not only by soil resistivity but also by environmental conditions such as irradiance and ambient temperature, which affects the PV module output [150].

Higher the grounding resistance lesser will be the stray current at the expense of larger possible voltage fluctuations [151]. High Common Mode Voltage (CMV) creates circulating currents between the converters and causes grounding issues. Grounding one pole gives rise to an SC between the poles whenever a fault occurs in the other pole and hence is not advisable. Midpoint grounding helps in reducing the fault current but has the drawback of increased voltage and associated stresses in the healthy pole during a fault [152]. High-resistance mid-point grounding assisted with ground current monitoring can be used in the range of 380–400 V DC for industrial applications [153]. In DC rail systems, due to the low value of rail-to-ground resistance, leakage currents flow between them, which lead to corrosion. The resistance of the leakage current path and the earthing system plays a significant role in deciding the magnitude of the stray current [154]. The choice of grounding method in a DC system depends on several factors such as the grounding in the AC grid side of the network, the voltage level of the DC bus and the converter configurations[148,12].

Table VIII
Switch Fault Diagnosis in Interleaved Converters.

Paper	Type of Converter	Methodology	Time of operation	Remarks
[126]	Three-phase Interleaved Buck Converter	• FD is done based on the harmonic amplitude and phase information of output voltage at the switching frequency • Compares the harmonic amplitude with a threshold for FD • FD is unaffected by changes in load resistance • Phase shift angles of healthy phases are adjusted to 180° when a fault occurs in one branch	FD time = 3.1 to 3.4 ms Time taken to stabilize output voltage = 6 ms (approx.) Total time is about 9.4 ms	• Assumes the parameters in all three branches to be identical except for the phase shift in the gate driving signal of the switches.
[127]	Three-phase IBC	• FD method uses magnitude and phase angle of the harmonic component in input current at switching frequency. Input current is available as it is already measured for MPPT. • DFT is computed in each switching cycle. For an OC switch fault, the input current will have considerable switching-frequency-based harmonic component due to unbalance in the three phasors. • The phase angle of the resultant phasor is used for identifying the faulty branch • Upon identifying the faulted phase, the phase angle of operation of the healthy phases is modified for fault-tolerant operation	FD time = switching time period (Tsw) Reconfiguration time = Tsw Total time = 2Tsw	• The analysis considers that the PV is operating at the maximum power point when OC fault occurs. • All phases are assumed identical.
[128]	Three-phase IBC	• Measures the three branch currents separately as they may not be identical in practice. • The error between actual and predicted values of the inductor current is used for FD in each of the three phases.	Total time for fault tolerant action = 5 ms (approx.)	• Does not assume all phases to be identical
[129]	m-phase IBC	• Analyses switch faults occurring at different instants of a switching cycle. • Inductor voltage is the parameter used for FD and is measured by adding an additional winding on the same core of the main inductor in each phase	FD time < Tsw	• FD duration is independent of CCM or DCM operation but depends on the duty cycle and instant of occurrence of the fault.
[130]	Three-phase IBC	• Proposes a fault-tolerant control strategy aims to reduce the current ripple when one phase is lost due to a fault for a converter connected to a fuel cell in an electric vehicle • The fault-tolerant control consists of modifying the PWM gate control signals according to the faulty leg	Not specified	• FD is not covered in this study
[131]	Multi-phase and multi-switch DC/DC boost converters	• Modifies the switching frequency and duty cycle of the power switches automatically in the event of a switch failure such that the frequency of inductor current and voltage ratio is maintained unaltered.	Not specified	• The redundancy offered by these converters is suited for standalone systems. • Such high redundancy levels may not be essential for microgrid applications with support from the grid/other sources.
[132]	Three-phase IBC	• Three leg currents are operated with Park's transformation and monitored for FD together with the voltage across the switches for detection of faulted switch • Phase shift in PWM signals is modified for fault-tolerant operation • By modifying the Park's transformation based on the number of legs this FD algorithm can further be extended to multiphase and floating IBCs.	Faulty leg detection time = 18 μs.	• Assumes that the converter is operating in CCM and that all the components are ideal and free from stray inductance and capacitance effects. • Also, perfect phase synchronization of all the phases is assumed in the analysis.
[133]	Interleaved DC-DC Converters	• The sign of the DC link current derivative is used for FD. • This information, together with the duty ratio and switching signal commands given to the switches, is used to identify the faulty switch. • It can be extended to buck, boost and buck-boost topologies • Both phase shift and switching frequency correction is employed for fault-tolerant operation	FD ranges from Tsw to 2 Tsw	• Suitable for interleaved topologies buck, boost and buck-boost bidirectional converters • The method is robust to phase control mismatches except in the case of extreme asymmetries, which may affect the fault diagnosis.
[134]	N-phase IBC	• The converter input current is used for fault diagnosis. • The input current value, along with the rising and falling-edge instants of the PWM signals, is used for identifying the faulty switch. • Fault tolerance - phase-shift adjustment along with the correction of the converter switching frequency • Suitable for CCM and DCM operation of the converter	Fault diagnosis takes less than 2Tsw	• All three Phases are assumed identical
[135]	Four-phase interleaved buck converter	• FD is done by measuring the input and output DC voltages and the output current whose phase angle carries sufficient information about the faulted phase. • Fault signature signals were found for each open circuit fault. The difference between the measured total current in magnitude and phase with respect to the predicted current was found, and the difference was analysed to detect the faulted phase.	Fault identification within 2Tsw	• CCM is assumed under steady-state • Fault identification time is independent of duty cycle.

Tsw - switching frequency.

Table IX
Fault Current Limiting Strategies for DC-DC converters.

Reference	Converter Used	Methodology used	Remarks
[137]	DC-DC Converters	A dynamic virtual resistor in series with the converter inductor is used for implementing the non-linear control.	• The method is verified by simulation for Buck, Boost and Buck-Boost type converters and experimentally validated for Boost Converter
[138]	SEPIC	An additional control loop comes into operation for limiting the input current upon detection of a fault	• Assumes that the controller action and subsequent CB tripping would be completed within 2 ms. This may not hold good practically. • Resuming conventional control after ensuring fault clearance would be a more practical approach rather than using a fixed time interval.
[139]	Voltage-sourced DC-DC Converters	The current reference of the primary current control loop is automatically adjusted when a fault is detected in order to limit the inductor current actively.	• Secondary and tertiary control loops, which carry out the voltage drop compensation and power flow control between the microgrid and the main grid, respectively, are ignored in this study. • Also, the capacitance of lines is ignored, and the microgrid is modelled as a series RL model
[140]	Interleaved buck converter	The converters enter current-limiting mode upon the occurrence of a fault and simultaneously coordinate the bus contactors to operate, thereby isolating the fault without the need for communication devices	• Fault path resistance through the cable is assumed to be small compared to the effective impedance of the healthy branches • Not intended to protect against high-impedance faults
[141]	Fully controllable DC-DC converters	Converters de-energize the grid momentarily for less than 10 ms so that the contactors can open and separate the faulty part of the grid	• The proposed method is not suitable for converter topologies with diodes. • Also, assuming a constant arc voltage in the analysis may not practically hold good considering the inherent complex arc behaviour.

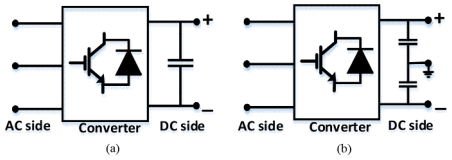


Fig. 11. Supply topologies in DC microgrid (a) Unipolar topology (b) Bipolar topology [144].

7. Fault current limiting and interrupting devices

CBs and FCLs are used to safeguard the system in the event of a fault. While CBs take the responsibility of breaking the current effectively, fault current limiting devices may also be used in conjunction with CBs. With such an arrangement, the FCL acts first limiting the fault current to a lower value which can be interrupted easily by the CB. Thus the responsibility of breaking the current is shared between these two devices. With FCLs, the required rating of CBs can be reduced, which also results in cost savings.

7.1. Fault current limiting devices

FCL is a device that offers low impedance under normal operating conditions so that it does not hinder the power flow and rapidly increases its impedance in the event of a fault, thereby reducing the fault current. An uninterrupting type FCL reduces the fault current to a level that can be safely interrupted by a CB in contrast to an interrupting FCL, which can perform both current limiting and interrupting functions.

Superconductors can be used as FCLs in the power distribution system [155]. Using superconducting FCLs for DCMGs requires optimization between the superconducting resistance and the cost [156]. HTS cables can also effectively limit the SC current with the help of their own self-limiting current characteristic [157,158]. A DC superconducting distribution system itself was proposed by Mitsuho Furuse et al. [159] to replace the AC system.

Non-Superconducting FCLs use power electronic devices such as thyristors and IGBTs. They are of different types, namely series dynamic braking resistor type, Bridge type, Transformer Coupled Bridge Type, and DC link type [160]. Table XI compares the superconducting and non-superconducting FCLs. FCLs are usually used in power systems with higher voltage and current ratings. However, developing cost-effective

Table X
DC Grounding Strategies.

Method	Advantages	Drawbacks	Applications
Ungrounded	• Negligible stray current	• Difficult to detect ground faults • CMV is high due to lack of ground connection	• Implemented in systems where supply to essential loads is to be guaranteed • Used in shipboard systems
Solid Grounding	• Effectively limits CMV • Reduced insulation level requirement due to reduced stress on the insulation of faulty conductor	• Stray current to ground is high • May cause flashes or arc hazards due to high fault current • System stability may be affected	• Used in systems where the circuit impedance is sufficiently high to limit the earth fault current safely
Resistance Grounding	• Moderately limits the stray current • Reduced transient and steady-state fault current • Limits the resonant overvoltages	• CMV is not entirely nullified • Large transient discharge current and steady-state currents under LG faults	• Used in unipolar and bipolar DC networks
Diode Grounding	• The negative bus is connected to ground through a diode when voltage exceeds a certain threshold	• Corrosion due to DC current occurs • Large transient discharge current and steady state currents under LG faults	• Used in DC traction systems
Thyristor grounding	• Connection to ground can be controlled • Under normal operating conditions, the system remains ungrounded and hence stray current losses are minimized • The system is grounded only when the overvoltage setting is exceeded	• Large transient discharge currents and steady-state currents under LG faults	• Used in DC traction systems

Table XI
Comparison of Fault Current Limiters [160].

Types of FCL	Advantages	Disadvantages
Superconducting FCL	• Almost negligible loss during normal operation • FD and operation are automatic • Practically implemented in existing power systems	• Heavier and more prominent in size • High cost • Causes interference with Communication lines
Non-Superconducting FCL	• Usually compact and light in weight • Low Cost • Improves the Dynamic Performance/stability • No interference with communication lines	• Losses during normal operation are not negligibly small • Mostly requires additional circuitry for FD • Practical implementations are only in the budding stages

FCLs for DCMGs can help to achieve improved fault-clearing times.

7.2. Fault current interrupting devices

A crucial aspect of DC protection is the challenge in circuit breaking due to the non-availability of a natural current zero point. Fuses are suitable for LVDC microgrids as the reactance of the system is low. However, faults with large time constants, such as those occurring in motors having large winding inductance, will decrease the interrupting ability of the fuse. In such situations, it would be required to rely on the SC current contribution of the converter output capacitance, which enables the melting of the fuse [161].

Conventional mechanical CBs are not suited for the DCMG environment due to the fast fault-clearing requirements. Also, due to the lack of natural current zero in DC, additional arrangements such as arc chutes may be required so as to cool the arc to facilitate easier quenching. A detailed study of the DC arc behaviour is necessary for the effective design of arc extinguishing methods in mechanical CBs [162]. A fuse model suitable for DC systems for determining the voltage and current variations

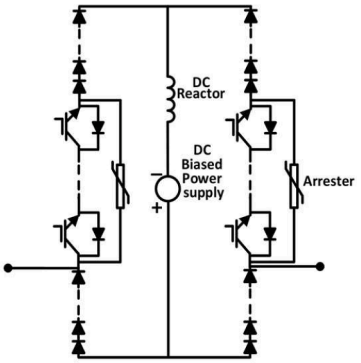


Fig. 12. IGBT Based SSCB with self fault-current limiting capability [168].

Table XIII
Solid State Circuit Breaking Devices - Features.

Device	Capability
Silicon bipolar devices (Thyristors, IGBTs, GTOs, ETOs and IGCTs)	• Blocks voltages from 4.5 to 8.5 kV range and nominal currents up to 3–6 kA.
Reverse-blocking IGCT	• Extremely low on-state voltage - typically 0.9 V at 1000 A.
SiC JFETs	• They are normally-ON JFETs with Blocking voltage ranging from 600-700V
SiC MOSFET	• Blocking voltages upto 3.3kV
SiC Super GTO	• Blocking voltages upto 12kV. 16 times thinner than GTO and offers higher operating frequency. Finds applications in medium and high voltage ranges
GaN FET	• Typical blocking voltage of 650 V (Monolithic bidirectional GaN FET) • The ON-state resistance (typically 200 mΩ) is the lowest of all types of power switches and therefore offers low conduction loss

Table XII
DC Circuit Breaking devices.

Device	Advantages	Disadvantages	Applications
Fuse	• Simple in operation • Economical • Low steady-state losses	• Difficult to control the time to trip • Difficulty in primary-backup coordination • Needs replacement after each operation • Not possible to have remote operation • Interrupting capability may not be sufficient for breaking large currents	• Suitable for low voltage and low current applications
Mechanical CBs	• Capable of handling high current • Low losses and low cost • Higher degree of isolation in the open state	• Reduced lifetime due to contact erosion caused by electric arcing • Slow operation • Not efficient in breaking direct currents	• Suited in DC only for Low voltages • Widely used in AC systems from 230V to EHV range
SSCB	• Low weight and volume • Ultra-high-speed • Produces no arc • Less complex control and high reliability	• Higher switching losses • High cost • Strict detection and timing requirements must be imposed to reverse bias the solid-state switch. • Additional active circuitry is needed to precharge the forced-commutation circuit	• Suitable where fast protection requirements are to be achieved, such as in DC microgrids • Suited for on-board applications, such as aircraft and ships
Z-Source DC circuit breaker	• Fast turn-off • Simple control strategy • Source does not experience the fault current • Creates natural current zero	• Activation requires a large transient current [164] • Modified designs are required to increase the permissible extent of load change that can be distinguished from a fault.	• Suitable for MVDC systems
Hybrid Circuit Breakers	• Losses are minimal • Reduced arcing compared to mechanical circuit breaking	• Complex control is required • Possibility of micro-arcing	• Suitable for MVDC systems

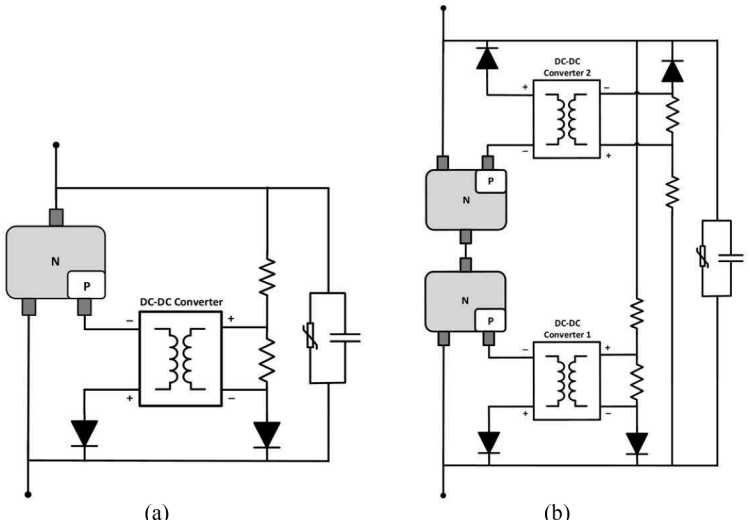


Fig. 13. SiC JFET based SSCB (a) Unidirectional (b) Bidirectional [172].

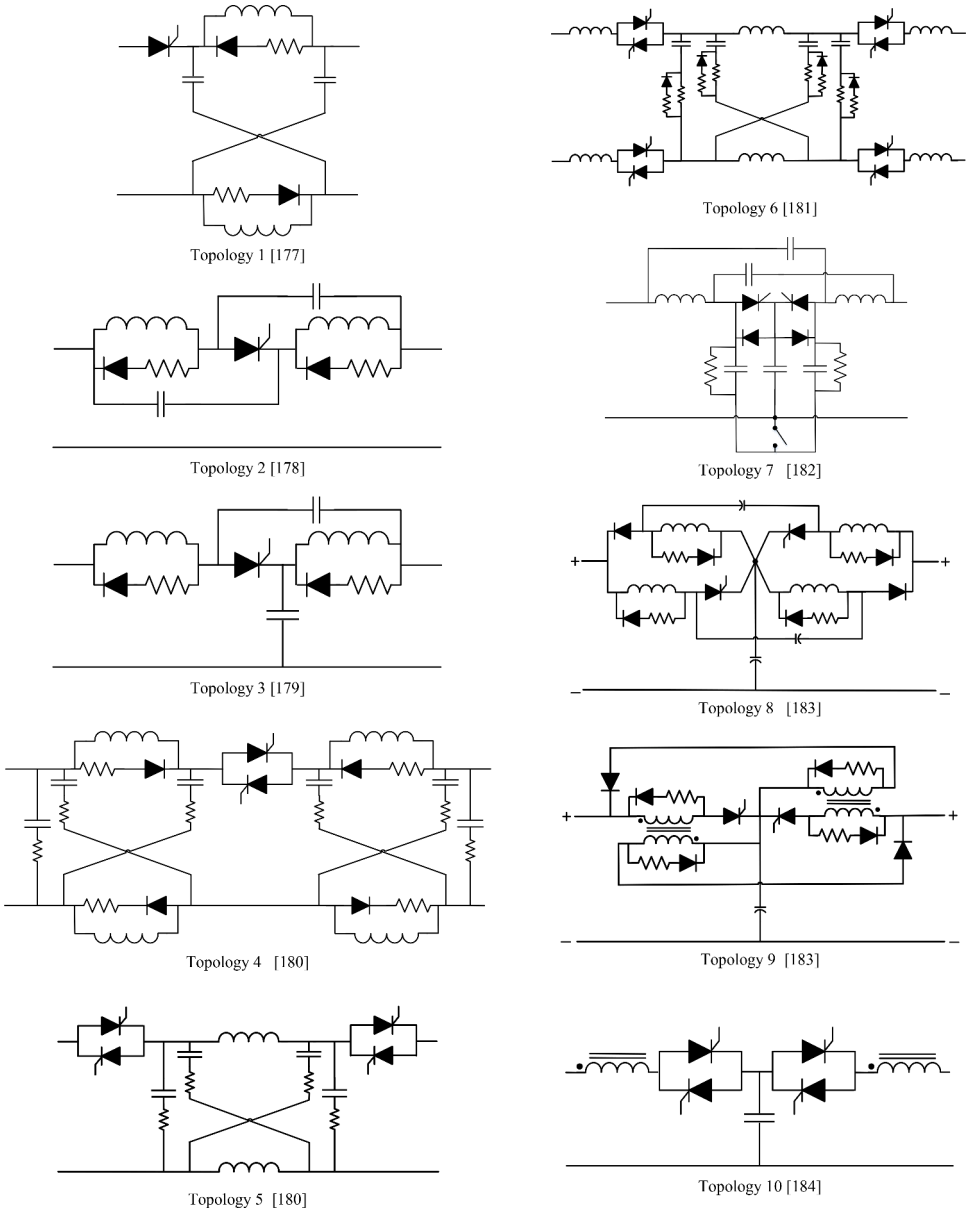


Fig. 14. ZCB Topologies.

during the arcing period is proposed in [163]. It uses a capacitor model with a resistance which is suited for determining the arcing time. However, contact opening techniques may not be effective as the voltage level rises. This led to the development of power electronic circuits for fulfilling the fault limiting and circuit-breaking requirements. Table XII shows the devices that have evolved for DC circuit breaking.

7.2.1. SSCBs

Advancements in material and manufacturing technologies have enhanced the capabilities of power electronic switches as attractive alternatives to conventional mechanical CBs. SSCBs are gaining importance due to their longer lifespan and ability to interrupt DC more effectively as compared to mechanical CBs [165,166].

Different topologies for SSCBs are being developed to suit the DC environment. It is desirable that they fulfil the protection requirements with the minimum number of active and passive elements [167]. Also, these topologies must be designed such that it does not affect the power flow during normal operations or degrade the transient response during power flow shifts as described in the literature [168]. An example of such a type is shown in Fig. 12, where the DC reactor is not directly connected to the line as in the case of typical DC FCL devices.

A critical factor in the design of semiconductor-based CBs is the on-state voltage drop. By suitable choice of doping levels of the various regions in the device, it is found that for an integrated gate commutated thyristor (IGCT) switch rated at 2800 V/ 2400A an on-state voltage drop as low as 1.1 V can be obtained even when 2000A current flows through it [169]. The design of suitable snubber circuits for SSCBs is also important. Discharge-suppressing type snubber topology is found to have better suppression of overvoltage and fault current with reduced cost and size and less impact on the main circuit [170].

Wide band gap semiconductor devices such as SiC and Gallium Nitride (GaN) power transistors, illustrated in Table XIII, are emerging as high-speed switching devices suitable for DC circuit breaking even for high voltage ranges. SSCBs with Silicon carbide MOSFET (SiC MOSFET) and Silicon carbide junction field effect transistor (SiC JFET) based devices (Fig. 13) are evolving as alternatives to silicon-based switches due to their faster switching capability, higher heat-withstanding capacity and higher blocking voltages. GaN switches are also gaining popularity due to their fast switching capability of up to 10 Mhz as compared to 1 Mhz for SiC. Investigations with these devices have been carried out in the literature for 380–400 V DCMGs and are found to have reduced fault clearing times and lesser thermal stresses [165,171-174].

7.2.2. Z-Source circuit breakers (ZCBs)

Conventional SSCBs typically consist of a solid-state switching device and a passive network, usually a pre-charged capacitor, to reverse bias the switching device for forced commutation. Even though this facilitates arcless and fast fault clearing, the solid state switch must be reverse-biased before the fault current rises above the interrupting capability of the breaker. This imposes stringent requirements on FD and timing and also requires an additional circuit for pre-charging the commutation circuit. These limitations have been overcome with the development of ZCB, which has evolved by reconfiguring the Z-source inverter, as it uses natural commutation. Fig. 14 shows different types of ZCBs whose features are listed in Table XIV.

In conventional ZCBs, as the load current flows through the thyristor switch during normal operation, it results in significant losses due to on-state voltage drop across the switch. For an LVDC system, this can be

Table XIV
ZCB Topologies.

Topology listed in Fig. 14.	Bidirectional	Common ground between source and load	Component count	System complexity	Number of components*					Reclosing capability	Remarks
					SCR	Diode	Inductor	Capacitor	Resistor		
Topology 1 [177]	No	No	Low	Simple	1	2	2	2	2	No	• Classical- Crossed Z source topology
Topology 2 [178]	No	Yes	Low	Simple	1	2	2	2	2	No	• Parallel-connected Z-source topology
Topology 3 [179]	No	Yes	Low	Simple	1	2	2	2	2	No	• Series connected Z-source breaker
Topology 4 [180]	Yes	No	High	Complex	2	4	4	6	10	No	• As the conduction path has only one switch, the conduction loss is half that of 'Topology 5' in Fig. 14. • The LC circuits on either side of the SCR introduce a delay in the propagation of fault current, especially when several such breakers are in series.
Topology 5 [180]	Yes	No	Low	Moderate	4	0	2	4	4	No	• Provides bidirectional feature with reduced component count
Topology 6 [181]	Yes	No	High	Complex	8	4	6	4	8	Yes	• Facilitates reclosing
Topology 7 [182]	Yes	Yes	Low	Simple	2	2	2	5	2	No	• Has an additional circuitry with a switch for manual tripping of load current • Disadvantage of this topology is that the fault current reflected to the source is high.
Topology 8 [183]	Yes	Yes	Low	Simple	2	6	4	3	4	No	• This topology significantly reduces the fault current reflected to the source.
Topology 9 [183]	Yes	Yes	Low	Simple	2	6	4	1	4	No	• Uses two sets of coupled inductors • The source does not see the fault. • Power losses are reduced due to the coupled inductors
Topology 10 [184]	Yes	Yes	Low	Simple	4	0	2	1	0	Yes	• Uses a set of coupled inductors • Provides reclosing and rebraking capability

*number includes clamping elements.

Table XV
Key Features of HCBs in the Literature.

Paper	Features of the proposed HCB
[193]	• Current injection type vacuum HCB driven by Thomson actuator • Offers improved dielectric recovery capability of the vacuum interrupter • Under test conditions, a short-circuit breaking time of less than 2.5 ms with 20kA current was achieved • Offers strong current interruption ability, high speed and long electrical life
[194]	• Offers Fault current limiting feature instead of circuit breaking action for temporary faults • Less complex topology with no requirement for an active commutation circuit • Medium speed HCB • For fault interruption, charging of the commutation capacitor takes time and hence not suitable for higher ratings
[195]	• The burden of dissipating the fault energy by the circuit element is reduced as part of the fault energy is returned to the source • Current is interrupted with minimum arcing • Reduction in inductor requirement as the zero crossing of current is achieved by natural oscillations of current using line inductance or smoothing reactor of the converter itself.
[185]	• Has low conduction loss and offers galvanic isolation. • Offers 7–9 ms mechanical action time and less than 8 ms electrical switching time when tested in a 150/380 V and 15A prototype
[196]	• Uses a switching mode transient commutation current injector circuit instead of a series load commutation switch to reduce the conduction power loss. • The additional current injection circuit enables dynamic tracking of the fault current at high speeds (within 30 μs) • More suited for MVDC and HVDC applications

overcome by using an ultra-fast, very low-resistance mechanical switch which replaces the thyristor switch [175]. With the knowledge of the system parameters, the minimum detectable fault current and minimum ramp rate can be suitably adjusted to eliminate false tripping. The inability of a conventional ZCB, to respond to faults of slower dynamics is overcome by including steady-state overload protection in addition to transient fault protection. A series connected ZCB design presented in [176] can tolerate a more considerable step change in load compared to its previous counterparts.

The main drawback of conventional ZCBs is the unidirectional conduction capability which restricts its areas of application. Bidirectional ZCBs have been proposed in the literature to overcome the limitations of their unidirectional counterpart, especially in DCMG applications [182], but such topologies are limited in number. Enhanced topologies and modified ground/ return paths for reducing or nullifying the fault current reflected to the source have also been developed [179,183].

7.2.3. Hybrid circuit breakers (HCBs)

The concept of HCBs was first introduced in the AC system [185]. HCBs were developed to combine the merits of mechanical and solid-state circuit breakers and eliminate the drawbacks of both types. Studying different semiconductor devices, such as IGBT, injection-enhanced gate transistor (IEGT) and IGCT, for their suitability in hybrid DC CBs, is essential in developing enhanced designs [186]. As stated in literature [187], IGCT-based HCBs for DC systems was first reported in [188] in which a considerable reduction in contact opening time, of less than 350μs, was achieved with a 4-kA/1.5-kV operating condition in a test system. While IGBT and IEGT have better turn-off ability, IGCT is cost-effective [189] and offers the lowest on-state voltage of the lot. Conduction ability is highest for IEGT. Voltage-controlled IGBT/IEGT and current-controlled IGCT offers good robustness. As these features directly impact the circuit braking process, a suitable trade-off should be made for the device selection.

Table XV lists the key features of HCBs proposed in recent literature for DC systems. Significant work on HCBs is still in progress, such as the use of superconducting materials for breaker design [190], coupled-inductor circuits for lossless breaking [191], and the development of breakers suited for traction and industry [21]. The Vacuum Arc commutation characteristic in a DC HCB is investigated in [192]. Successful arc commutation depends on the current, arc voltage, on-state resistance of its thyristors, and the externally applied transverse magnetic field.

An undesirable phenomenon in DC HCBs is micro-arcing which occurs during the commutation of current from the separating contacts to the power electronic switches. It causes erosion of the contacts, with pips and crater formations, and occurs for resistive and inductive loads. The duration of micro-arcing can be reduced by lowering the resistance and inductance values of the breaker [197]. The proper choice of material for the switch contacts for reducing micro-arcing can be investigated as an extension of this study.

8. Conclusion

This paper throws light into the research interests in the field of protection of DCMGs. Due to the pattern of DC fault current, fault detecting time as low as 5 ms is desirable in DC circuit breaking as compared to about 20 ms in AC. Reviewing existing literature reveals that mimicking the conventional protection schemes used in the AC system is not sufficient for protection in a DCMG. In this context, there is wide scope for research in the following areas:

- Analysis of DC fault current pattern for identifying protection strategies suited uniquely for DCMGs.
- Development of FD techniques for high resistance faults together with development of back-up protection schemes.
- Strategies to facilitate effective protection during loss of communication
- Set up co-ordinated protection and control so that system performance and reliability are dealt hand-in-hand
- Development of strategies for condition monitoring of power electronic converters.
- Design of fault-tolerant and fault current limiting converters.
- Analysing the impact of converter operation on the protection schemes in a DCMG.
- Development of an accurate model for the DC arc for fast detection of DC arc faults
- Development of fast acting and economic circuit breaking devices with low on-state voltage drop for DCMG system.
- Standardisation of grounding techniques for DCMGs.
- Analysis and standardization of DC transient voltage limits for DCMGs.

No advancement in the electrical power system can flourish without a parallel advancement in its protection system. It is, therefore, the need of the hour to develop foolproof and cost-effective solutions for fulfilling the complete protection requirements of the DCMG. Only then can the true potential of DCMG systems unfold.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

All data used have been referenced in the paper.

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