Design and Analysis of QCA based Area Efficient 4x8 SRAM Array

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***Abstract*—Static Random-Access Memories (SRAM) is the popular choice for memory. As the memory requirement increases, so does the power consumption. Quantum-dot Cellular Automata (QCA) is the technology for low energy, compact and faster digital circuits. The paper aims to design, implementation and performance analysis of compact 4x8 bit SRAM array. First, basic gates are realized in QCA and then one-bit memory cell is constructed. The optimized 4x8 bit SRAM is realized and simulated using QCADesigner with QCA cells of 18nm cell width and height. The proposed QCA memory cell has a cell count of 41 QCA cells; this is very less compared to QCA memory cells in literature. The proposed 4x8 bit SRAM array has a total QCA cell count of 3823, with one clock cycle delay for read/write operation, occupies area of 4.1 µm² and energy dissipation is 1.32 eV, as measured using QCADesigner-E.**

Keywords— CMOS · Memory cell · QCA · SRAM

I. Introduction

Portable and wireless devices are power-hungry as they access extensive amount of memory and process large amount of data. Due to technology scaling in these devices, speed is important [1, 11]. The performance of these devices is limited by interconnection of bandwidth between the chips. In Digital systems, for example, DSPs, microprocessors call for low power design. The low power activity has been the basic need, predominantly focusing on expanding the battery life, to decrease the general cost of over the top cooling and furthermore to maintain a strategic distance from failures which happen because of hot spots. Due to the advancements in technology, portable and wireless communication devices require huge memory. Traditionally, SRAMs are used as memory elements in portable and wireless devices.

SRAM is a variant of memory which stores each bit using bi-stable latching. In the conventional SRAMs, when power is not provided to the memory, data is misplaced and consumption of power turns out to be another major issue. CMOS technology is widely used for SRAM, but often has drawbacks, and upcoming technologies have to overcome them.

SRAM has an important role to play with regard to power consumption and area occupied in a wide range of devices. As the memory size increases, the area and power consumption also increases. As a result, low power and small area designs have become inevitable parts of today's devices and hence an eminent factor in the advancement of VLSI technology. Few low power technologies are Reversible logic [3], Adiabatic logic, and QCA technology [1, 2]. The switching activities which reduce the overall power by providing stored energy back to the supply, thereby making the total heat or energy in the system remains constant. Although adiabatic logic reduces power, it occupies area and delay is more.

QCA provides a solution which is based out of Nano-scale and establishes itself as a latest method of information transfer and computation [15]. QCA is preferred for the implementation of memory circuits.

The aim of this paper is to design, implement, simulate and analyze SRAM array using QCA technology. The simulations of the circuits are performed using Coherence vector and Bi-stable simulation engines in the QCADesigner. The energy dissipation of the QCA cells is analyzed using QCADesigner-E.

Organization of the paper is as follows: A brief literature review of the related works is discussed in section 2, following which basic concepts of QCA are explained in section 3. Section 4 discusses the design principles in QCA in order to implement the SRAM. Section 5 illustrates the simulation results obtained by implementing 4x8 SRAM. Conclusions derived are listed in section 6 with future scope.

II. Literature Review

Due to the wide range of portable devices, low power VLSI design in recent years has been attracting a lot of interest. Kianpour [1] proposed the fact that kT × ln2 J of energy is to be dissipated as heat for loss of information of every bit which occurs for every logical computation that are not reversible, where k being the Boltzmann's constant and T being the temperature in k at which operations of system occur.

The outline of parallel QCA memory is presented in [4], the clocking zones are independent of the memory size and is being shared amongst all the cells in a column. The R/W' control circuit was very simple and needs two extra clock signals. In the line-based architecture, the storage is achieved when we move the data back and forth in a QCA line. These memory architecture designs needs additional three zones for storage.

The synchronization of line-based memory architecture has been improved in [5] using dual phase clocking signal and the clock zone required for data storage was reduced to two. The dual phase clocking signal was excited using single clock generator. Tile-based memory architecture has been discussed in [6], it contains three tiles and placed in the order of input tile, output tile and memory tile to store one-bit information. The number of memory tiles can be extended between input and output tiles according to the storage of N-bit information in which the input tile can be used to select incoming input data to the memory loop. The memory cell is designed using 74 QCA cells.

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A set of equally sized tiles together forms complex circuits in the square formalism. The QCA memory can be designed using square formalism [7]. The main advantage of this technique is simple geometric layout and disadvantage of this methodology is lower density and spatial redundancy and additional control circuit. The H-memory architecture has been introduced in [8], it uses a square shaped spiral structure which loops back for data storing. It is a binary tree structure and the additional control circuit is provided at every node to perform read/write operation. The number of clocking zones does not increase even after adding extra layers in order to increase the word size of the every memory cell.

The process of how a new generation technology i.e., the QCA technology is replacing the old conventional CMOS has been discussed in [12]. The work discusses the efficient implementation of the SRAM cells and their analysis in terms of delay, area, and power. The efficient utilization of the wide range read/write memory array has also been discussed.

Literature review infers that QCA technology has an advantage of being low energy that occupies very small area, thus the QCA technology is an alternative realization of SRAM when compared other (CMOS) technologies.

III. Basics of QCA Technology

QCA is identified as one of the upcoming recent nanotechnologies and is expected to be promising by being able to achieve, high switching speed, low power consumption and lesser area. QCA computations are based on electrostatic interaction amongst QCA cells [4]. The fundamental QCA cell is for the most part is a four dot cell.

In Fig. 1, an unoccupied dot is represented with a white circle and occupied dot is occupied with a black circle. Due to the electrostatic interaction between the electrons in the QCA cell, they generally occupy diagonally opposite positions which forms two charge distributions or two logical states. The two states are perceptible and they can be utilized to change the logical levels '1' and '0' of a specific bit [7].

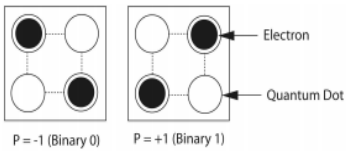

Fig. 1: QCA cell representation

The QCA logics basic structure of consists of 3-input majority voter MV, output of MV is represented as:

$$MV(A, B, C) = A \cdot B + B \cdot C + A \cdot C \qquad (1)$$

Fig. 2 represents the majority gate in QCA. It is used as a part of logical functions. A 2-bit AND is realized using 3-bit MV is shown in Fig. 3. Logical OR gate is realized as MV(A,B,1) and logical AND as MV(A,B,0) [9].

Four Quantum cells situated at the edges of the square cell forms a QCA cell. In every cell there are two electrons that can burrow between neighboring dots [8].

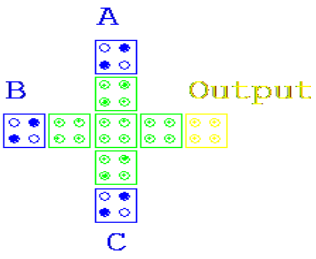

Fig. 2: QCA Majority Gate

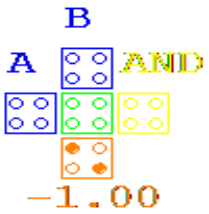

Fig. 3: QCA AND gate

A QCA wire and the state of the cells in various clock zones are represented as clock-1, clock-2, clock-3 and clock-4 respectively. These stages are named as switch, hold, release and relax as shown in Fig. 4. In switch period, the barrier potentials will be low and cells are unpolarized. Amid switch stage, the QCA cells get polarized and potential barriers turn out to be high; in this stage the computation is done. After the hold stage, potential barriers are high. In release stage, QCA cells get unpolarized as potential barriers are low. In the relax stage, QCA cells still remain unpolarized as the boundaries stay low.

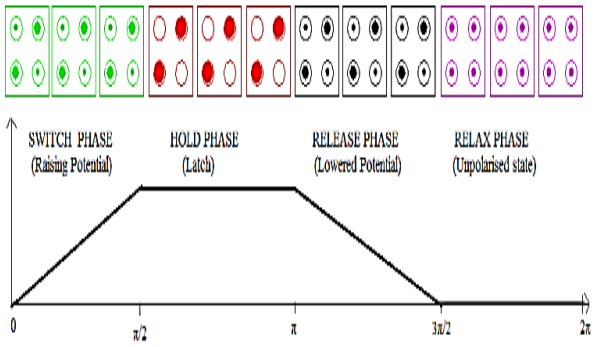

Fig. 4: Polarization of QCA Cells for various clocking zones [9].

A well-known QCA inverter is one in which the information can be applied to one of the ends and transformed yield can be obtained at opposite end, as depicted in Fig. 5. The input wire would then be part into two diverse parallel wires and as a result of columbic interaction it polarizes the cell.

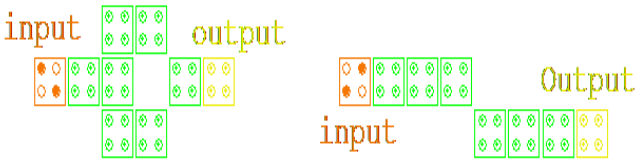

Fig. 5: (a) QCA NOT gate **(b)** Simple QCA NOT gate

IV. Design and Implementation of 4x8 SRAM Array

A 4x8 bit SRAM consists of 2:4 decoders, 4x8 memory array and 8 bi-directional buffers for data transfer. The memory array is formed by replicating 1-bit memory cell in a hierarchical approach. One-bit memory cell is replicated to form an 8-bit memory array. Thus formed row is replicated to form 4 rows, each of 8-bit. This forms the 4x8 memory array of SRAM as shown in Fig. 6.

The decoder is connected to the memory array as shown in Fig. 6. Each of the output lines of the address decoder enables the corresponding row of 8-bit memory. If read mode is empowered, the information in the cell is transported to output. The R/W' decides mode of the cell. The 4x8 bit SRAM is designed with QCA cells of 18nm cell width and cell height using QCADesigner.

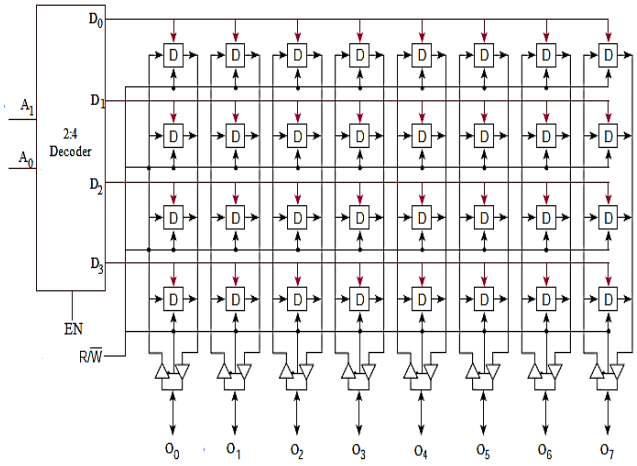

Fig. 6: Block Diagram of 4x8 bit SRAM

A. Memory Cell

One-bit memory cell can be used as basic building block in the construction of the 4x8 memory array. Using the bottom-up approach, 2 cell memory array, 8 cell memory array and hence the 4x8 cell memory array are constructed and simulated on the QCADesigner.

Fig. 7 illustrates the schematic logic diagram of a memory cell. Output gets enabled when EN is equal to '1' while output becomes equal to '0', when EN is equal to '0'. If R/W' = '0' WRITE is selected and then value of D is stored in memory. The READ is selected and stored bit is put on the output when R/W' = '1'.

Proposed memory cell implemented in QCADesigner is shown in Fig. 8, it has a cell count of 41 QCA cells as compared to memory cell proposed in [1] which has 52 QCA cells.

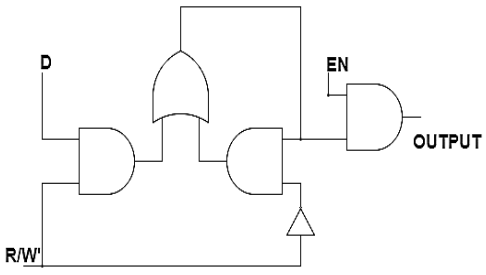

Fig. 7: Logic diagram of memory cell

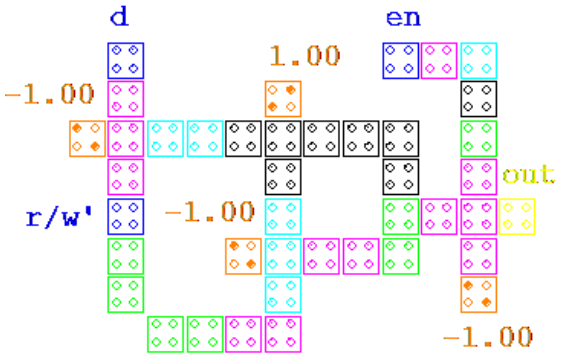

Fig. 8: Memory cell in QCADesigner

In the proposed memory cell there is a reduction of 21.15 % cell count in each memory cell. The memory cell has added functionality of enabling the memory cell and read/write pin along with data input as compared to QCA SRAM memory loop in [8].

B. Decoder

The QCA cell of 2:4 decoder is illustrated in Fig. 9. The four Majority voter (MV) gates configured as four AND gates. The signals A and B are the inputs to the gates and all the possible input configurations are realized using inverters. D_0, D_1, D_2 and D_3 are the corresponding outputs of the decoder. Fig. 10 represents proposed QCA based 2:4 decoder implemented in QCADesigner.

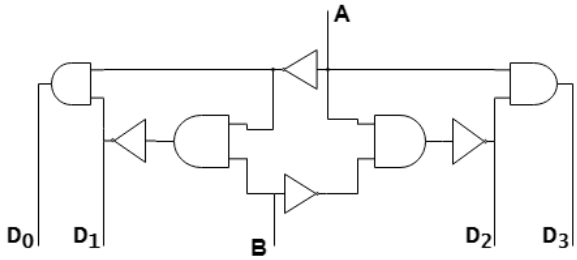

Fig. 9: Logic diagram of 2:4 decoder

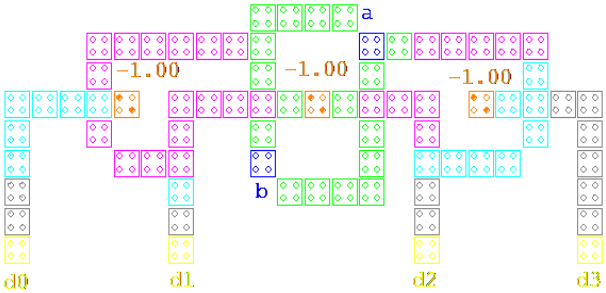

Fig. 10: Proposed 2:4 Decoder in QCADesigner

C. 4x8 SRAM Array

The 4x8 SRAM array consists of 2:4 decoder and 4x8 memory arrays. In CMOS logic design, bi-directional buffers are used for data transfer. In the proposed design two separate data lines, one for data input and other for data output are associated with the memory array. One-bit memory cell is replicated eight times to form a row of memory array which is then replicated four times, hence forming the 4x8 bit memory array. Thus formed memory

array is integrated with the 2:4 address decoder. The control logic consists of the R/W'. Data is fed to SRAM through input lines I_0 to I_7. The output is read out through O_0 to O_7 lines. Fig. 11 illustrates the QCA implementation of 4x8 SRAM memory array using QCADesigner.

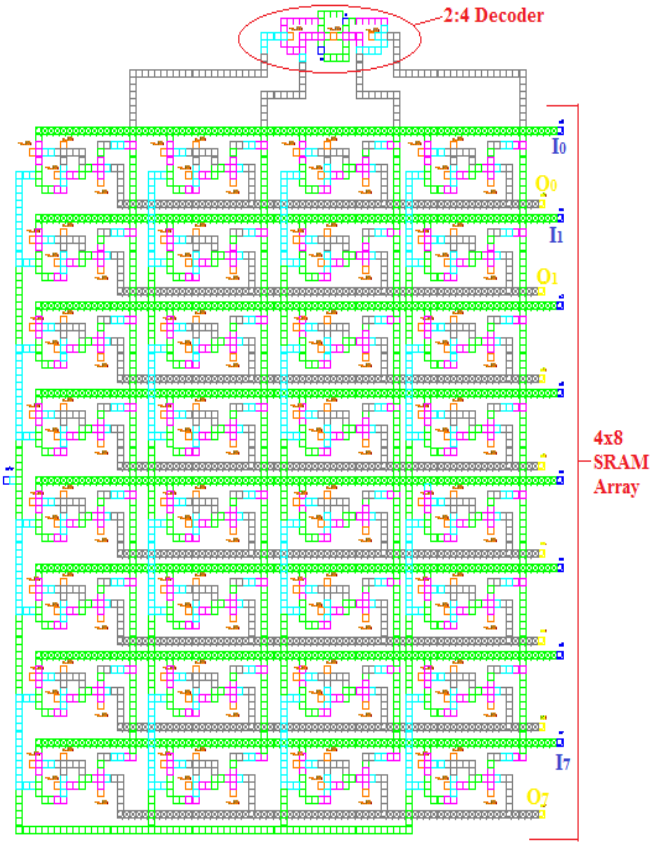

Fig. 11: 4x8 Bit SRAM in QCADesigner

V. Results and Discussion

CAD tool, QCADesigner V2.0.3 is designed for the purpose of QCA circuit design and simulation. QCADesigner is be used for simulation of the proposed SRAM design. QCADesigner tool provides individual the platform to layout and verifies the QCA circuits that the individual chooses. Coherence Vector and Bistable simulation engine are the two simulators used in the QCADesigner for the simulation of the designs. One-bit memory cell, 2:4 decoder, 4x8 bit SRAM is simulated using the QCADesigner and energy dissipated is computed.

One-bit cell is the elementary block for the SRAM. The One-bit memory cell illustrated in Fig. 8 is simulated using QCADesigner tool. The output waveforms are shown in the Fig. 12. Higher bit order memory array are formed by replicating the 1-bit memory cell.

A 2:4 decoder implemented in QCADesigner as shown in Fig. 10 is simulated using Bistable simulation engine. The decoder outputs are D_0, D_1, D_2 and D_3. Fig. 13 depicts that there are four possible combinations for 2-bit input, corresponding to each combination one of the output lines is activated. The decoder outputs are used as enable pins to the memory array.

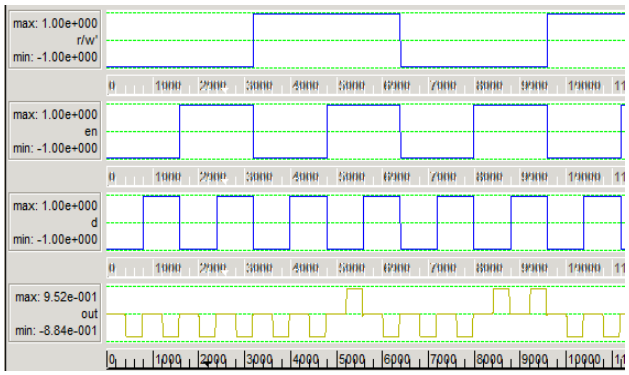

Fig. 12: Output of 1-bit Memory Cell

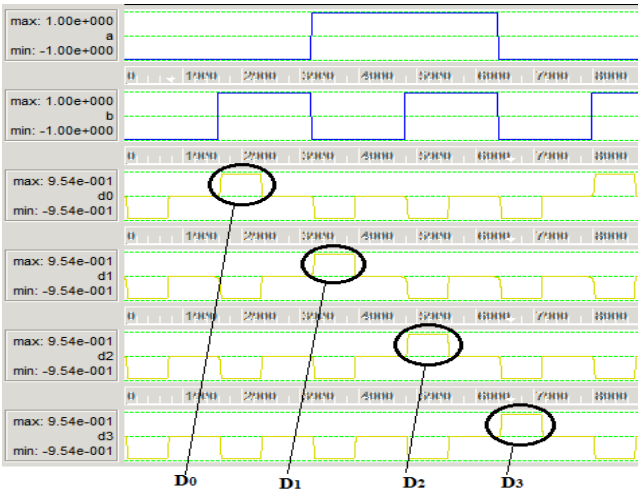

Fig. 13: Snapshot of Output of 2:4 Decoder

A. 4x8 SRAM Array

One-bit memory cell is replicated 32 times and memory array of the SRAM is formed. Thus formed memory array is integrated with the 2:4 decoder. The control logic consists of the R/W' and enable. The R/W' controls the read and write action of the memory array. The four outputs of the decoder, control enable action of the corresponding rows of memory array. Data is applied to the SRAM through input lines I_0 to I_7. The output is taken through O_0 to O_7 lines. The 4x8 bit SRAM presented in the Fig. 11 is simulated in the QCADesigner.

Fig. 14 depicts the output of 4x8 SRAM array. The inputs are represented in blue color and the outputs in yellow color. The input to the decoder is the address of the 8-bit memory array. The output of the address decoder enables the corresponding 8-bit memory array. The 8-bit data gets written into memory cell when R/W' is low. Fig. 14 illustrates the read operation of SRAM when both enable (EN) and R/W' is '1'. Input data is provided as input using Coherence vector table in QCADesigner. Total area of QCA based 4x8 SRAM layout is retrieved from the QCADesigner. Proposed QCA based one-bit memory cell is compared with other QCA memory cells w.r.t. cell count, area, and delay (read/write) and listed in Table I.

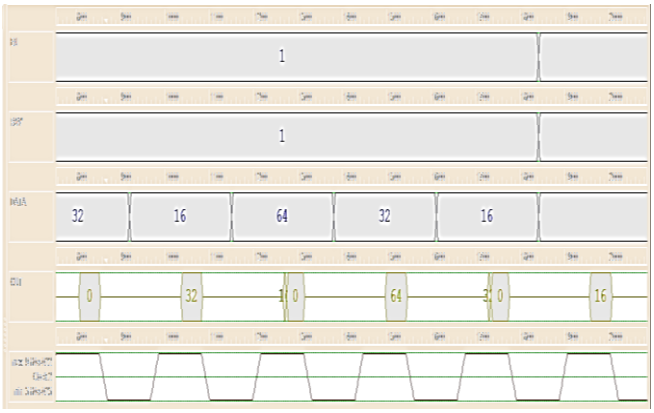

Fig. 14: Output of 4x8 Bit SRAM

Table I: Comparison of QCA memory cells

QCA Memory Cell	Cell Count	Area (μm²)	Delay (clock cycles)
QCA memory cell [2]	158	0.16	2
QCA memory cell [11]	103	0.13	1.75
QCA RAM cell [10]	92	0.10	2
QCA RAM cell [13]	88	0.10	1.5
QCA RAM cell [5]	75	0.09	1.5
QCA memory cell [1]	52	0.09	1.5
Proposed memory cell	**41**	**0.07**	**1**

The proposed memory cell is best in terms of cell count, area, and clock cycles. Proposed memory cell has a QCA cell count of 41 cells and area of 0.07 μm², which in minimum among the cells listed in the Table I. Also clock cycles required is one. Hence, when the proposed cell is used in SRAM overall cell count and the total area of the SRAM minimizes.

The area occupied by each of the individual components and the final SRAM design are tabulated in Table II. The cell count of proposed SRAM is 3823 QCA cells and has a total area of 4.1 μm².

Resizing is an added option in the QCADesigner to downsize the circuits that are larger than the substrate. Resizing has to be done only after the finalization of QCA circuits.

Table II: Area occupied by the sub-components of SRAM

Memory Component	Area (μm^2)
1-bit memory cell	0.07
8-bit memory array	0.74
4x8 bit memory array	3.52
2:4 decoder	0.11
4x8 bit SRAM	4.10

B. Energy Analysis of 4x8 SRAM Array

Energy dissipation of the QCA circuits is analysed in QCADesigner-E [9]. It is an extension to the existing layout designer tool, QCADesigner. The QCA circuits created in QCADesigner are compatible with the QCADesigner-E. Dissipated energy is obtained from the coherence vector energy simulation engine. Snapshot of memory cell with the energy value displayed in the bottom of the QCADesigner-E as shown in Fig. 15. The energy dissipated is expressed in terms of eV. Energy dissipated by various sub-systems is tabulated in Table III. The energy and equivalent power dissipated by SRAM is approximately the sum of all its sub-systems and interconnects.

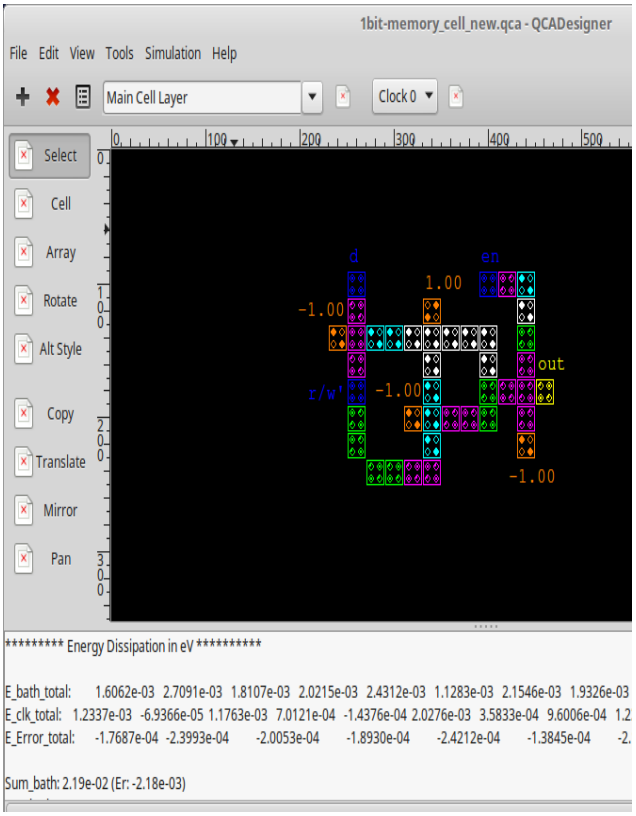

Fig. 15: Snapshot of memory cell energy analysis in QCADesigner-E

Table III: Analysis of the sub-circuits of SRAM using QCADesigner-E

QCA Component	Energy Dissipated (meV)
Memory cell	21.9
2:4 decoder	238
4x8 SRAM	1320

VI. CONCLUSIONS

Low power SRAMs plays an important role in a wide range of electronic devices and reduces the overall power consumption of the devices. QCA has emerged as a trend to substitute CMOS in nanotechnology field. The proposed 4x8 bit SRAM is designed using the hierarchical approach and implemented in QCADesigner. The proposed SRAM occupies an area of 4.1 μm^2 and has a cell count of 3823 QCA cells. Energy analysis of QCA circuits is assessed using QCADesigner-E. The total energy dissipated by

SRAM is 1.32eV. QCA reveals to be a strong challenger to complement CMOS technology in digital integrated circuits, in near future. To realize and simulate complex circuits, QCADesigner CAD tool needs to be improved. Proposed memory cell is designed on only one-bit storage. Hence, there is a possibility for designing 8-bit memory on a single cell.

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