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TECHNICAL PAPER

An efficient energy harvesting circuit for batteryless IoT devices

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Abstract
A new energy harvesting circuit for battery-less IoT beacon tags is developed herein to maximize power conversion efficiency as well as high throughput power with a wide input–output range. This design energy harvest (EH) circuit incorporates a charge pump (CP) with shoot-through current suppression, a body selector circuit, a maximum power point tracking circuit (MPPT), a timing control circuit, a hysteresis control circuit and a low dropout regulator. Also in this MPPT circuit is a gated clock tuned in a self-adaptive fashion to match the input impedance of the EH circuit to the output impedance of the photovoltaic (PV) panel, thus achieving successfully maximum power point. The circuit is implemented in an integrated chip in an area of 1.2 mm^2 via the TSMC 0.18 process. Experiments on the chip are conducted and the results show that the input voltage range is allowed from 0.55 to 1.7 V to effectively harvest the solar power from a flexible dye-sensitized solar cell. The achieved peak power conversion efficiency (PCE) is 77% at the input power of 52 μW. For a wide range of lighting luminance (300–1300 lx,) the achieved average PCE is more than 70%. The achieved wide input–output range and the maximum throughput power of 200 μW is much larger than others reported, while the 77% of PCE is close to that best power conversion efficiency reported.

1 Introduction

The growth of the complementary metal oxide semiconductor (CMOS) industry is nowadays driven significantly by the mobile and internet of things (IoT) devices (Goerlich 2016). Based on reports, the market of IoT beacon tag will exceed 11 trillion US dollars in 2025. Figure 1a shows the block diagram of the IoT beacon tag, which incorporates a solar cell, an energy harvesting circuit, an optical receiver, and a radio-frequency transceiver module. Figure 1b shows a typical production management system that uses the IoT beacon tags for position tracking of workpieces in a factory with assistance from a wireless sensor network (WSN) (Yao et al. 2013). However, for long-hour operations, the limited battery power of the IoT beacon tag is one of the major issues. By integrating the energy harvesting (EH) circuit with the power management unit of the IoT beacon tag, battery issues can be eased. The function of the EH circuit is to collect the energy from the ambient energy source and then provide a stable supply voltage to other modules.

Piezoelectrics (Gasnier et al. 2014), thermoelectrics (Carreon-Bautista et al. 2014), radio-frequencies (Reinisch et al. 2011), and photovoltaics (Esram and Chapman 2007) are the seen ambient renewable energy resources. However, the availability and sustainability of these ambient energy resources is highly uncertain. Among all the ambient energy sources, the photovoltaic (PV) panel is one of the promising energy sources due to its relative advantages in availability, sustainability and the level of energy can be harvested. However, there are issues with PV energy source, such as that the output power depends on the environmental lighting intensity, and whether the harvested power can be converted efficiently to a stable bias voltage to drive loads. Thus, an efficient EH circuit is required to provide a stable and adequate drive voltage to the sub-circuits of the IoT beacon tag. Inductive and capacitive architectures are the two widely used for energy harvesters. Low output ripple, low leakage current, high voltage conversion ratio, and the high power conversion efficiency are the main advantage of the inductive architecture (Carreon-Bautista et al. 2014). However, the inductive architecture is difficult to be integrated with other sub- circuits and/or systems due to a large-sized external inductor in the circuit. Considering to minimize the overall

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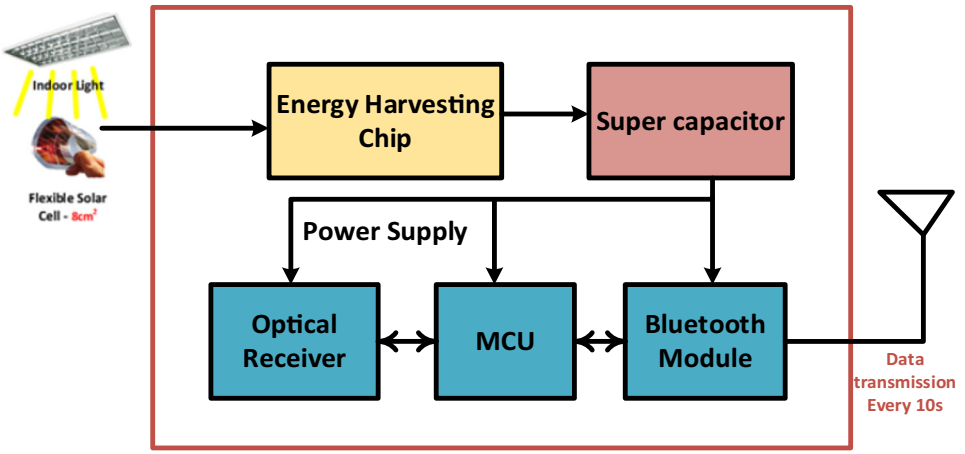
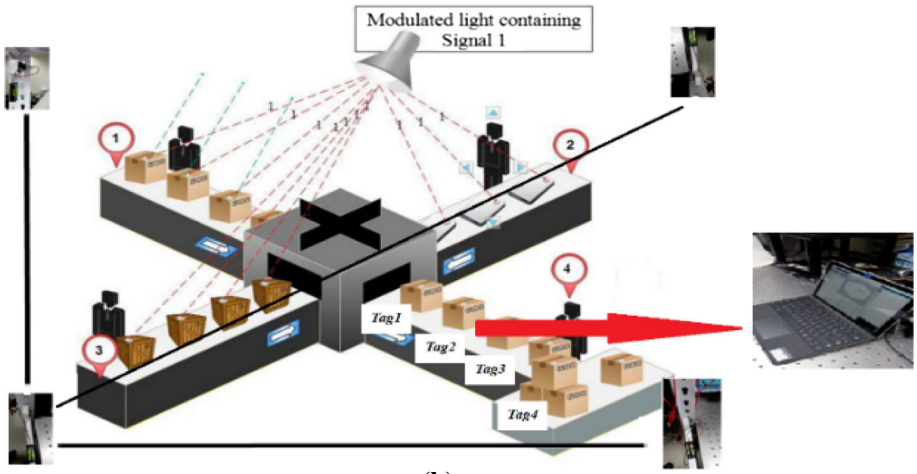


(a)



(b)

Fig. 1 The proposed battery-less IoT beacon tag, **a** the circuit system in sub-circuit blocks, **b** a typical production management system that uses the IoT beacon tags for position tracking of workpieces in a factory with assistance from a wireless sensor network

size of the IoT device, a charge-pump (CP) based, fully on-chip, EH circuit is designed, realized and tested in this study.

The most important design feature of the EH circuit to be realized by this study is to achieve maximum power point tracking circuit (MPPT) for maximizing power conversion efficiency from the front-end photovoltaic (PV) panel to loads. The MPPT is made possible in this study by tuning the equivalent input impedance of a charge pump circuit to match the output impedance of the PV panel. Conventionally, the hill-climbing-based MPPT commonly seen in the literature used the power conversion ratio modulation or switched frequency modulation techniques. The MPPT circuit proposed by Liu and Sanchez-Sinencio (2015) and Kim et al. (2011, 2015) used the concept of frequency and capacitance tuning. Liu and Sanchez-Sinencio (2015) proposed a capacitive type energy harvesting circuit with MPPT circuit being able to provide an output bias of at least 1.5 V. The resulted maximum power conversion efficiency (PCE) is 86.4%. Similarly, Kim *et al.* (2011) propose an energy harvester circuit which achieve a maximum conversion efficiency of 86%. However, narrow output range, low PCE (< 42%) at idle (< 1 μA) and large chip area are the main drawbacks of the designs proposed by Liu and Sanchez-Sinencio (2015) and Kim et al. (2011). Rawy et al. (2018) proposed a DC–DC converter using 3D-MPPT. This circuit results in a higher conversion ratio of 88% at the input power of 200 μW. However, it still suffers from complex MPPT algorithm and circuit implementation, deep-submicron process parameter variation, production cost, and narrow output ranges.

For battery-less IoT applications, high integration ability, low complexity, re-configurability, dynamic output range, and production cost are most important design directives. By considering these directives, this study presents a new on-chip energy harvesting circuit for battery-less IoT beacon tags. This designed circuit includes a maximum power point tracking circuit and a cross coupled charge-pump circuit with shoot-through current suppression. Also in the designed circuitry is a hysteresis control

circuit providing high voltage protection; a low dropout (LDO) regulator offering an output voltage independent of the input voltage, loads as well as temperature variations. The experimental result shows that the input voltage range is allowed from 0.55 to 1.7 V to effectively harvest the solar power from a flexible dye-sensitized solar cell (DSSC). Note that DSSC is one kind of flexible PV panels that provides high conversion efficiency under indoor lighting environment. The resulted maximum output power is 200 μW, while the maximum PCE is 77%. For a wide range of lighting luminance (300–1300 lx), the achieved average PCE is more than 70%. Furthermore, for light load condition ($I_{out} < 1$ μA) over the input range of 0.55–1.7 V the achieved PCE is more than 52%.

The remainder of this study is organized as follows. The design of proposed EH circuit is discussed in Sect. 2. Simulation and the experimental results are presented in Sect. 3. Finally, Sect. 4 concludes this study.

2 The energy harvest (EH) system

An energy harvesting (EH) circuit is designed herein to collect the energy from the ambient energy source and then provide a stable bias to other load modules. In Fig. 2a, a complete block diagram of the EH circuitry is shown, where it is seen that the EH circuit incorporates a flexible dye-sensitized solar cell (DSSC), a maximum power point tracking unit, a cross-coupled charge pump circuit, a controller unit, a bandgap reference circuit (BGR), a driver unit, a sample signal generator circuit, a hysteresis control circuit and a low drop out (LDO) regulator. Note that DSSC is one kind of flexible PV panels that provides high conversion efficiency under indoor lighting environment. The circuit-level diagram of the proposed EH circuit is shown in Fig. 2b, where it should also be noted that the cross-coupled charge pump is slightly modified for shoot-through current suppression. Furthermore, the design and working principles of all the other sub-circuits, such as MPPT, BGR, etc., are discussed in details.

2.1 The solar cell

The flexible dye-sensitized solar cell (DSSC) with favorable performance under indoor lighting is used by this study for the design and experimental validation. Approximately, 15-20 μW/cm^2 of solar energy can be harvested by the DSSC solar cell in a size of 77 mm × 50 mm in an indoor environment of low-illumination intensity. The I–V curves of the DSSC for a wide range of lighting luminance (100–1300 lx) are shown in Fig. 3, where it is seen that the open-circuit output voltage (V_{oc}) ranges from 1.5 to 1.7 v. In fact, the equivalent inner impedance of the solar cell varies with illumination intensities, loads, and temperature. Figure 4 shows a simplified circuit model of the DSSC. The circuit model incorporates a current source, a reverse bias diode, a series resistance, and a shunt resistance.

2.2 The proposed cross-coupled charge pump circuit

A cross-coupled charge pump (CP) circuit is proposed herein to convert the DSSC output power to a required bias level to drive the load. The detailed topology of this circuitry is schematically shown in Fig. 5. Note that the cross-coupled charge pump circuit behaves like switched capacitors, therefore the equivalent resistance of the CP can captured by

$$R_{CP} = \frac{1}{fC}, \tag{1}$$

where f is the switching frequency while C is the pumping capacitance (Liu and Sanchez-Sinencio 2015) in the CP circuit. The maximum average output current I_{avg} can then be determined by

$$I_{avg} = \frac{\Delta Q}{t} = C\frac{\Delta V}{t} = 2fC\Delta V, \tag{2}$$

where C is the pumping capacitance while f is the switching frequency. Note that the factor of 2 accounts for the design practice that the charging period is one half of switching period. In a conventional cross-coupled CP circuit, the complementary voltage at the internal nodes is used to restrain the cross-coupled switches. This circuit minimizes the voltage drop at the output switches. In this circuit, only two non-overlap clocks (clk and clk_b) are needed to control the CP impedance. Moreover, during transition due to simultaneous conduction of the NMOS and PMOS switches, a possible shoot-through current flows from higher voltage nodes to the input node (V_{in}) of the CP. The resulting overshoot current reduces the charge pump efficiency and the output voltage (Lee and Mok 2005; Kim et al. 2005).

A mechanism of shoot-through current suppression equipping the proposed CP circuit is illustrated Fig. 5a, b. To avoid the shoot-through current, additional PMOS-switches (S_1–S_2) and resistors (R_{11}–R_{22}) are designed to control the timing of switches M_{pr} and M_{pl}. Therefore, the ON-time of NMOS and PMOS are staggered. As illustrated by Fig. 5a, b, during step 1, net_{2n} is at logic high while net1n is at low with clock clk being at logic 0. Thus, the NMOS M_{nl} turns ON. A dc current flows from higher voltage node (V_{in}) to the pumping capacitor via M_{nl}. Therefore, the voltage across the pumping capacitor rises up to a maximum of V_{in}–V_{thn}. Meanwhile, PMOS transistor

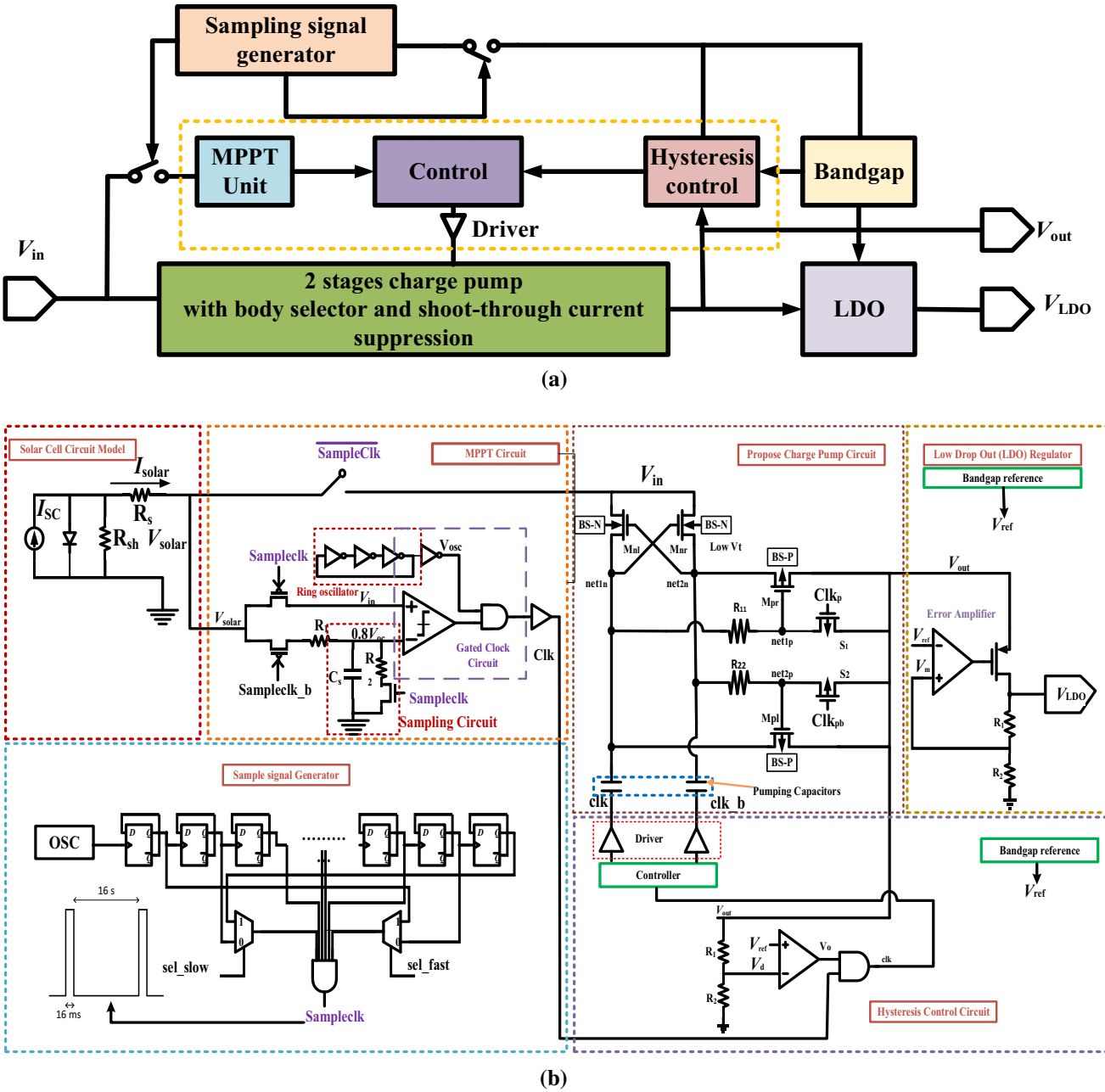


Fig. 2 **a** The proposed energy harvest (EH) circuit in functional blocks, **b** the EH circuitry in device level

M_{pl} is ON (while M_{pr} being OFF), and S_2 is ON (while S_1 being OFF). In results, the current flowing from the pump capacitor charges up the output node (V_{out}) via the transistor Mp1. The additional switch S_2 controlled by the signal clk_{pb} and resistance R_{22} add up in total an RC delay, which prevents the cross-coupled NMOS and PMOS switches to conduct simultaneously, successfully suppressing the shoot-through current. The identical process happens during step 2, the opposite pump capacitor charges from the higher potential node V_{in} while the output node is charged through PMOS transistor M_{pr}. Finally, the overall voltage at the output node (V_{out}) becomes 2.5 times (depends on the charge pump impedance) of the input voltage V_{in}.

It is pertinent to note at this point that as the source node of the cross-coupled transistors (M_{nl}–M_{nr} and M_{pl}–M_{pr}) switches during the aforementioned circuit operaitons, the body effect phenomena occurs. An adaptive body selector is required in the charge pump circuit to minimize the body effect. (Kim et al. 2013; Gasnier et al. 2014). A basic PMOS based body selector circuit employed by this study is shown in Fig. 6, which consists of a pair of low threshold

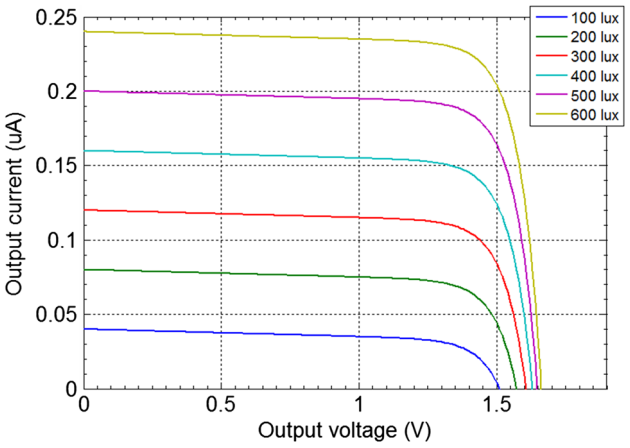


Fig. 3 Typical experimental I–V curves of the DSSC under varied environmental luminances

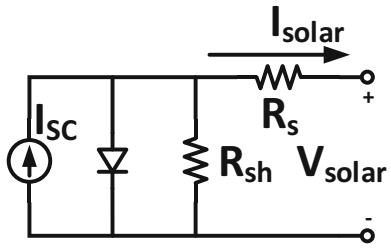


Fig. 4 The model for the adopted DSSC

(V_T) transistors to connect the body of the PMOS transistor symmetrically (Kim et al. 2015). If the voltage at node A is higher than node B, node B turns ON the transistor Ms_{el1}. Thus, the body of P-switch (MP) connects to high potential node A. Similarly, if the voltage at node A is lower than node B, node A turns ON the transistor M_{sel2}. Thus the body of P-switch (MP) connects to high potential node B. Similar circuit design for NMOS body selector can be implemented. Low V_T devices are employed herein to minimize the conduction losses. Also, it helps to enhance the adaptability for low start-up voltages.

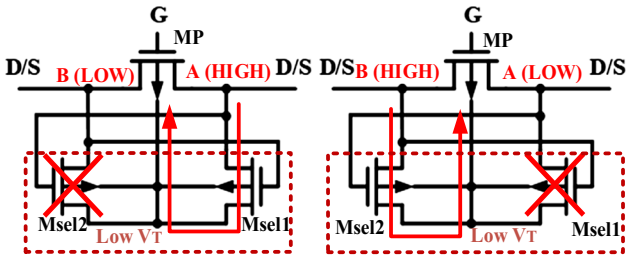


Fig. 6 The operational principles of the P-type body selector

2.3 Maximum power point tracking (MPPT) circuit

Towards the design of the MPPT circuit, the approach of fractional open circuit voltage (FOCV) is utilized for the advantages of low power consumption and simple architecture. The bandwidth of the solar cell varies according to its area and output capacitance, aranging from several hundreds of hertz to 1 kHz (Li et al. 2012). The response

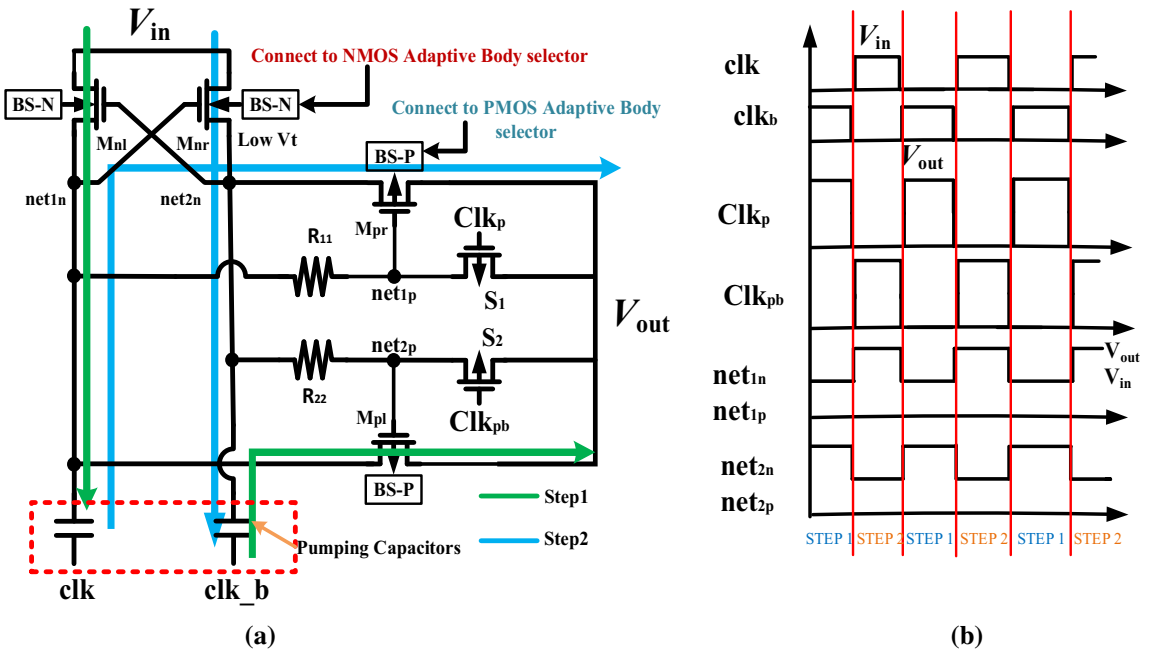


Fig. 5 **a** The cross-coupled charge pump proposed with shoot-through current suppression and body selectors, **b** the corresponding timing diagram

time for the solar cell is around 1–10 ms (Carreon-Bautista et al. 2014).

The design of MPPT starts with the effort on the circuit for generating sampling clocks as shown in Fig. 7, which incorporates a low-frequency, low-power ring oscillator, an asynchronous delayed flip flops (D-FF) based frequency divider, and an AND gate controlled with the select signal. The signals sel_slow & sel_fast pin is supplied to generate the output Sampleclk at a specific frequency. This signal if Sampleclk is further used to control the MPPT circuit to realize the alternating phases of charging and sampling (Men et al. 2016). The period and pulse width of the control signal are 16.016 s and 16 ms, respectively. Finally, in the period of 16 ms, logic '1' is used to control the subsequent sampling switch, while the 16 s of the logic '0' signal is used to control the operation of the charge pump.

The MPPT circuit shown in Fig. 8a incorporates a sampling circuit and a gated clock circuit. Figure 8b illustrates the principle of the gated clock employed herein. The sampling circuit comprises a voltage divider with resistors R_1, R_2, capacitor C_S and an NMOS switch. The size of the NMOS sampling switch is adjusted to minimize charge leakage. The resistances of the voltage divider, R_1 and R_2, is designed as 2 MΩ identically. In general, five times of the RC time constant (5τ) is required to fully charge or discharge the sampling capacitor (C_S). In this design, 16 ms is required to fully charge the sampling capacitor. The value of C_S is set to ensure that the voltage across C_S can reach steady state in time to prevent the charge leakage. In this way, the sampling capacitor C_S can be designed, following

$$Cs < \frac{\tau}{2\ \mathrm{M}\Omega} = \frac{3.2\ \mathrm{ms}}{2\ \mathrm{M}\Omega} = 1.6\ \mathrm{nF}. \quad (3)$$

As seen from Figs. 1 and 8a for circuit design, the sampling phase starts when Samplclk is at logic '1' while the charging/tracking phase starts when Samplclk is at logic '0'. In the sampling phase, the solar cell charges the

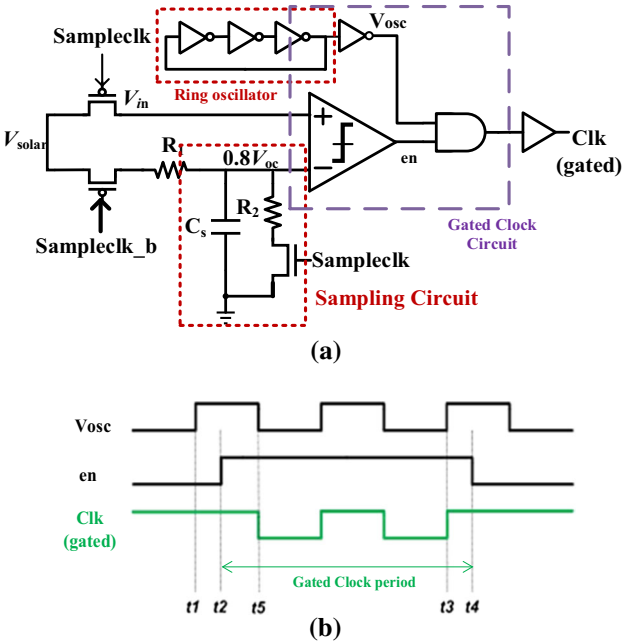


Fig. 8 **a** The circuit implementing maximum power point tracking (MPPT), **b** an illustration of the gated clock in a diagram

sampling capacitor to $0.8V_{oc}$, while in the charging phase solar cell current (I_{solar}) charges the pumping capacitors of the cross-coupled charge pump. Note that V_{oc} is the open circuit voltage of the solar cell.

The design of the MPPT circuit also incorporates a ring oscillator, a latched comparator, and an AND gate. The operating frequency of the ring oscillator is 2 MHz. The maximum power point of the solar cell is set to 0.8 times of the open circuit voltage (V_{oc}). During the sampling phase, $0.8V_{oc}$ is stored on the sampling capacitor. In the charging/tracking phase, the latched comparator compares the input voltage (V_{in}) with the $0.8V_{oc}$. If the input voltage V_{in} is higher than $0.8V_{oc}$, the comparator output switches to logic high, and then the AND gate allow the oscillator to output V_{osc} in a gated period, i.e., the Clk illustrated by Fig. 8b. Then the Clk is applied to the controller and driver

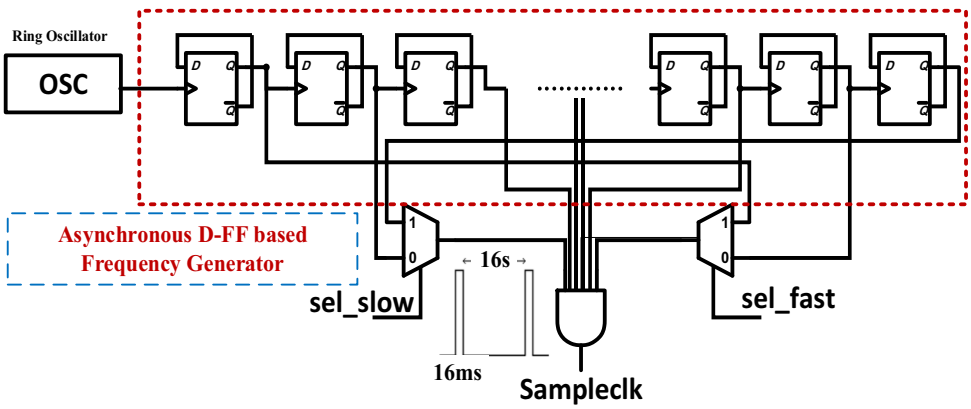


Fig. 7 The circuit for generating sampling clocks

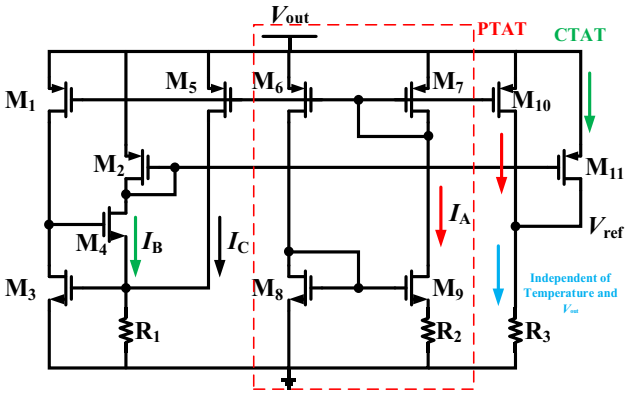


Fig. 9 The designed bandgap reference circuit

unit which generate a non-overlap clock and control signals, clk-clk_b and clk_p-clk_{pb}, for the subsequent pumping circuit to charge/discharge. Based on Eq. (1), the input impedance of the charge pump circuit is decreased to have V_{in} finally reaching $0.8V_{oc}$, the maximum power point. On the other hand, when V_{in} is less than the $0.8V_{oc}$, the output of the comparator switched to logic low and then the AND gate stop the output clock (Clk). In this way, the input impedance of the charge pump circuit increases, which force V_{in} to approach $0.8V_{oc}$. The aforementioned mechanism is actually based on a gated clock to achieve MPPT.

2.4 Bandgap reference circuit

The incorporation of the bandgap reference (BGR) circuit in to the entire circuitry in Fig. 2 (b0 provides a stable reference voltage to the low-dropout regulator and hysteresis control unit. The BGR circuit ensures sufficient power supply noise rejection from the supply voltage and temperature variation. Figure 9 shows the subthreshold bandgap reference circuit (Men et al. 2016; Huang et al. 2006). The principle of the BGR is to design a proportional to absolute temperature current (PTAT) and a complementary to absolute temperature current (CTAT). In this circuit, the quiescent current is less than 5 μA. The output reference voltage can be derived, yielding

$$V_{ref} = \left[\frac{P_{10}}{P_7} I_A + \frac{P_{11}}{P_2}\left(\frac{V_{GS3}}{R_1} - NI_A\right)\right] \times R_3 \quad (4)$$

where $P = \frac{W_{eff}}{L_{eff}}$, and N is the multiple of current I_A.

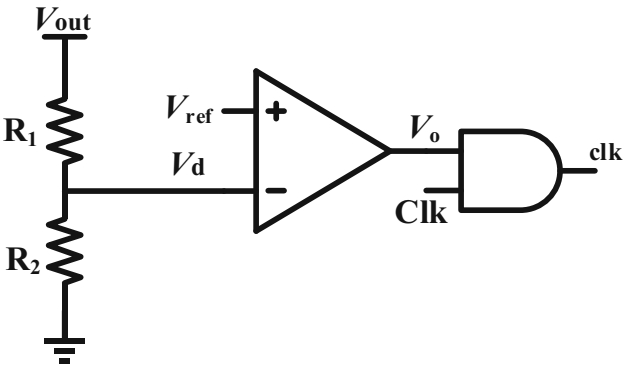
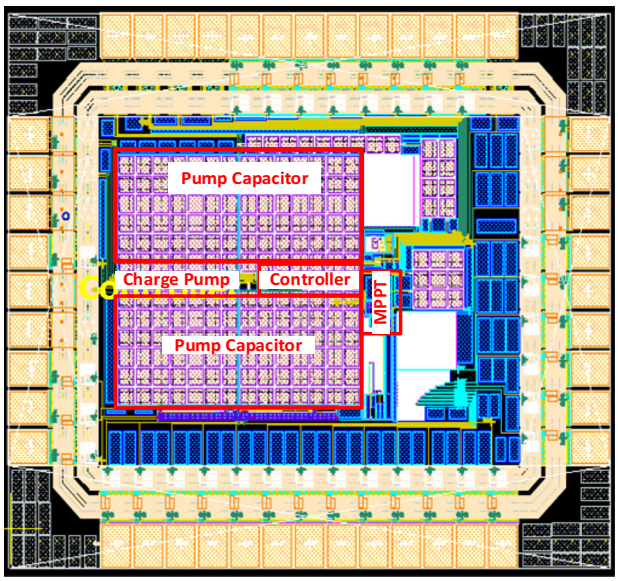
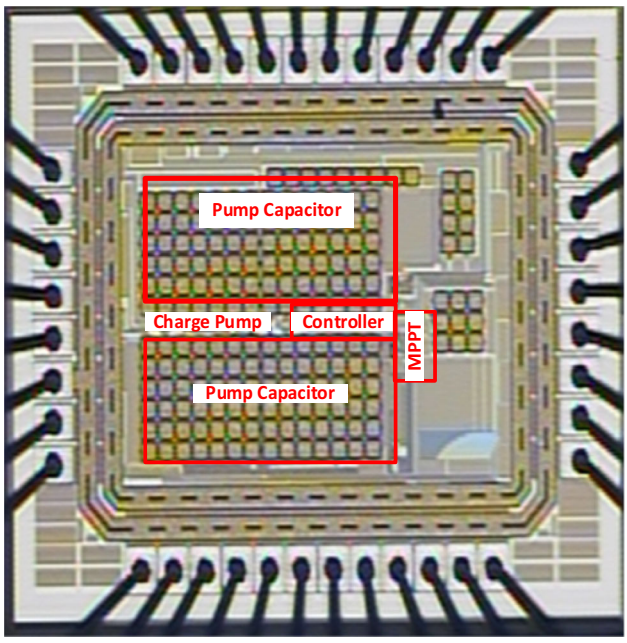


Fig. 10 The hysteresis control circuit at output



(a)



(b)

Fig. 11 **a** The layout and **b** die photo of the taped-out chip

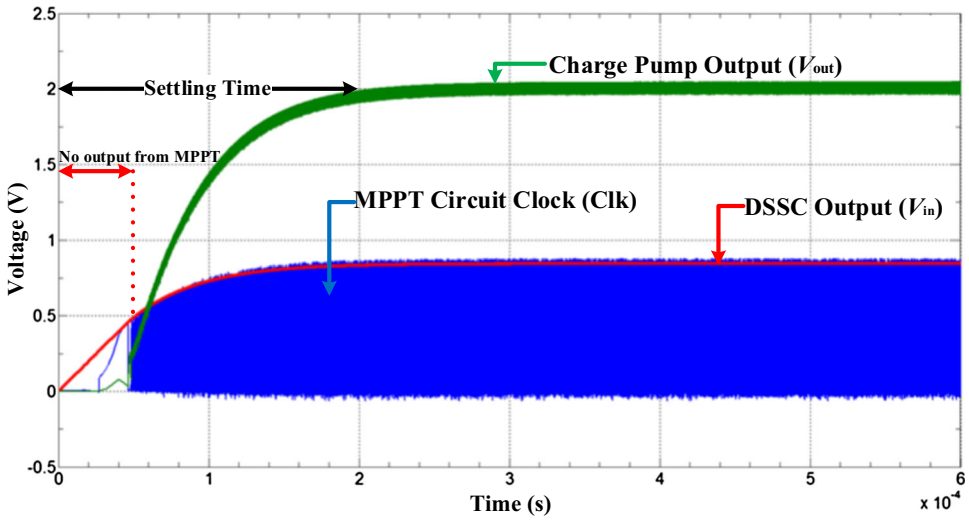
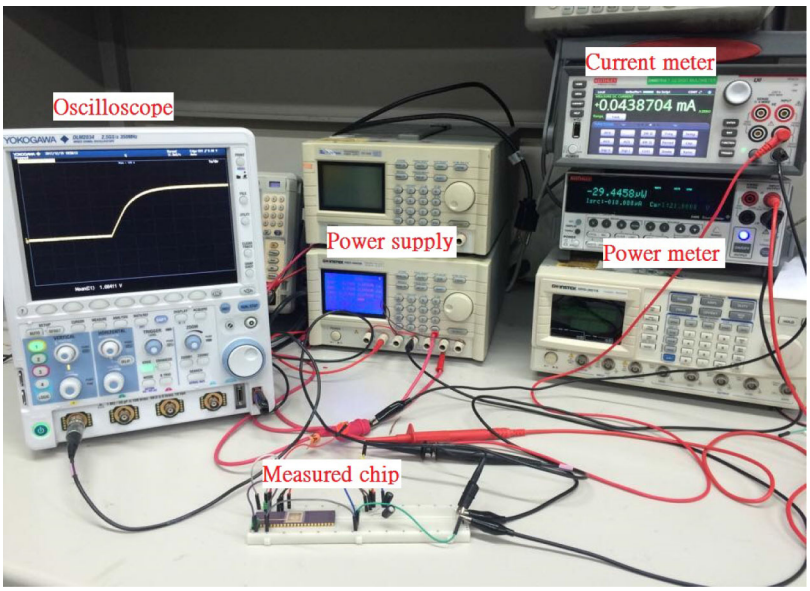
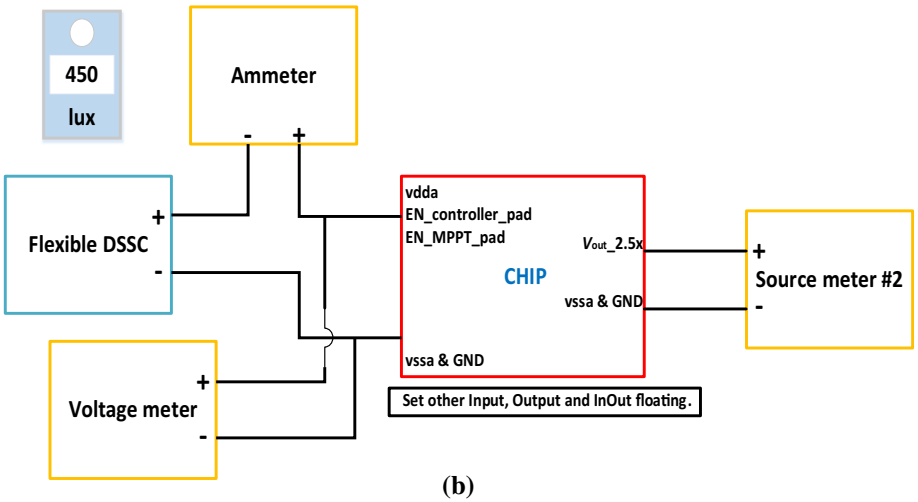


Fig. 12 Simulation result of the charge pump circuit



(a)



(b)

Fig. 13 **a** Experimental setup, **b** the measurement system in blocks

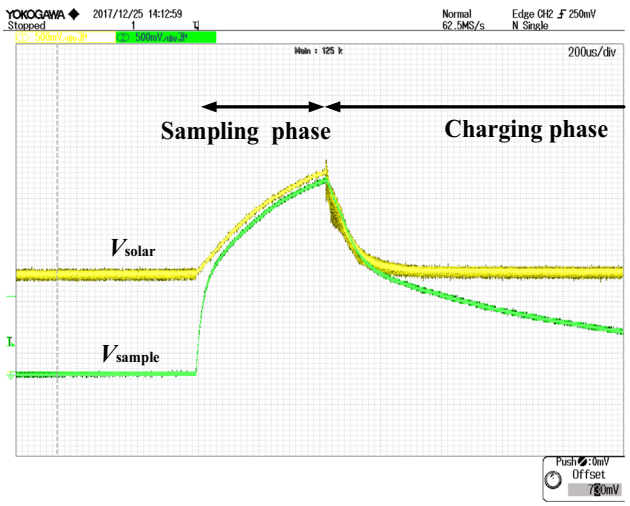


Fig. 14 Measurement result of the designed MPPT circuit

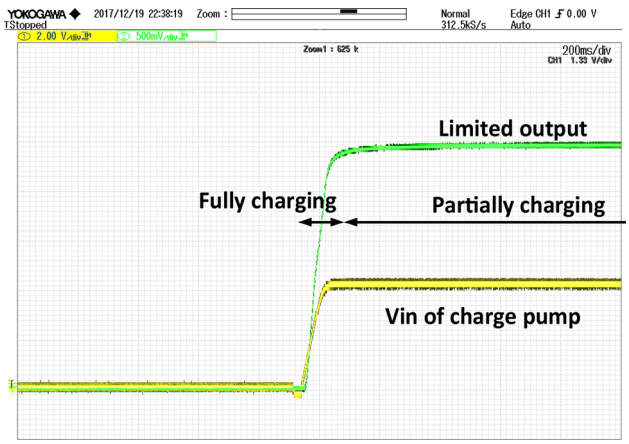


Fig. 16 Experimental result of the hysteresis control circuit

2.5 Output hysteresis control circuit, controller, driver and low dropout regulator circuits

An output hysteresis control circuit shown in Fig. 10 is designed herein for controlling the maximum output level of the charge pump circuit. It consists of a voltage divider, a P-type latch comparator, and an AND gate. In this circuit, the resistances of the voltage divider determine the limiting voltage V_d. Seen in Fig. 10, if V_d is higher than V_{ref}, then the output of the comparator V_o switches to logic '0', and then the AND gate stop outputting the clock signal (clk). Thus, the function of the charge pump circuit is automatically limited to partially charging state only. In another case, when the output voltage of charge pump is not too high (V_d<V_{ref}), V_o changes to '1' then the clock signal passes through AND gate, then charges the charge pump circuit to operate normally. One of the significant benefits of the hysteresis control is that it provides high voltage protection. Another advantage is that the limiting voltage V_d can be tuned for various applications by varying the divider resistor R_1 and R_2.

The controller block incorporates a non-overlap logic generator and a level shifter. The non-overlap clock generator circuit generates the signals of clk and clk_b by using the CLK signal from the MPPT circuit. To turn off the PMOS switches S_1 and S_2 in the CP as shown in Fig. 2b, it is required to increase the voltage level of the control signals clk_p & clk_{pb}. A level shifter circuit generates high voltage levels of clk_p & clk_{pb} from clk and clk_b. An inverter based driver provide a transient current to the pumping capacitances. Meanwhile, the switching inside the CP brings high ripples at the output pin (V_{out}). A low-dropout (LDO) regulator is designed herein to filter out the ripples and provide a stable output voltage (V_{LDO}) for external loading. (Shao et al. 2009; Kim et al. 2011). The

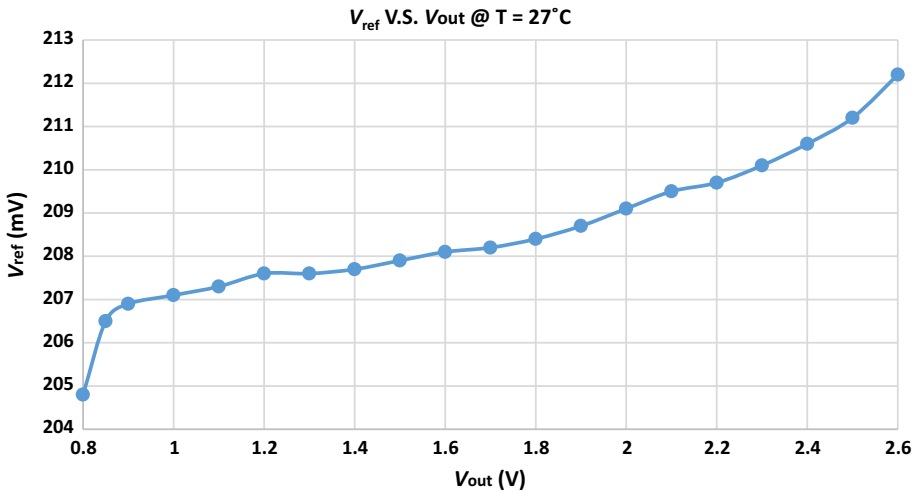


Fig. 15 Experimental result of the bandgap reference circuit within the possible range of V_{out}

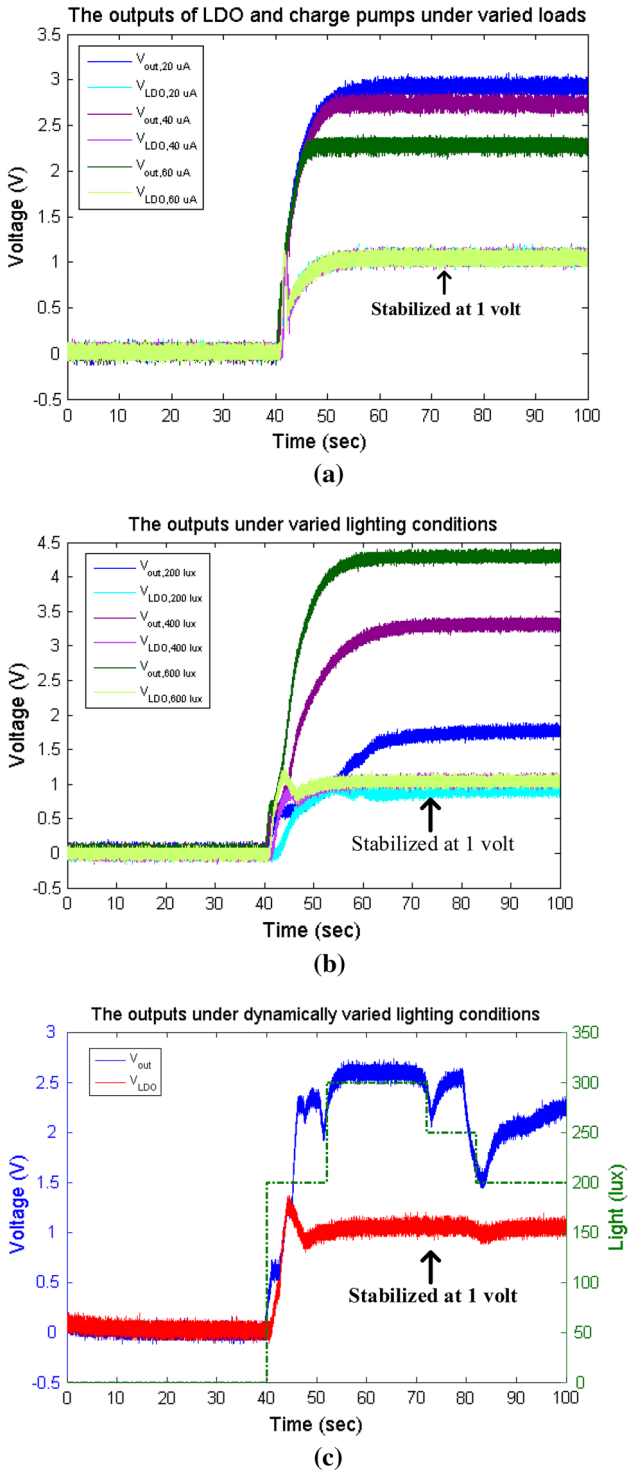


Fig. 17 Experimental results of LDO and charge pump outputs under **a** varied loads, **b** varied indoor lighting conditions, **c** dynamically varied lighting conditions

design of the low-dropout (LDO) regulator circuit incorporates an error amplifier, a pass transistor, and a voltage divider.

3 Simulation and experimental results

With the EH circuit designed successfully, an effort is devoted to simulation and experiment to validate the expected performance of the designed EH circuit. The designed EH circuit is first realized in a chip layout for the TSMC 0.18 μm process, as shown in Fig. 11a. Simulations based on the chip layout are then carried out. Figure 12 show the simulated dynamics of voltages at selected nodes. It is seen from this figure that the MPPT is not ON until the DSSC output, Vin, reaching 0.5 V. Then with MPPT ON, the output voltage of the charge pump, V_{out}, stabilizes around 0.2 ms at 2 V, as expected as 2.5 times of the input voltage of 0.8 V.

The designed circuit has been next taped out by the TSMC 0.18 μm process. The die photo is shown in Fig. 11b, where the chip area is 1.2 mm^2. Figure 13 presents the experimental setup and measurement blocks. A flexible DSSC panel is available for harvesting indoor lighting power. The environmental lighting intensity is tuned at varied luminance from 300 to 1300 lx. Figure 14 shows the experimental result of the MPPT circuit. In this figure, the yellow curve denotes the output voltage of the DSSC, while the green one does the sampling voltage (V_{sample}) which is 0.8 times of the DSSC output. The midpoint of the green curve shows the maximum power point voltage in the charging phase. It can be seen that the DSSC operates at the maximum power point for a short time. Consequently, the sampling and charging phases are repeated to track the maximum power point. Figure 15 presents the experimental result of the bandgap reference circuit. Testing result shows that the output of bandgap reference circuit is stable at 206 mV ± 2 mV for the input sweep of 0.9–2.5 V. The measured quiescent current and PSSR of bandgap reference circuit is 3.74 μA and 1.3 mV/V respectively. Figure 16 shows the experimental result of the limiting function performs by the output hysteresis control circuit. In this figure, the yellow line shows the constant 4 V external supply to charge pump circuit while the yellow line shows the output of the charge pump circuit also, the output voltage is limited at about 3 V. Note that, without this limiting function, the output voltage would keep rising to about 12 V and may damage the IC. Figure 17a shows the experimental result of the LDO regulator. In this figure, the green curves are the outputs of the cross-coupled charge pump circuit, while the yellow ones are those of the LDO regulator circuit. It can be seen from this figure that the LDO circuit can regulate the charge pump output voltage V_{out} to a stable constant voltage of 1 V to varied loads. On the other hand, Fig. 17b show the experimental outputs for charge pump and LDO under varied environmental lighting conditions. It can be also

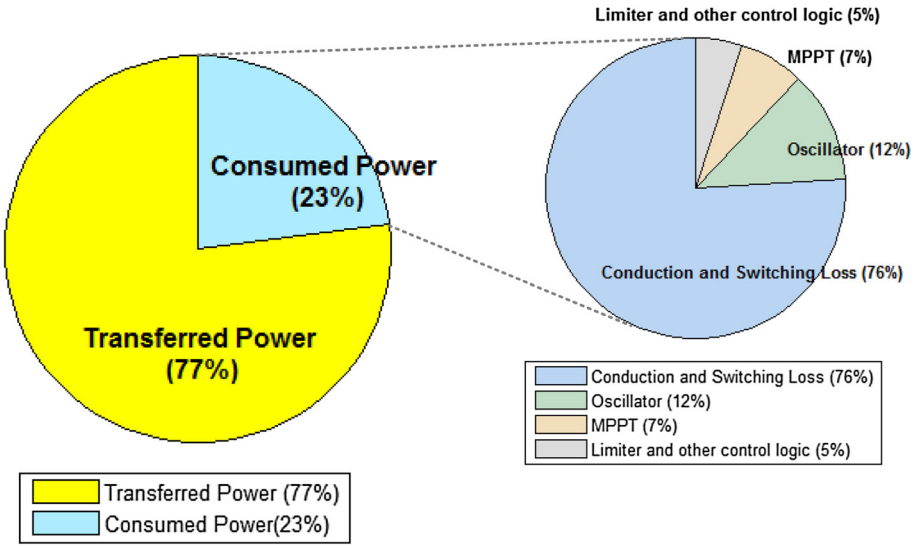


Fig. 18 Breakdown of power consumption

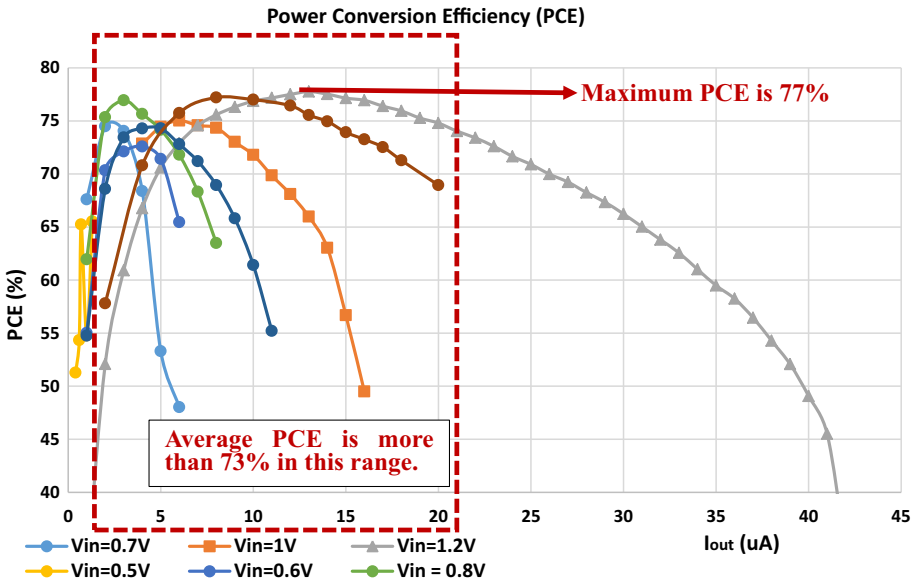


Fig. 19 PCE versus the output load currents at different input voltages

Table 1 Comparison table

Property	Proposed chip	Kim et al. (2015)	Liu and Sanchez-Sinencio (2015)	Kim et al. (2011)
Process	0.18 μm	0.13 μm	0.18 μm	0.35 μm
Input voltage	0.55–1.7 V	> 0.15 V	1.1–1.5 V	1–2.7 V
Output voltage	1–3.3 V	> 0.6 V	3.3 V	2 V
Output power	0–200 μW	Not mentioned	0–21 μW	0–80 μW
MCE	77% @52 μW	72.5%	86.4% @12 μW	86% @35 μW
MCE for load current 0.35 μA to 1 μA	> 60%	< 40%	< 40%	< 40%
Area	1.2 mm^2 (with pad)	0.66 mm^2 (without pad, off-chip capacitors)	2.25 mm^2 (with pad)	2.28 mm^2 (without pad)

seen clearly that the LDO output is stabilized well at 1 V at steady state under varied lighting conditions. Lastly, dynamical lighting conditions are also applied to validate the circuit performance. Figure 17c shows that the LDO can quickly be stabilized at 1 V with the lighting changed among 200, 300, 250 and 200 lx through every period of 10 s at steady state. On the other hand, Fig. 18 shows the power consumptions by different circuit blocks. It is seen that the 77% of the power harvested from the DSSC is successfully transferred to power a battery-less IoT beacon tag. Note also from this figure that most of the power consumption occurs due to conduction and the switching losses. The MPPT circuit consumes 1.164 μW, which is only 3% of the total power consumption, validating a successful design by this study. The power conversion efficiency (PCE), the ratio of total output power P_{out} to the input power P_{in}, is calculated herein by

$$PCE = \frac{P_{out}}{P_{in}}, \tag{5}$$

to evaluate the performance of the EH circuit, In practice, this PCE is affected by the input voltage and the load. Figure 19 shows the variation of PCE with respect to different output load currents at different input voltages. The maximum PCE of the proposed circuit is about 77% at the input power of 52 μW. Furthermore, the average maximum PCE is more than 70% for the input range from 0.55 to 1.2 V. For light load condition ($I_{\text{out}} < 1$ μA) over the input range of 0.55 to 1.2 V, the achieved PCE is more than 52%. Compared with the results of (Kim et al. 2015; Liu and Sanchez-Sinencio 2015; Kim et al. 2011), the power consumption of the MPPT circuit proposed herein is 50 percent lower, and the average PCE is higher for the input range of 0.55 to 1.7 V. Table 1 compares the performances of the proposed work with other similar energy harvesters. The comparison shows that the proposed EH circuit allows minimum input voltage sense of 0.55 V, high PCE (77%), wide output range (1–3 V) and high throughput power (200 μW). Note that this throughput of 200 μW is consistent to the maximum power that can be transmitted by the switching pumping capacitors as shown in Fig. 5.

4 Conclusion

This study proposes a new, efficient energy harvesting (EH) circuit equipped with a modified cross-coupled charge-pump for a flexible dye sensitized solar cell (DSSC) to power a battery-less IoT beacon tag. In this EH circuit, a ring oscillator with the function of gated clock is designed to drive the switched capacitances in the charge pump. The gated clock is tuned in a self-adaptive fashion to match the input impedance of the energy harvest circuit with the output impedance of the DSSC, thus achieving successfully maximum power point tracking (MPPT) for high power conversion efficiency. The circuit is implemented in an integrated chip with area of 1.2 mm^2 via the TSMC T18 process. Experiments are conducted and show that with the DSSC output ranging from 0.55 to 1.7 V, the designed charge pump controlled with the orchestrated gated clock can effectively harvest the indoor lighting power with a maximum power conversion efficiency (PCE) of 77% at an input power of 52 μW from the DSSC. It is also proved that the PCE of 70% and higher can be achieved over a large range of lighting luminance from 300 to 1300 lx. The achieved wide input and output range and the maximum throughput power of 200 μW is much larger than others reported, while the 77% of PCE is close to the best power conversion efficiency ever reported.

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References

Carreon-Bautista S, Eladawy A, Mohieldin AN, Sanchez-Sinencio E (2014) Boost converter with dynamic input impedance matching for energy harvesting with multi-array thermoelectric generators. IEEE Trans Ind Electron 61(10):5345–5353

Esram T, Chapman PL (2007) Comparison of photovoltaic array maximum power point tracking techniques. IEEE Trans Energy Convers 22(2):439–449

Gasnier P, Willemin J, Boisseau S, Despesse G, Condemine C, Gouvernet G, Chaillout J-J (2014) An autonomous piezoelectric energy harvesting IC based on a synchronous multi-shot technique. IEEE J Solid-State Circuits 49(7):1561–1570

Goerlich K (2016) Live business: the importance of the internet of things," live business, internet of things, knowledge networks, Redefining Resource Management, May 05, 2016

Huang P-H, Lin H, Lin Y-T (2006) A simple subthreshold CMOS voltage reference circuit with channel- length modulation compensation. IEEE Trans Circuits Syst II Express Briefs 53(9):882–885

Kim J, Mok P, Hoi Lee (2005) Switching noise and shoot-through current reduction techniques for switched-capacitor voltage doubler. IEEE J Solid-State Circuits 40(5):1136–1146

Kim J, Kim J, Kim C (2011) A regulated charge pump with a low-power integrated optimum power point tracking algorithm for indoor solar energy harvesting. IEEE Trans Circuits Syst I Express Briefs 58(12):802–806

Kim H, Min Y, Jeong C, Kim K, Kim C, Kim S (2013) A 1-mW solar-energy-harvesting circuit using an adaptive MPPT with a SAR and a counter. IEEE Trans Circuits Syst II Express Briefs 60(6):331–335

Kim J, Mok P, Kim C (2015) A 0.15 V input energy harvesting charge pump with dynamic body biasing and adaptive dead-time for efficiency improvement. IEEE J Solid-State Circuits 50(2):414–425

Lee H, Mok PKT (2005) Switching noise and shoot-through current reduction techniques for switched-capacitor voltage doubler. IEEE J Solid-State Circuits 40(5):1136–1146

Li X, Tsui C, Ki W (2012) Solar energy harvesting system design using re-configurable charge pump. In: 2012 IEEE faible tension faible consommation, Paris, 2012, pp 1–4

Liu X, Sanchez-Sinencio E (2015) An 86% efficiency 12 μW self-sustaining PV energy harvesting system with hysteresis regulation and time-domain MPPT for IOT smart nodes. IEEE J Solid-State Circuits 50(6):1424–1437

Men G-Y, Cheng Y-P, Chao PC-P, Yang C-C, Pribadi EF (2016) A charge pump with MPPT circuit employed in batteryless photovoltaic IoT tags. ASME 2016 Conference on Information Storage and Processing Systems, pp V001T09A003

Rawy K, Yoo T, Kim TT (2018) An 88% efficiency 0.1–300 μW energy harvesting system with 3-D MPPT using switch width modulation for IoT smart nodes. IEEE J Solid-State Circuits 53(10):2751–2762

Reinisch H, Wiessflecker M, Gruber S, Unterassinger H, Hofer G, Klamminger M, Pribyl W, Holweg G (2011) A multifrequency passive sensing tag with on-chip temperature sensor and off-chip sensor interface using EPC HF and UHF RFID technology. IEEE J Solid-State Circuits 46(12):3075–3088

Shao H, Tsui C, Ki W-H (2009) The design of a micro power management system for applications using photovoltaic cells with the maximum output power control. IEEE Trans Very Large Scale Integration Syst (VLSI) 17(8):1138–1142

Yao R, Wang W, Farrokh-Baroughi M, Wang H, Qian Y (2013) Quality-driven energy-neutralized power and relay selection for smart grid wireless multimedia sensor based IoTs. IEEE Sensors J 13(10):3637–3644