UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Spring 1404
Computer Assignment 4

FSMs and Counters - Week 10

Name:	**Date:**
Username:	

A sequence detector searches for a 1 followed by six 0's and then a final 1. When this is detected on the J input, the output becomes 1 for exactly one clock cycle and then the search begins again.

For implementing this circuit, you need a Moore machine and a divide by 6 circuit. Write SystemVerilog description of this part using a sequence detector and a divider. Both parts are to be written in SystemVerilog and the two should be completed as a unit to be used in the next Computer Assignment.

a. Show a block diagram of an FSM and a counter for implementing this circuit.
b. Show the state diagram that initiates the six-counter and waits for the count of 6.
c. Show how the counter is initialized and utilized during the sequence detection.
d. Write SystemVerilog description of the sequence detector. In the same module, write the **always** statements for the FSM part and one for the counter.
e. Using a SystemVerilog testbench in the ModelSim simulation environment completely simulate your circuit. This is your pre-synthesis description.
f. Import your sequence detector in Quartus and build a symbol for it. Synthesize this design and see its timing, floor-plan and cells used. The synthesis process generates the post-synthesis description of your start-sequence detector. The .vo and .sdo files that are produced contain the netlist and timing of the synthesized circuit.
g. Instantiate the pre- and post-synthesis descriptions of the sequence detector in a SystemVerilog testbench and compare the timing of the two descriptions.

Deliverables:

Generate a report that includes all the items below:

A. Prior to coming to the lab, for all the above problems hand-drawn schematic diagrams and partial timing diagrams are required. Your SystemVerilog descriptions must correspond to the circuit diagrams. Your simulation run and the project built for this purpose must be demonstrated to the TA.
B. Document your Quartus projects. Make sure you understand the synthesis outputs and their corresponding timings.

C. For the circuit you are designing, you should look at the FPGA layouts, device view and RTL view. Be able to explain the details of various views. In the layout, be able to identify FPGA cells that use a memory element versus those that are purely combinational.
D. Be prepared to answer questions asked about the timings, generated hardware, pre- and post- synthesis, and FPGA mappings.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAnn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.