Single Miller Capacitor Frequency Compensation with Nulling Resistor for Three-Stage amplifiers

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Abstract—A frequency compensation technique for three-stage amplifiers is introduced. The proposed solution exploits only one Miller capacitor and a resistor in the compensation network. The straightness of the technique is used to design, using a standard CMOS 0.35-μm process, a 1.5-V OTA driving a 150-pF load capacitor. The dc current consumption is about 14 μA at DC and a 1.6-MHz gain-bandwidth product is obtained, providing significant improvement in both MHz·pF/mA and (V/μs)·pF/mA performance parameters.

I. INTRODUCTION

With the scale down of transistor dimensions and supply voltages, multistage amplifiers have become increasingly important because they can provide dc-gains in excess of 100 dB and large output swings under low supply voltage. Nevertheless, the design of such amplifiers is a challenging task since the increased number of high impedance nodes (and, in turn, of low frequency poles) may result in instability or in a poor frequency performance. Therefore, many compensation techniques have recently been proposed [1]-[14].

When the amplifier is made up of three gain stages and the second is the only inverting one, the most suitable option is the reversed nested Miller compensation (RNMC) [1], [9]-[14], whose topology is shown in Fig. 1. Unfortunately, the basic RNMC technique exhibits an undesired right-half-plane (RHP) zero which limits the maximum achievable bandwidth. Then, some solutions to remove the RHP zero have been suggested [10]-[14]. Although these solutions resolve the stability problems, the high power dissipation required by the compensation network remain a serious problem.

In this paper we develop a power efficient compensation technique, improving the simple RNMC topology by exploiting only one Miller capacitor [5] and a resistor. The compensation network can be implemented without using extra transistors, thus optimizing power consumption Design equations which allow setting the values of the compensation network elements for the desired phase margin are carried out.

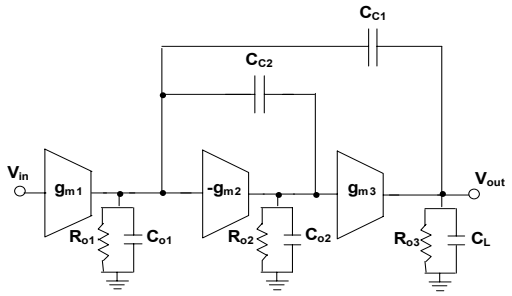

Figure 1. Reversed nested miller compensation topology.

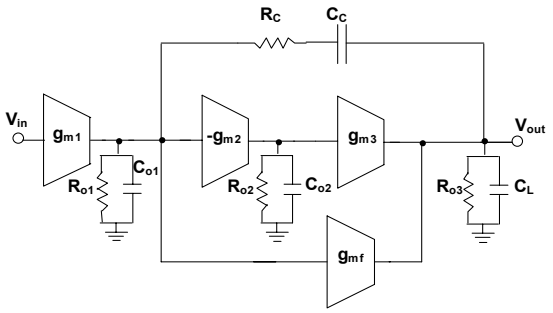

Figure 2. Proposed compensation topology.

II. PROPOSED COMPENSATION TECHNIQUE

The proposed solution is shown in Fig. 2 where g_{mi}, R_{oi} and C_{oi} are the i-th stage transconductance, resistance and equivalent output capacitance, respectively. The compensation is realized by the capacitor C_C in series with the resistor R_C, connected across the second and third stage, and the feedforward stage g_{mf}. Assuming $C_C >> C_{oi}$, $g_{mi}R_{oi} >> 1$, $i=1,..3$, the open-loop transfer function of the circuit in Fig. 2 is expressed by

$$A_v(s) \approx A_0 \frac{1+s\dfrac{g_{m2}g_{m3}C_C R_{o2}R_C + g_{mf}C_C R_C - C_C}{g_{m2}g_{m3}R_{o2}} + s^2 \dfrac{g_{mf}R_C - 1}{g_{m2}g_{m3}} C_C C_{o2}}{\left(1+\dfrac{s}{\omega_{P1}}\right)\left(1+s\dfrac{C_L}{g_{m2}g_{m3}R_{o2}} + s^2\dfrac{C_{o2}C_L}{g_{m2}g_{m3}}\right)(1+sC_{o1}R_C)} \quad (1)$$

where $A_0 \approx g_{m1}R_{o1}g_{m2}R_{o2}g_{m3}R_{o3}$ is the DC gain and $\omega_{P1} \approx 1/\left(C_C R_{o1} g_{m2} R_{o2} g_{m3} R_{o3}\right)$ is the dominant pole. Consequently, the gain-bandwidth product is, as usual, $GBW = g_{m1}/C_C$. The function exhibits two nondominant poles, another high-frequency pole, that will be neglected in the analysis to come, and two zeroes that can be made both negative by setting $g_{mf} > g_{m3}$. In particular, setting $g_{mf} = g_{m3} = 1/R_C$ the s^2 term in the numerator of (1) is set equal to zero and the transfer function is rewritten as

$$A_v(s) \approx A_0 \frac{1+s\dfrac{C_C}{g_{m3}}}{\left(1+\dfrac{s}{\omega_{P1}}\right)\left(1+s\dfrac{C_L}{g_{m2}g_{m3}R_{o2}} + s^2\dfrac{C_{o2}C_L}{g_{m2}g_{m3}}\right)} \quad (2)$$

and only a LHP zero, $z = g_{m3}/C_C$, is left, which can be used to improve phase margin.

A. Design guidelines

Let us now develop some design equations for the proposed compensation technique introducing the phase margin as additional design parameter. Using relation (A4) in the appendix, the phase margin Φ can be expressed as

$$\tan(\Phi - \Phi_z) = \frac{g_{m2}g_{m3}C_C^2 - g_{m1}^2 C_{o2}C_L}{g_{m1}C_C C_L} R_{o2} \quad (3)$$

where $\Phi_z = \tan^{-1}(g_{m1}/g_{m3})$ is the contribution due to the LHP zero.

The last design constraint regards asymptotic stability and is obtained by applying (A6) in the Appendix:

$$GBW < \frac{1}{C_{o2}R_{o2}} \quad (4)$$

It can be seen that, in principle, very high values of the gain-bandwidth product can be obtained, since C_{o2} is a parasitic capacitance.

III. Simulation Results

The analyzed compensation strategy was exploited to design a three-stage amplifier using a triple-metal double-poly 0.35-µm CMOS process, supplied by AMS. Figure 3 shows the schematic of the OTA used in simulations with Spectre. The input stage is made up of transistors M1-M8 implementing a folded cascode stage. The second inverting stage is made up of common source M9-M10. The last non-inverting stage is realized by transistors M11-M14. In particular, the feedforward transconductance stage g_{mf} is realized through M13 whose gate is connected to the output of the first stage, thus implementing a pseudo class AB output stage which is capable of driving the load capacitor, C_L, with a current much higher than the output branch quiescent current. The compensation resistor R_C was implemented using a NMOS in triode region.

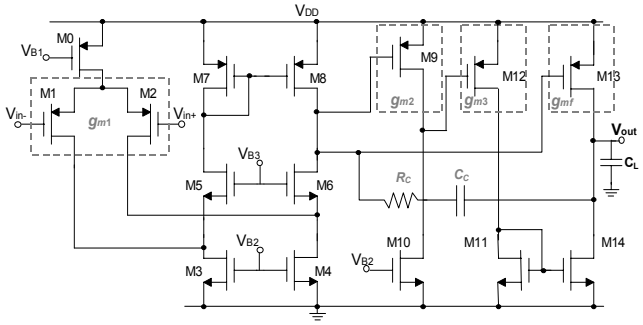

Figure 3. Simplified schematic of the OTA with the proposed compensation network used in simulations.

Transistors aspect ratios are reported in Table I. The OTA was powered with a 1.5-V supply and the total current dissipation is 14 µA. The load capacitance was set equal to 150 pF. The stage transconductances are g_{m1}=22.4 µA/V, g_{m2}=40.6 µA/V $g_{m3} \cong g_{mf}$=87 µA/V, and the compensation capacitor is C_C=2.2 pF. Figure 4 shows the OTA open-loop frequency response.

TABLE I. Transistors aspect ratios.

Transistor	Value
M0	40/1.4
M1, M2	30/0.35
M3, M4,M5, M6,M10	10/1.4
M7, M8	24/1.4
M9	12/0.35
M12, M13	24/0.35
M11, M14	50/1.4

As predicted by the design procedure, the *GBW* and the phase margin are equal to 1.6 MHz and 57°, respectively. The time response of the amplifier in unity-gain configuration to a 300-mVpp input step is shown in Fig. 5. Positive (negative) slew rate and settling time were +0.5 (–0.8) V/µs and 2 (0.6) µs.

The OTA main performance parameters are summarized in Table II. To provide a performance comparison between the proposed compensation technique and other reported compensation topologies two figures of merit, $FOM_S = (GBW \cdot C_L)/Power$ and $FOM_L = (SR \cdot C_L)/Power$, are

commonly used. To ensure a comparison independent of the particular supply voltage, two other figures of merit are frequently used, $IFOM_S=(GBW \cdot C_L)/I_{TOT}$ and $IFOM_S=(SR \cdot C_L)/I_{TOT}$ [3]-[8]. The higher the value of the figures of merit, the better is the amplifier performance. The values of the figures of merit of different three-stage amplifiers are reported in Table III.

It can be seen that the proposed compensation techniques outperforms all the other previously reported nested and reversed-nested Miller topologies, while requiring only two passive components in the compensation network.

TABLE II MAIN PERFORMANCE PARAMETERS.

Parameter	Value
Power Supply	1.5V
Total Bias Current	14 µA
Loading Capacitance	150 pF
DC Gain	113 dB
Gain-bandwidth Product	1.8 MHz
Phase Margin	57°
Gain Margin	9 dB
Positive/Negative Slew Rate	0.5/-0.8 V/µs
Positive/Negative 1% Settling Time	2/0.6 µs

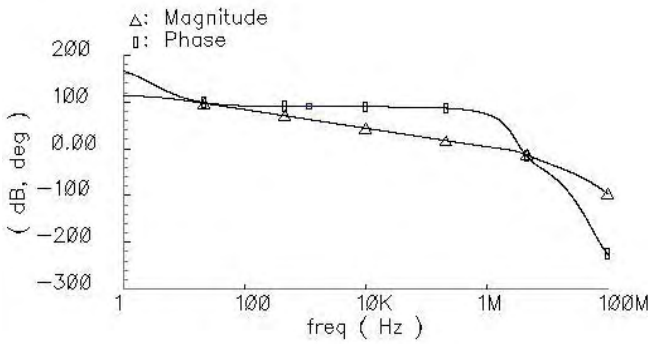

Figure 4. Open-loop frequency response.

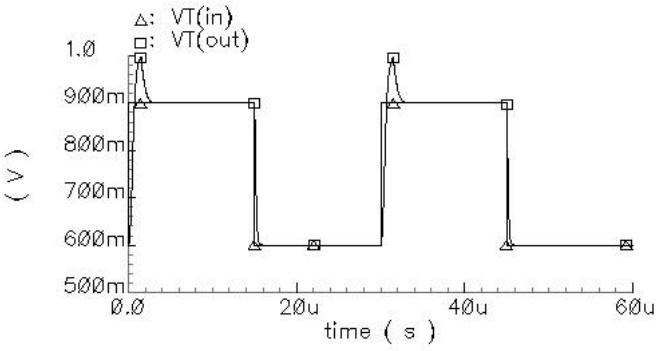

Figure 5. Unity-gain buffer transient response.

TABLE III. PERFORMANCE COMPARISON OF DIFFERENT AMPLIFIERS.

	C_L (pF)	V_{DD} (V)	I_{TOT} (mA)	*Power* (mW)	*GBW* (MHz)	*SR*[b] (V/µs)	*Comp. Capacitors* (pF)	FOM_S (MHz·pF)/mW	FOM_L (V/µs·pF/mW)	$IFOM_S$ (MHz·pF/mA)	$IFOM_L$ (V/µs·pF/mA)
RNMC with VB [10][a]	10	1.5	0.055	0.083	4.5	2.3	C_{C1}=3.7 C_{C2}=2.2	542	277	818	418
RNMC with VB NR [11]	15	3	0.48	1.44	19.46	13.8	C_{C1}=3 C_{C2}=0.7	209	149	608	431
NFRNMC [12][a]	120	2	0.18	0.36	2.5	-	C_{C1}=7 C_{C2}=1	833	-	1667	-
CFRNM [12][a]	120	2	0.2	0.40	2.5	-	C_{C1}=7 C_{C2}=1	750	-	1500	-
RAFFC [13][a]	500	2	0.12	0.24	1.75	1.52	C_{C1}=11.5 C_{C2}=0.5	3645	3166	7292	6333
RDPZCF [14][a]	500	2	0.07	0.14	1.2	0.8	C_{C1}=12 C_{C2}=0.5	4286	2857	8572	5714
SMFFC [5]	120	2	0.21	0.42	9	0.51	C_{C1}=4 (one)	2571	971	5143	1943
AFFC [6]	100	1.5	0.17	0.25	5.5	0.36	C_{C1}=5.4 C_{C2}=4	2200	564	3235	212
$ACBC_F$ [7]	500	2	0.162	0.324	1.9	1	C_{C1}=10 C_{C2}=3	2932	1543	5864	3086
TCFC [8]	150	1.5	0.03	0.045	2.85	1.035	C_{C1}=1.1 C_{C2}=0.92	9500	3450	14250	5175
This work[a]	150	1.5	0.014	0.021	1.6	0.65	C_{C1}=2.2 (one)	**11430**	**4543**	**17143**	**6964**

a. simulated
b. average value

IV. Conclusion

A compensation technique for three-stage OTAs with only the second stage inverting is developed. Design equations introducing the phase margin as main design parameter were carried out. The proposed compensation network exploits only one Miller capacitor, a resistor and the transistors of the basic OTA topology, thus optimizing power consumption. Simulation results on a 1.5-V three-stage amplifier driving a 150-pF load are given to confirm the advantages of the compensation strategy. The proposed amplifier is currently being fabricated using a standard 0.35-μm process supplied by AMS and measurement will be executed in the near future.

V. Appendix

Let $A_v(s)$ represent the open-loop transfer function of a generic three-stage amplifier

$$A_v(s) = A_0 \frac{1 + sb_1 + s^2 b_2}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + sa_1 + s^2 a_2\right)} \quad \text{(A1)}$$

The phase margin Φ is expressed by [1]

$$\Phi = 180° - \tan^{-1}\left(\frac{GBW}{\omega_{p1}}\right) - \tan^{-1}\left(\frac{a_1 GBW}{1 - a_2 GBW^2}\right) + \tan^{-1}\left(\frac{b_1 GBW}{1 - b_2 GBW^2}\right) \quad \text{(A2)}$$

Since $\omega_{p1} << GBW$, (A2) can be approximated by

$$\Phi = \tan^{-1}\left(\frac{1 - a_2 GBW^2}{a_1 GBW}\right) + \tan^{-1}\left(\frac{b_1 GBW}{1 - b_2 GBW^2}\right) \quad \text{(A3)}$$

Finally, denoting Φ_z the contribution of the numerator of (A1), the following relation is obtained

$$\tan\left(\Phi - \Phi_z\right) = \frac{1 - a_2 GBW^2}{a_1 GBW} \quad \text{(A4)}$$

Now let us develop a general expression for the stability of a generic three-stage amplifier whose open-loop transfer function can be expressed as (A1). Neglecting the zeroes, the closed-loop transfer function in unity-gain configuration is given by

$$A_{v,CL}(s) = A_0 \frac{1}{1 + s\frac{1}{GBW} + s^2 \frac{a_1}{GBW} + s^3 \frac{a_2}{GBW}} \quad \text{(A5)}$$

Since the order of the numerator of (A5) is less than the order of its denominator, the stability is determined only by the denominator [5], [9]. Therefore, by applying the Routh-Hurwitz stability criterion [10] on (A5), the following relation is carried out

$$a_1 > a_2 GBW \quad \text{(A6)}$$

It is worth noting that (A6), which states a condition for the unconditional stability, expresses a constraint on the maximum intrinsically achievable gain-bandwidth product of the amplifier.

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