A 0.9-V 33.7-ppm/°C 85-nW Sub-Bandgap Voltage Reference Consisting of Subthreshold MOSFETs and Single BJT

Lidan Wang, Chenchang Zhan, Junyao Tang, Yang Liu, and Guofeng Li

***Abstract*— A low temperature coefficient (TC) and high power supply ripple rejection (PSRR) CMOS sub-bandgap voltage reference (sub-BGR) circuit using subthreshold MOS transistors and a single BJT is presented in this brief. The proposed sub-BGR consists of a novel complementary-to-absolute-temperature (CTAT) voltage generator based on a scaled emitter-base voltage of a BJT, and an improved proportional-to-absolute-temperature (PTAT) voltage generator based on stacking of ΔV_{GS} of sub-V_{TH} MOSFETs. As the CTAT circuit achieves a reduced absolute value of the negative TC, the PTAT circuit achieves reduced power consumption without consuming a large chip area. The proposed sub-BGR circuit is implemented in a standard 0.18-μm CMOS process. Measured results show that the sub-BGR circuit can run with a supply voltage down to 0.9 V while the power consumption is only 85 nW. An average TC of 33.7 ppm/°C and a PSRR of better than −40 dB over the full frequency range are achieved.**

***Index Terms*— CMOS, high-power supply ripple rejection (PSRR), low power, sub-bandgap, subthreshold, voltage reference (VR).**

I. Introduction

Voltage references (VRs) compatible with CMOS processes are critical for modern analog and mixed-signal very large scale integration circuits and systems. The existing VRs can be roughly categorized as two types: one type related to the bandgap voltage of silicon or a fraction of it (i.e., sub-bandgap) using BJTs and resistors, the other one related to other factors such as MOS transistor threshold voltages and subthreshold parameters using MOS transistors (with or without resistors). Generally speaking, the bandgap or sub-bandgap references show relatively small process variations than CMOS VRs with relatively high power consumptions. Many research efforts have been attracted to develop low-power high-performance VRs such as the ones reported in [1]–[12]. However, it remains a design challenge to achieve satisfactory performances in all the major aspects. For example, although several low-power VRs have been developed in [1]–[7], the other performances such as temperature coefficient (TC) and power supply ripple rejection (PSRR) are not very good. In particular, the designs in [1]–[3] used the leakage current to generate the reference voltage, and the PSRR at low frequencies of these circuits are not very good. The circuits in [4] and [5] used the switched-capacitor voltage divider and 2× charge pump to achieve a division of the complementary-to-absolute-temperature (CTAT) voltage (V_{EB}) and low power supply voltage, but the TC is as large as 75 ppm/°C and the temperature range is limited to be only 0 °C–80 °C [4]. Furthermore, although curvature compensation techniques are used in [5], the measured PSRR was not reported. Subthreshold transistors are used to divide the CTAT voltage (V_{EB}) in [6] and [7], but the temperature range is −20 °C–120 °C [6] and the TC is also very high (114 ppm/°C [7]) which are not satisfactory.

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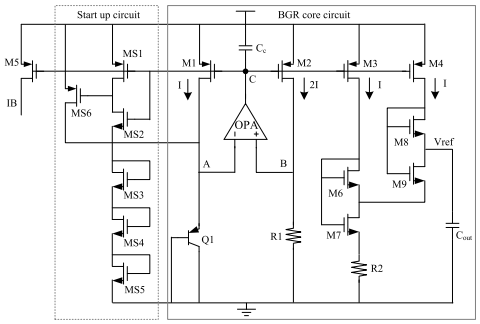

Fig. 1. Structure of the proposed CMOS sub-bandgap voltage reference.

For the CMOS VRs reported in [8]–[11], many concerns remain as well. The threshold voltages are used for the reference voltage, but the power consumptions are larger than 200 nW in [9]; the threshold voltage differences are used to generate the reference voltage in [10] and [11], but the TC is larger than 60 ppm/°C, in addition to the other nonsatisfactory performances. From the above analysis, the existing circuits can hardly achieve low power, small TC, and high PSRR simultaneously. Therefore, a new sub-bandgap voltage reference (sub-BGR) with only one BJT, two resistors, and subthreshold transistors is proposed in this brief, which uses the resistively divided V_{EB}-based CTAT voltage. Low TC with small variations and low power consumption are achieved, in addition to high PSRR and small line sensitivity. For the rest parts of this brief, the structure of the proposed sub-BGR is introduced in Section II. The PSRR calculations are described in Section III. The measured results are given in Section IV, and conclusions are followed in Section V.

II. Proposed Sub-Bandgap Voltage Reference

Fig. 1 shows the proposed sub-BGR circuit which uses a single parasitic vertical PNP BJT, i.e., Q1 to generate the CTAT voltage. The operational amplifier OPA shown in Fig. 2 enforces nodes A and B to have equal potential. As a result, the current I_R that flows through the resistor $R1$ is given by

$$I_R = \frac{V_{EB}}{R1} \tag{1}$$

where V_{EB} is the emitter-base voltage of Q1. As evidenced by (1), the voltage V_{EB} should be decreased and $R1$ increased in order to reduce the current I_R and hence the power consumption. However, increasing $R1$ would inevitably increase the area consumption of the chip. So the best way is to minimize the value of V_{EB}. Fortunately, decreasing the current of Q1 also decreases its emitter-base voltage. Fig. 3 shows the simulated voltage V_{EB} versus current through Q1 and V_{EB} decreases by around 60 mV if the current decreases by 10 times, expectable from the I–V behavior of a BJT. However, reducing V_{EB} also reduces the negative TC, or, increases the absolute

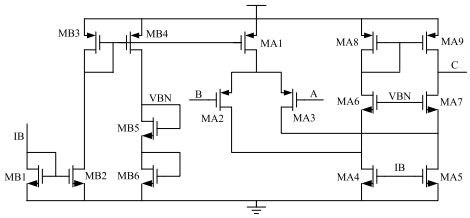

Fig. 2. Schematic of the OPA used in the proposed sub-BGR.

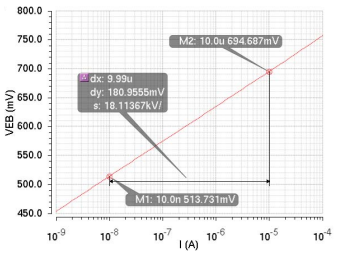

Fig. 3. Simulated emitter-base voltage ($V_{\rm EB}$) versus emitter current (I) of Q1.

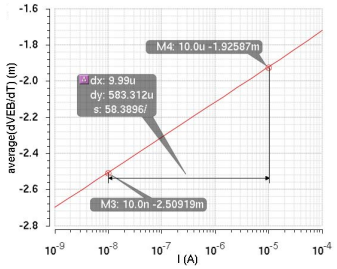

Fig. 4. TC of $V_{\rm EB}$ versus current I.

value of TC of $V_{\rm EB}$ [12], since the derivative of $V_{\rm EB}$ is as shown in

$$dV_{\rm EB}/dT = V_{\rm EB}/T - (4+m)V_T/T - E_g/qT \tag{2}$$

whereby m is the nonideality factor of Q1, V_T is the thermal voltage, E_g is the bandgap energy of silicon, and q the elementary charge.

Fig. 4 shows the negative TC of $V_{\rm EB}(K_N)$ versus current through Q1 and the absolute value of K_N increases by 0.2 mV/°C if the current decreases by ten times. The current through Q1 should not be too small so as not to increase the required positive TC of the proportional-to-absolute-temperature (PTAT) voltage. In this design, the current through Q1 is chosen to be around 13 nA to achieve a reasonable tradeoff between $V_{\rm EB}$ and its TC value. To optimize the power and area, the current I_R through *R1* is chosen to be two times of the current through Q1, and the resistance *R1* is about 20 MΩ. The transistors M1–M4 are current mirrors and the size of M2 is two times of M1 and M3–M4. So the current through *R2* is the same as that of *R1*. The voltage across *R2* is then given by

$$V_{R2} = \frac{R2}{R1}V_{\rm EB}. \tag{3}$$

Since $V_{\rm EB}$ has a negative TC and the TC of *R2* and *R1* are the same, $V_{\rm R2}$ also has a negative TC.

The PTAT voltage generator consists of transistors M6–M9 all of which work in the subthreshold region. The subthreshold drain current I_D of a MOSFET is an exponential function of its gate–source voltage $V_{\rm GS}$ and drain–source voltage $V_{\rm DS}$. For $V_{\rm DS} > 0.1$ V, drain current I_D is almost independent of $V_{\rm DS}$ and is approximately given by

$$I_D = K\mu C_{\rm OX}(\eta-1)V_T^2 \exp\left(\frac{V_{\rm GS}-V_{\rm TH}}{\eta V_T}\right) \tag{4}$$

where K is the aspect ratio ($=W/L$) of the transistor, μ is the carrier mobility, $C_{\rm OX}$ is the gate-oxide capacitance, V_T ($=k_BT/q$) is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge, $V_{\rm TH}$ is the threshold voltage of the MOSFET, and η ($=1+C_d/C_{\rm ox}$) is the subthreshold slope factor, respectively [7].

The drain–source voltage $V_{\rm DS}$ of transistors M6–M9 are designed to be larger than 0.1 V. The threshold voltages of M6 and M7 are the same, and the drain current of M7 is two times that of M6, so the drain–source voltage of M7 can be derived from (4) and given by

$$V_{\rm DS7} = V_{\rm GS7} - V_{\rm GS6} = \eta V_T \ln\left(\frac{2K_6}{K_7}\right). \tag{5}$$

In a similar way, the voltage $V_{\rm DS9}$ is given by

$$V_{\rm DS9} = V_{\rm GS9} - V_{\rm GS8} = \eta V_T \ln\left(\frac{K_8}{K_9}\right). \tag{6}$$

Therefore, the output voltage $V_{\rm ref}$ is given by

$$\begin{aligned} V_{\rm ref} &= \eta V_T \ln\left(\frac{2K_6K_8}{K_7K_9}\right) + \frac{R2}{R1}V_{\rm EB} \\ &= \frac{R2}{R1}\left[\eta V_T \ln\left(\frac{2K_6K_8}{K_7K_9}\right)\frac{R1}{R2} + V_{\rm EB}\right]. \end{aligned} \tag{7}$$

The voltage in the bracket of the second term is the bandgap voltage [7]. The value of *R2*/*R1* is less than 1 to get a sub-BGR.

The derivative of $V_{\rm ref}$ over temperature is given by

$$\frac{dV_{\rm ref}}{dT} = \eta\frac{k}{q}\ln\left(\frac{2K_6K_8}{K_7K_9}\right) + \frac{R2}{R1}K_N \tag{8}$$

where K_N is the negative TC of $V_{\rm EB}$. A zero T6C can be obtained since the two terms of (8) can cancel each other with proper design, and hence $V_{\rm ref}$ would be stable across a temperature variation range. The absolute value of the negative TC is reduced by *R2*/*R1* times compared with the traditional current-mode bandgap voltage reference [13]. So the PTAT compensation factor of (K_6K_8/K_7K_9) can also be reduced, which helps reduce the power and area of the PTAT circuit.

A. Process Variations

The generated $V_{\rm ref}$ of the proposed sub-BGR is associated with the process parameter η in the PTAT term, as can be seen from (7), which is not constant in actual devices and depends on the gate-oxide and depletion-layer capacitances [7]. Yet, the variation of η is not big [1]. The TC of $V_{\rm ref}$ is also related to the process parameter η as seen from (8). The effects of parameter η on $V_{\rm ref}$ and TC of $V_{\rm ref}$ are similar, so the trimming methods for $V_{\rm ref}$ and TC of $V_{\rm ref}$ can be similar. Moreover, the process variation of $V_{\rm EB}$ is very small, so the output voltage $V_{\rm ref}$ variation is very small. Figs. 5 and 6 show the Monte-Carlo simulation results of $V_{\rm ref}$ and TC without trimming. The average $V_{\rm ref}$ and standard deviation are 463.8 and 1.6 mV, respectively, leading to a σ/μ of 0.35%. The average TC and standard deviation are 36.8 and 7.5 ppm/°C, respectively. The variation of TC is relatively large due to the mismatches, so a trimming circuit is used to achieve a low-TC reference voltage $V_{\rm ref}$.

B. DC Offset of OPA

Considering the offset voltage $V_{\rm os}$ (modeled at the –ve input) of the OPA, the proposed sub-BGR in Fig. 1 operates under the condition of

$$V_B = V_A + V_{\rm os}. \tag{9}$$

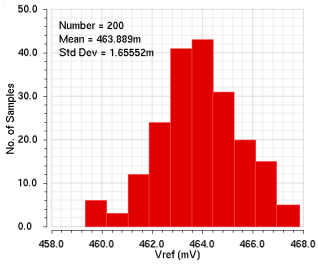

Fig. 5. Monte-Carlo simulation result of V_{ref} without trimming.

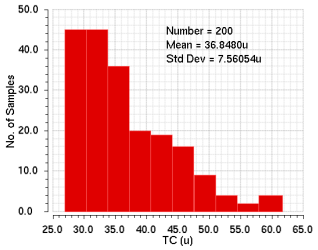

Fig. 6. Monte Carlo simulation result of TC without trimming.

TABLE I
DEVICE SIZES OF THE PROPOSED CIRCUIT

Device	W/L (μm/μm)	Device	W/L (μm/μm)	Device	W/L (μm/μm)
M1	4/10	MS4	2/10	MB1	2/10
M2	2×4/10	MS5	2/10	MB2	2/10
M3	4/10	MS6	2/10	MB3	2/10
M4	4/10	MA1	4×2/10	MB4	2/10
M5	1/18	MA2	2×4/4	MB5	4/10
M6	32×1/12	MA3	2×4/4	MB6	4/10
M7	1/12	MA4	4×2/10	Q1	10/10
M8	17×1/12	MA5	4×2/10	R1	3000×1.5/9
M9	1/12	MA6	6/8	R2	857×1.5/9
MS1	4×4/1	MA7	6/8	C_c	9×24/24
MS2	2/8	MA8	4/8	C_{out}	11×25/25
MS3	2/10	MA9	4/8		

The total V_{ref} including the V_{os} is then given by

$$V_{\text{ref}} = \eta V_T \ln\left(\frac{2K_6K_8}{K_7K_9}\right) + \frac{R2}{R1}V_{\text{EB}} + \frac{R2}{R1}V_{\text{os}}. \tag{10}$$

As can be found out from (10), the effect of V_{os} is reduced by *R2/R1* times compared with the traditional bandgap voltage [13], since *R2/R1* is less than 1. The offset voltage can still affect the V_{ref} and TC of V_{ref} if V_{os} is changing with the temperature, so the trimming circuit also helps calibrate the effects caused by the variations. The minimum supply voltage of the proposed BGR is given by

$$V_{\text{DD,min}} = V_{\text{EB}} + V_{\text{GS}} + V_{\text{OV}} \tag{11}$$

where V_{GS} is the gate-source voltage of input transistor in OPA, and V_{OV} is the overdrive voltage of MA1 in OPA. All of the transistors in OPA are working in the subthreshold region to reduce the minimum supply voltage as well as power consumption. In this design, a minimum supply voltage of 0.9 V is achieved. The device parameters of Figs. 1 and 2 are listed in Table I.

C. Trimming Circuit

Trimming on the PTAT voltage, rather than the CTAT one, is adopted to reduce the area consumption of the circuit. The designed trimming range is three to four times of the Monto Carlo simulation results to cover the process and mismatch variations with certain margins. Fig. 7 shows the trimming circuit. Transistor M6 in Fig. 1 is used for trimming to make sure that the V_{DS} of M6–M9 is larger than 0.1 V. There are 6 bits S0–S5 used for trimming. When the switch is on, the trimming transistor is connected to the circuit and used as M6 to increase the TC of the PTAT voltage. On the other hand, the trimming transistor is disconnected from the circuit to decrease the TC of PTAT if the switch is off. When the process is at the TT corner, the control transistor is disconnected from the circuit to decrease the TC of PTAT if the switch is off. When the process is at the TT corner, the control bits S0–S5 are 000001. The final control voltages of these switches used to trim the TC of V_{ref} depend on the variations of V_{ref}.

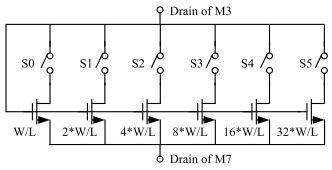

Fig. 7. Trimming circuit of M6.

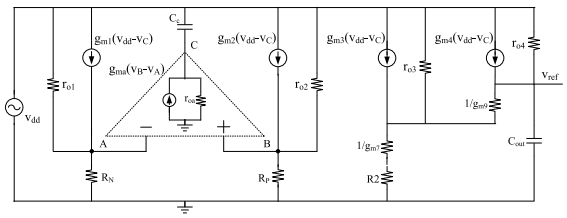

Fig. 8. Small-signal model for PSRR calculation.

III. PSRR ANALYSIS

Fig. 8 shows the small-signal model for the PSRR analysis, whereby R_P and R_N are equal to *R1* and $1/g_{\text{mQ}}$, respectively; g_{mQ} is the trans-conductance of Q1; g_{ma} and r_{oa} are the trans-conductance and output resistance of the op-amp, respectively; C_c is the compensation capacitor between node C and the power supply VDDA; g_{m1}–g_{m4} and r_{o1}–r_{o4} are the trans-conductance and the output resistance of M1–M4, respectively; g_{m7} and g_{m9} are the transconductance of M7 and M9. Transistors M6 and M8 make voltage source followers, so their output resistances are neglected. The expression of PSRR is defined by $20\log_{10}(\upsilon_{\text{ref}}/\upsilon_{\text{dd}})$. Since $g_{\text{m2}} = 2g_{\text{m1}} = 2g_{\text{m3}} = 2g_{\text{m4}}$ as can be derived from (4), the value $\upsilon_{\text{ref}}/\upsilon_{\text{dd}}$ can be obtained based on the small-signal model of Fig. 8 and the result is approximately expressed by

$$\begin{aligned}
\frac{\upsilon_{\text{ref}}}{\upsilon_{\text{DD}}} &= \frac{2R_4(1+g_{m4}r_{o4})}{(r_{o4}+R_4)(1+g_{\text{ma}}r_{\text{oa}}(g_{m2}R_B - g_{m1}R_A))} \\
&\quad \cdot \frac{(1+s/z_1)}{(1+s/p_1)(1+s/p_2)} \\
R_4 &= R2 + 1/g_{m7} + 1/g_{m9} \quad R_B = R_P \parallel r_{o2} R_A = R_N \parallel r_{o1} \\
z_1 &= \frac{1+g_{m4}r_{o4}}{r_{\text{oa}}C_c} \quad p_1 = \frac{1}{C_{\text{out}}(r_{o4} \parallel R_4)} p_2 \\
&= \frac{g_{\text{ma}}(g_{m2}R_B - g_{m1}R_A)}{C_c}
\end{aligned} \tag{12}$$

whereby the poles and zeros of the PSRR function are given by separated terms. The PSRR improvement over the traditional compensation techniques is due to the extended zero z_1 frequency due to C_C [14]. Fig. 9 shows the simulated prelayout PSRR of the circuit, with the pole and zero frequencies marked on the plot. The additional zeros and poles are caused by the input capacitances of OPA which are neglected here.

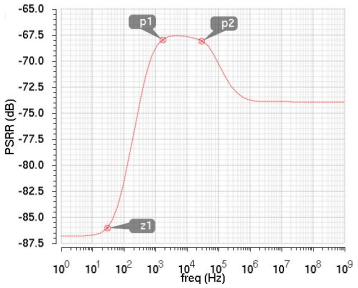

Fig. 9. Simulated prelayout PSRR of the proposed sub-BGR.

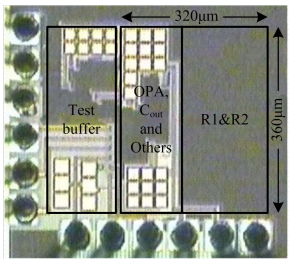

Fig. 10. Chip microphotograph.

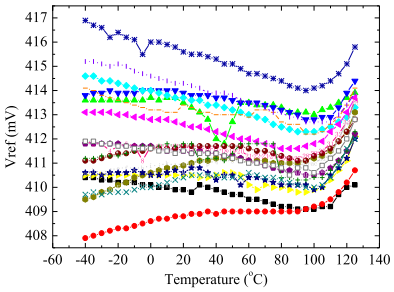

Fig. 11. Measured V_{ref} versus temperature with one time trimming.

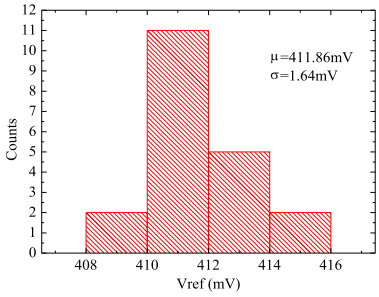

Fig. 12. Measured V_{ref} at room temperature of 20 chips.

IV. Measurement Results

The proposed sub-BGR is designed and fabricated in a standard 0.18-μm CMOS process. Fig. 10 shows the chip photograph and it takes an active area of 360 × 320 μm^2. The 20 samples from the same run have been measured. Fig. 11 shows the measured one-time-trimmed output voltage V_{ref} versus temperature for a range of −40 °C–125 °C. To obtain these results, a random chip is selected and trimmed to minimize the TC. Then, the same trimming code is used for the rest of the chips, i.e., the other 19 chips have not been trimmed or optimized. Fig. 12 shows the measured output voltage V_{ref} at room temperature for the 20 chips. The average value and standard deviation are 411 and 1.64 mV, respectively, and the variation coefficient σ/μ value is as small as 0.39%. The output voltage differences between the simulated and measured results in Figs. 5 and 11 were introduced by the process and mismatch variations. Fig. 13 shows the TC distribution for the 20 chips, and the

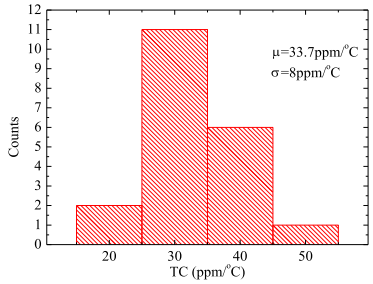

Fig. 13. Measured TC distribution of 20 chips.

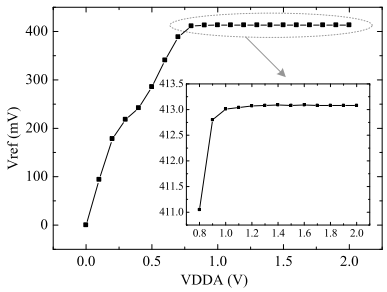

Fig. 14. Measured line sensitivity of the proposed sub-BGR.

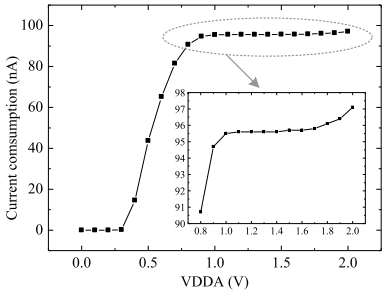

Fig. 15. Measured current consumption versus VDD of the proposed sub-BGR.

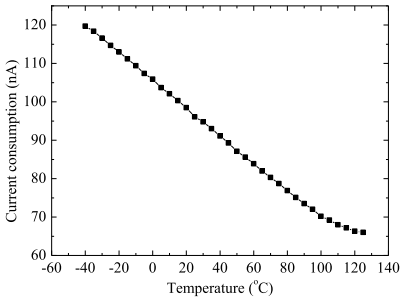

Fig. 16. Measured current consumption versus temperature when VDDA = 1.8 V.

average value and standard deviation of TC are 33.7 and 8 ppm/°C, respectively.

Fig. 14 shows the measured output voltage versus the power supply from 0 to 1.8 V and the line sensitivity is 0.06%/V for 0.9–1.8 V supply. Fig. 15 shows the current consumption versus the power supply voltage, and the power consumption is 85 nW when the VDDA is 0.9 V. Fig. 6 shows the measured current consumption versus temperature when VDDA is 1.8 V, and the current decreases by about 60 nA when the temperature increases from −40 °C to 125 °C, since the bias current I_R has a negative TC. This is advantageous over the traditional designs, which usually have roughly exponentially increased power consumptions when the temperature increases [3], [8], [11]. The relatively small current variation with

TABLE II
MEASURED PERFORMANCES COMPARISON WITH OTHER WORKS

	This work	[1] ISSCC 2015	[3] TVLSI 2017	[4] ISSCC 2015	[6] VLSIC 2017	[7] JSSC 2013	[8] JSSC 2012	[11] TVLSI 2015
CMOS technology(nm)	180	350	180	130	180	180	130	180
Type	Sub-BGR	BGR	CMOS VR	Sub-BGR	Sub-BGR	Sub-BGR	CMOS VR	CMOS VR
Supply voltage (V)	0.9-2	1.4-3	1.1-1.8	0.5-1.5	0.8-1.6	0.7-1.8	0.5-3	0.15-1.8
Power consumption (nW)	85	29	4.6	32	37	52.5	0.002	0.026
VREF (mV)	411.86	1176	755	500	477	548	176	17.69
Variation coefficient σ/μ (%)	0.39	0.2	0.64	0.6	0.89	1.05	0.72	1.6
Temperature Range (°C)	-40~125	-10~110	-15-140	0-80	-20~120	-40~120	-20~80	0~120
Average TC (ppm/°C)	33.7	15	34	75	51.2	114	62	1462.4
Line Sensitivity (%/V)	0.06	0.198	0.28	2	0.04	N/A	0.033	2.03
PSRR (dB)								
@10Hz	-61	N/A	-9	-40	N/A	-75	-50.4	-64*
@100Hz	-44	N/A	N/A	N/A	-50	-56	-51.5	-64*
@1MHz	-46	N/A	-47	N/A	-19	-8.7	-62	-115*
Area (mm^2)	0.11	0.48	0.059	0.0264	0.034	0.024	0.0013	0.0012

*represents the simulation results

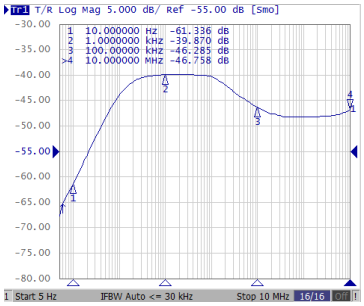

Fig. 17. Measured PSRR of the proposed sub-BGR.

temperature can also help with reducing the TC variation of the PTAT voltage. Fig. 17 shows the measured PSRR of the proposed circuit, and the PSRR is −61, −40, and −46 dB at 100 Hz, 10 KHz, and 1 MHz, respectively. The differences between the measured and simulated PSRRs are mainly due to the reduction of zero z_1 [14], caused by the joint effects of $g_{m4}r_{o4}$ variation, parasitic capacitance at node C, and output resistance of the OPA. A performance summary and comparison with the state-of-the-art works is listed in Table II. Compared to the works of CMOS voltage reference or sub-BGR circuits, this design achieves better balanced performances in terms of variation coefficient, temperature range, TC, and PSRR. It is worth mentioning that, the relatively large chip area in this implementation is mainly caused by the area of resistors *R1* and *R2* which takes 0.08 mm^2, since the width of these resistors is designed to 1.5 μm. The width can be reduced to achieve smaller area with larger variation and mismatch of the resistance values. For example, if the width of *R1* and *R2* is reduced from 1.5 to 1 μm, then the total active area will be reduced from 0.11 to 0.05 mm^2.

V. CONCLUSION

A 0.9-V 33.7-ppm/°C sub-BGR generator implemented in 0.18-μm CMOS process has been presented. The proposed design employs MOS transistors working in subthreshold regions to achieve low voltage and low power operations. The proposed CTAT circuit consists of a vertical PNP BJT and two resistors to reduce the power. The improved PTAT circuit is made up by two cascaded sub-PTAT circuits with subthreshold transistors to reduce the power consumption without consuming large chip area. The PSRR computational formulas have been derived from the small signal model, which can help us optimize the circuits. The measured results verified the good performances, which makes the proposed sub-BGR circuit very attractive for low-power applications.

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