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A 68-nW novel CMOS sub-bandgap voltage reference circuit

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ABSTRACT

This paper proposes a CMOS sub-bandgap reference (sub-BGR) circuit without resistors for ultra-low power applications. The BGR core circuit consists of a vertical PNP bipolar transistor, a temperature-compensation amplifier and a Proportional to Absolute Temperature (PTAT) voltage generator. The PTAT voltage generator consists of four p-type transistors and generates a positive temperature dependent voltage, which compensates for the negative temperature dependent base-emitter voltage in a PNP bipolar transistor. The circuit generates a sub-bandgap voltage of silicon. The sub-BGR is fabricated with 65-nm standard CMOS process with an area of 400 μm × 80 μm. Experimental results demonstrate that this sub-BGR circuit can generate a 202.8 mV reference voltage with a power consumption of 68 nW.

1. Introduction

Nowadays, an Internet of Things (IoT) system, such as the smart intelligent sensor, requires life-long operating [1]. Therefore, the power dissipation of Integrated Circuit (IC) becomes a critical aspect for IoT applications. On the other hand, compact circuit area is always preferable as it allows high-integration and reduces the cost.

Voltage reference is one of the most important circuits for the ICs used in IoT system. The Bandgap Reference (BGR) has been widely applied as the voltage reference because of its low PVT shift. Conventionally, a BGR circuit requires the use of passive resistors, and nine or more bipolar transistors, which consume large die size [2]. When a BGR circuit works in nano-ampere current levels, large-value resistors are needed to generate an appropriate voltage drop, further increasing the die size needed. Therefore, traditional methods are not practical in nano-watt power application. In recent studies, voltage references operated at nano-watt power dissipation were presented [3,4,5,6]. However, [3,4] are not compatible with the standard CMOS process. [5] needs extra clock generator circuit which consumes additional power and die area. [6] is implemented with the standard CMOS process but not area-efficient.

To address the severe trade-offs between power dissipation and die size in CMOS technologies, we propose a resistor-less sub-BGR circuit with nano-watt power operation capability and an efficient die size.

2. Architecture

The sub-threshold current I_{sub} of a MOS transistor can be expressed as

$$I_{sub} = \mu c_{ox}(m-1)\frac{W}{L}V_T^2 \exp\left(\frac{V_{GS}-V_{TH}}{mV_T}\right)\left(1-\exp\left(\frac{-V_{ds}}{V_T}\right)\right) \quad (1)$$

While μ is the carrier mobility, c_{ox} is the gate–oxide capacitance, W and L are transistor channel width and length, respectively. V_T is the thermal voltage, m is the subthreshold slope factor [7].

In this design, $V_{ds} > 4V_T$, so term $\exp\left(\frac{-V_{ds}}{V_T}\right)$ can be ignored.

Then equation (1) can be simplified as

$$I_{sub} = \mu c_{ox}(m-1)\frac{W}{L}V_T^2 \exp\left(\frac{V_{GS}-V_{TH}}{mV_T}\right) \quad (2)$$

Fig. 1 shows the architecture of the BGR circuit we proposed. The circuit consists of a PNP bipolar transistor, a temperature-compensation amplifier and a PTAT voltage generator. Different from Ref. [6] which needs a nano-ampere current reference circuit, this work does not need any extra bias circuit. The output reference voltage is the sum of the Complementary to Absolute Temperature (CTAT) voltage and PTAT voltage.

$$V_{ref} = \alpha V_{be} + \beta V_T \quad (3)$$

If α and β are designed by suitable ratio, then output reference is temperature independent.

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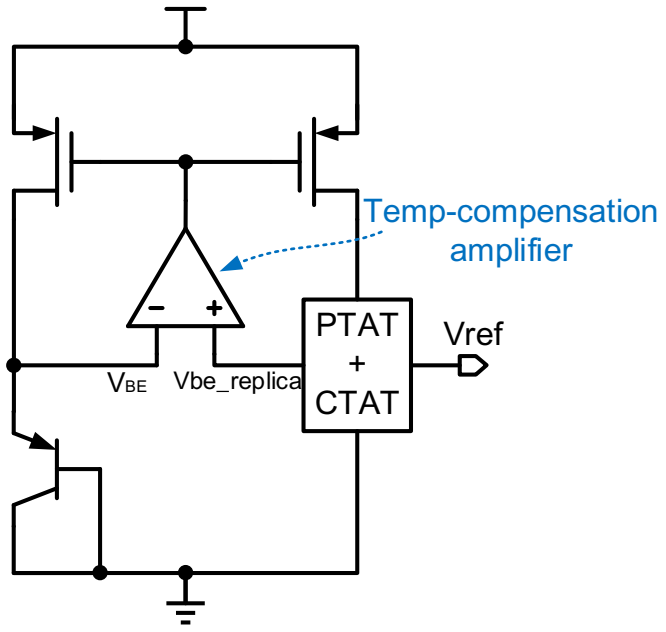

Fig. 1. Block diagram of sub-BGR architecture.

In real industry practice, temperature compensation trim is necessary for yield improvement, so an extra compensation mechanism, a temp-compensation amplifier, is introduced to realize the trim function. So the final output reference voltage is expressed as

$$V_{ref} = \alpha V_{be} + \beta V_T + \gamma V_{trim} \tag{4}$$

Fig. 2 shows detailed temp-compensation amplifier structure. Its DC gain is 24 dB and the phase margin is 50° at worst case. It was designed with unbalanced PMOS mirror ({P36 + P50||P51||P52||P53} versus P35). P50, P51, P52, P53 are PMOS transistors, the sizes of which increase progressively at 2× multiple interval, by which we get adjustable [1×, 15×] trim current. Gates of these PMOS transistors are connected to their sources, so they all work at the sub-threshold regions [3].

The compensation current I_c can be written as

$$I_c = \mu c_{ox}(m-1)\frac{W}{L_{p5x}}V_T^2 \exp\left(\frac{-V_{TH}}{mV_T}\right) \tag{5}$$

$\frac{W}{L_{p5x}}$ means combinations of P50–P53 in Fig. 2, represents [1×, 15×] compensation current.

P16 works under subthreshold, so the current passes through P16:

$$I_{sub,p16} = \mu c_{ox}(m-1)\frac{W}{L}V_T^2 \exp\left(\frac{V_{GS,P16} - V_{TH}}{mV_T}\right) = I_s \exp\left(\frac{V_{GS,P16}}{mV_T}\right)$$

And now we have compensation current I_c, then

$$I_{sub,P16} = I_{sub,P17} + Ic$$

And

$$V_{SG17} = mV_T \ln\left(\frac{I_{sub,P17}}{Is}\right)$$

$$V_{SG16} = mV_T \ln\left(\frac{I_{sub,P17} + Ic}{Is}\right)$$

Then the input offset can be expressed as

$$V_{offset} = V_{cp} - V_{be} = V_{gate,P17} - V_{gate,P16} = mV_T Ln\left(1 + \frac{Ic}{I_{sub,P17}}\right) \approx mV_T\left(\frac{I_c}{I_b/2}\right) \tag{6}$$

It is obvious that temp-compensation amplifier adds extra positive voltage. Therefore, the temperature curve of Vref is calibrated.

P57, P56, P55, P54 are 1.8 V PFETs (their gates are drawn with thick lines in Fig. 2) used as current switches. 1.8 V PFET has much bigger threshold voltage and negligible drain-to-source leakage current (aA level) if it's cut-off, so compensating current can be ignored. If we insist on using the core PFET as switch, leakage current or compensation current (at pA or nA level) from P50/P51/P52/P53 can still flow through it, then switch function is useless. S3, S2, S1, S0 are control bits from control logic.

So the final output reference voltage can be rewritten as

$$V_{ref} = \alpha V_{be} + \beta V_T + \gamma mV_T\left(\frac{I_c}{I_b/2}\right) \tag{7}$$

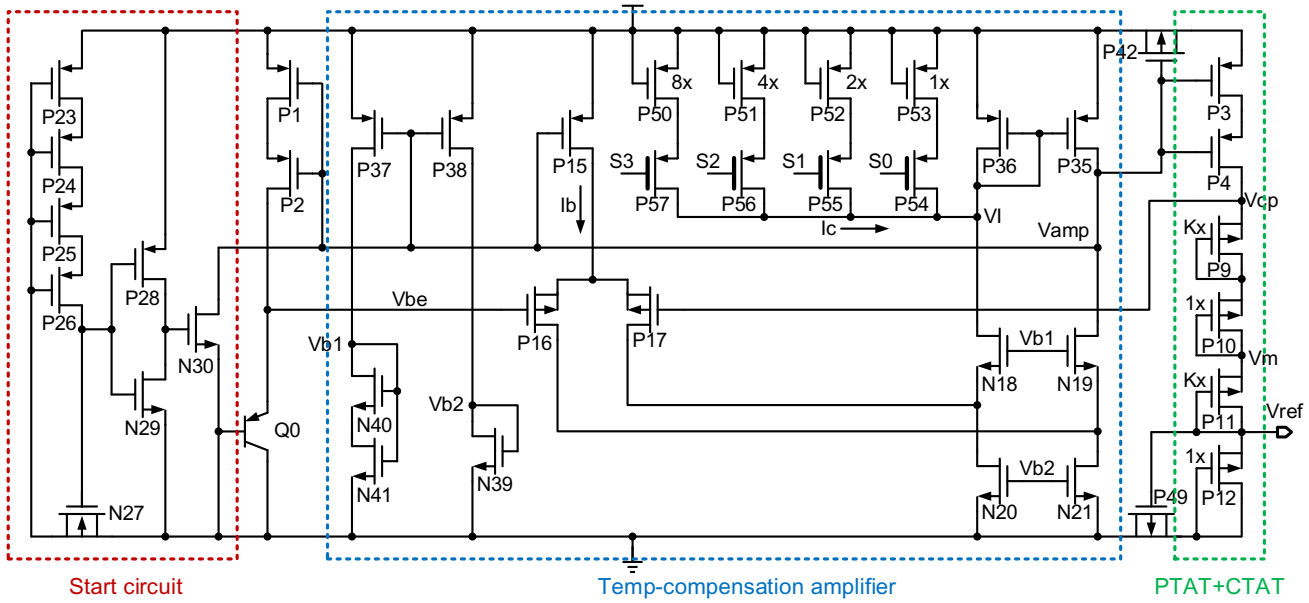

Fig. 2. Proposed sub-bandgap voltage reference (sub-BGR).

Fig. 3 shows the simulation results of Ic temperature compensation trim effect on Vref.

3. Circuit implementations

Fig. 2 shows the transistor-level diagram for the proposed sub-BGR, all PMOS transistors work in sub-threshold region.

For the PTAT portion, the sizes of P9 and P11 are K times those of P10 and P12, and P9/P10/P11/P12 are serial, so

$$I_{mp11} = \mu c_{ox}(m-1)\frac{KW}{L}V_T^2 \exp\left(\frac{V_m - V_{ref} - V_{THP}}{mV_T}\right)$$

$$I_{mp12} = \mu c_{ox}(m-1)\frac{W}{L}V_T^2 \exp\left(\frac{V_{ref} - V_{THP}}{mV_T}\right) \quad (8)$$

Since $I_{mp11} = I_{mp12}$, V_{ref} can be expressed as

$$V_{ref} = \frac{V_m}{2} + \frac{mV_T \ln K}{2} \quad (9)$$

where V_m is half of V_{cp}, and $V_{cp} = V_{be} + V_{offset}$.

Substitute (6) into (9), we get

$$V_{ref} = \frac{V_{be}}{4} + \frac{mV_T \ln K}{2} + \frac{mV_T\left(\frac{I_c}{I_b/2}\right)}{4} \quad (10)$$

Equation (10) is the similar principle as regular bandgap generator. In general, TC (Temperature Coefficient) of V_{be} is −1.5 mV/°C, and TC of V_T is 0.086 mV/°C. By adjust K properly (K = 80 in this work), a low temperature-coefficient voltage can be obtained. The calibration term $mV_T\left(\frac{I_c}{I_b/2}\right)/4$ in equation (10) is used to fine-tune the output curve. Moreover, the term helps reduce K requirement of "PTAT + CTAT" portion, it can greatly reduce the die size.

More precisely, temp-compensation amplifier contributes 52 mV offset in typical cases. As a result, when Vbe is about 653 mV, the Vcp is 705 mV, and the amplifier output voltage is about 0.98 V with a 1.2 V supply.

For "Start circuit" portion in Fig. 2., its operating flow is: at the beginning of power-on, N27's gate voltage is ~0 V (Because we pull-down it at power-off state, switch transistor is not drawn in Fig. 2), then drain of N30 is pulled low, after ~ 30 ns (worst case) or longer, gate of N27 is charged to power level, then N30's gate is ~0 V, so start-up circuit will not impact core circuit.

Take account power consumption, the currents of P50–P53 are 2.3 nA, 1.2 nA, 585 pA, 293 pA, cascade of P9–P11 consumes about 15 nA, Q0 consumes about 15 nA, and the total power consumption of the temp-compensation amplifier is 30 nA.

4. Results

500 iterations of Monte-Carlo simulation have been implemented to verify the process variation effects. As shown in Fig. 4., the output reference voltage standard deviation of V_{ref} is 3.80 mV. Process variation affects bipolar and FET heavily, so compensation current trimming is very practical to realize better accuracy.

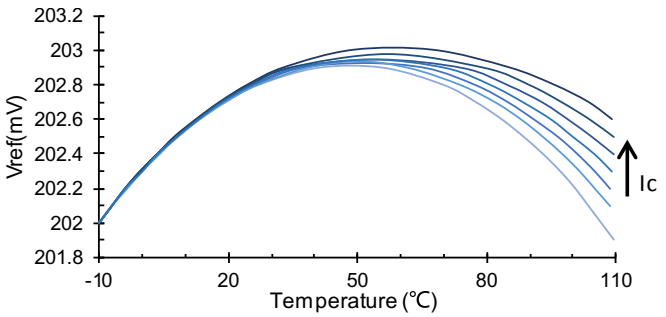

Fig. 3. Ic temperature trim effect on Vref.

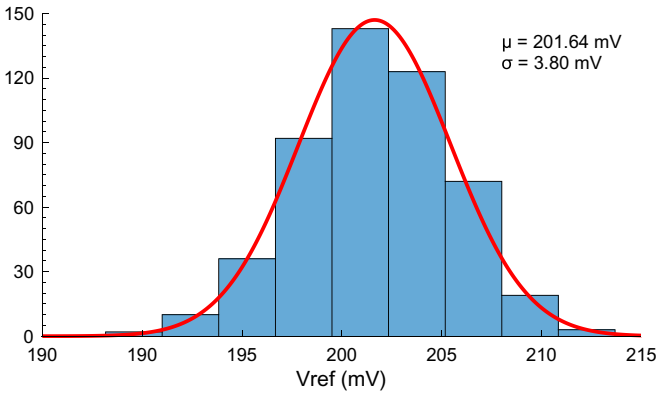

Fig. 4. Summary of 500 iterations of Monte-Carlo simulation.

Fig. 5. Chip micrograph.

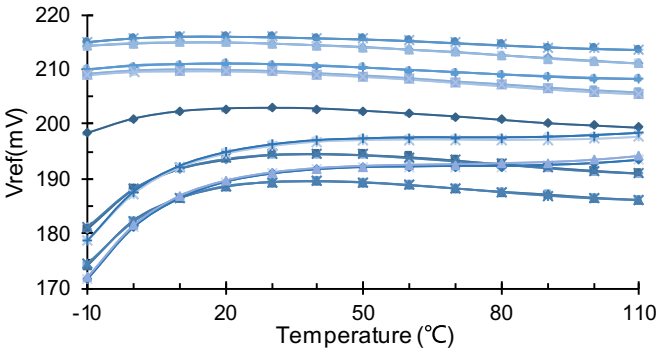

Fig. 6. Measured Vref vs. temperature of 17 chips.

Prototype chips were fabricated with 65-nm standard CMOS process. Fig. 5 shows the chip micrograph. The area of the sub-BGR circuit is 400 μm × 80 μm.

Fig. 6 shows measured V_{ref} curve vs. temperature from 17 chips. Output reference voltage is around 202.8 mV and TC is 36.6 ppm/°C. 17

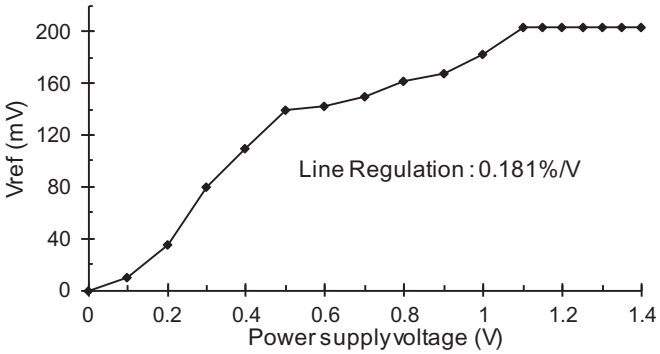

Fig. 7. Measured line regulation.

Table 1
Comparisons of performance of BGR.

	This Work	[2]	[3]	[4]	[5]	[6]	
Process (nm)	65	350	180	350	130	180	
Type	Sub-BGR	BGR	BGR	BGR	BGR	BGR	Sub-BGR
Temp Range (°C)	−10–110	−15–150	0–110	−10–110	0–80	−40–120	
VDD(V)	1.2	2.5	1.8	2.5	/	1.2–1.8	0.7–1.8
Power (nW)	68@R	95000	9.3	28.7@R	32	100@R	52.5@R
Vref(V)	0.2028	0.6177	1.238	1.176		1.09	0.548
TC (ppm/°C)	36.6	3.9	26	12.75	75	147	114
Line Reg (%/V)	0.181	0.039	0.08	0.198	/	/	/
Active Area (mm^2)	0.032	0.1019	0.055	0.48	0.0264	0.0294	0.0246

chips have been tested with ±10% supply voltage variations to assure robust. Lab results show some variations under different supplies caused by BJT base emitter voltage variations.

Fig. 7 shows measured V_{ref} curve vs. power supply and line regulation is calculated.

Table I compares performance with previously reported state-of-the-art BGR circuits [2,3,4,5,6]. The power dissipation of this work is 68 nW. This work shows a smaller area than most of prior works, and is fully compatible with standard CMOS process. Measurement results show that the proposed circuit is a good candidate as the voltage reference for most ultra-power IoT applications.

5. Conclusion

We propose a standard CMOS-compatible sub-BGR circuit with just one bipolar transistor and no resistors for nano-watt power IoT application. The sub-BGR circuit uses a base-emitter voltage of a PNP bipolar transistor. To generate PTAT voltage, sub-threshold p-type transistors are used in the sub-BGR circuit. The power dissipation of sub-BGR core circuit is 68 nW. The proposed circuit can be used as voltage reference circuit for power-aware and area-sensitive IoT applications.

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