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A 0.6V-Minimum-Supply, 23.5ppm/°C Subthreshold CMOS Voltage Reference with 0.45% Variation Coefficient

Chenyu Huang, *Student Member, IEEE*, Chenchang Zhan, *Member, IEEE*, Linjun He, Lidan Wang and Yang Nan

***Abstract*—In this paper, a low-voltage low-temperature-coefficient (TC) subthreshold CMOS voltage reference (CVR) is presented. The proposed CVR employs the ΔV_{GS} of different-threshold and same-threshold NMOS transistor pairs to generate the complementary-to-absolute-temperature (CTAT) and proportional-to-absolute-temperature (PTAT) voltages, respectively. Low TC with small variations and high power supply ripple rejection (PSRR) are achieved. The proposed design is fabricated in a standard 0.18-μm CMOS process. It measures an average reference voltage of 218.3 mV with a deviation of 0.97 mV and variation coefficient of 0.45%. It achieves an average TC of 23.5ppm/°C for a temperature range of -40 to 125°C. The measured PSRR is -66.4 dB, -42.4 dB and -42.3 dB at 10 Hz, 1k Hz and 10M Hz, respectively. The measured line sensitivity (LS) is 0.40%/V for 0.6 V to 2.0 V supply. The consumed power is 30.5 nW at 0.6 V supply.**

***Index Terms*—Subthreshold, CMOS voltage reference, supply voltage**

I. Introduction

VOLTAGE references (VRs) are indispensable components of many electronic devices. They are widely used for low drop-out regulators (LDOs), amplifiers, and many other analog circuits [1]. VRs are required to generate accurate and stable reference over wide temperature with low power consumptions. Bandgap voltage references (BGRs), which generate references related to the silicon bandgap energy or a fraction of it, and CMOS voltage references (CVRs), which have references related to MOS transistor parameters such as threshold voltage, are the two generally considered VR types [2].

The conventional BGRs have been widely utilized in power management integrated circuits (PMICs), which can achieve small process variations, but can hardly achieve low power consumptions [3-6], making it difficult to be employed in the ultra-low-power applications such as internet-of-things (IoTs). As for the previously developed design of CVRs, either higher supply voltage is required for the case of CMOS transistors working in strong inversion [7], or the working temperature range is quite limited for the ultra-low-power CVRs [8-12]. All these existing works cannot simultaneously achieve low TC, small variations, low power and low voltage operations.

In this paper, we propose a low-voltage CVR circuit which has all MOS transistors working in subthreshold region. The low temperature sensitivity is realized through the subthreshold characteristics between drain current and gate-source voltage. Specifically, different-threshold and same-threshold NMOS pairs in subthreshold regions are employed to generate the complementary-to-absolute-temperature (CTAT) and proportional-to-absolute-temperature (PTAT) voltages respectively. Low TC with small variations is achieved. Moreover, an operational amplifier and compensation capacitor are used to improve the line sensitivity and power supply ripple rejection (PSRR). The rest of this paper is organized as follows: Sec. II presents the design principle and implementation of the proposed circuit. The testing result and comparison with prior works are shown in Sec. III. Sec. IV draws the conclusions.

II. Proposed Voltage Reference

Fig. 1 shows the schematic of the proposed CVR circuit (start-up circuit not shown). Transistor M_5 is a high-voltage (i.e., 3.3 V in this work) IO device that has a high threshold voltage, while all the other transistors are the standard low voltage (i.e., 1.8 V) core devices. The reference is implemented by the summation of the drain-source PTAT voltage of M_7, V_{ds7}, and the CTAT voltage of resistor R_2. Working in subthreshold region with $V_{DS} \geq 0.1$ V, the current I_D is expressed as [4]

$$I_D = KI_0 e^{\frac{V_{GS}-V_{TH}}{\eta V_T}} \quad (1)$$

where K = W/L is the aspect ratio of the transistor, $I_0 = \mu_0 C_{ox}(\eta-1)V_T^2$ is a process-dependent parameter, in which μ_0 and C_{ox} are the carrier mobility and gate-oxide capacitance per unit area, respectively; η is the subthreshold slope factor, and $V_T = k_B T/q$ represents the thermal voltage, where k_B, T and q are the Boltzmann constant, absolute temperature and the elementary charge, respectively. V_{GS} is the gate-source voltage of the transistor, and V_{TH} is its threshold voltage [4]. To simplify the analysis, η is considered the same for different transistors. The negative input terminal of the amplifier, i.e., V_N, can be derived from (1) as

This work was in part supported by the National Natural Science Foundation of China (NSFC) under grant 61604067 and the Shenzhen Science and Technology Innovation Committee (STSTI) under grants JCYJ20160429191518358 and JCYJ20160530191008447.

The authors are with the Department of Electrical and Electronic Engineering, the Southern University of Science and Technology (SUSTech), Shenzhen, China (e-mail: huangcy@mail.sustc.edu.cn, zhancc@sustc.edu.cn, helj@mail.sustc.edu.cn, wangld@sustc.edu.cn, nany@mail.sustc.edu.cn).

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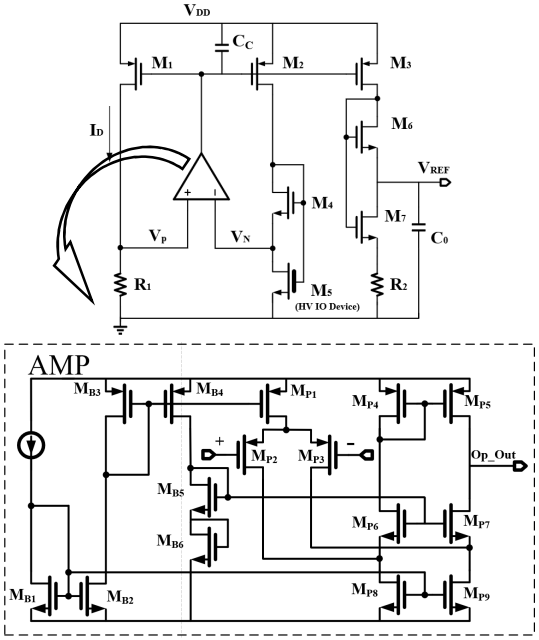

Fig. 1 Schematic of the proposed CVR circuit (without start-up circuit)

$$V_N = V_{GS5} - V_{GS4} = V_{TH5} - V_{TH4} + \eta V_T \, l\, n\left(\frac{K_4 I_{O4}}{K_5 I_{O5}}\right) \quad (2)$$

in which V_{THi} and K_i represent the threshold voltage and aspect ratio of transistor M_i, respectively. As mentioned above, V_{TH5} is higher than V_{TH4} at the same temperature, while they both decrease with temperature. Fig. 2 shows the threshold voltages of M_5 and M_4 vs. temperature, and their difference could generate the CTAT voltage component. Moreover, K_4 = 3 μm / 8.8 μm in this design is smaller than K_5 = 2 μm / 3 μm and the parameter ratio I_{04}/I_{05} could be omitted from the discussion of (1), therefore the generated V_N is a CTAT voltage.

Replicated to M_1 branch by the feedback loop, V_P generates the CTAT current through resistor R_1, which will be mirrored through M_3 to M_6, M_7 and R_2. Similar to (2), the drain-source voltage of M_7, i.e., V_{DS7}, could be derived as

$$V_{DS7} = V_{GS7} - V_{GS6} = V_{TH7} - V_{TH6} + \eta V_T \, l\, n\left(\frac{K_6 I_{O6}}{K_7 I_{O7}}\right) \quad (3)$$

Due to the same type of M_6 and M_7, which are both deep-n well transistors with each one's source terminal connected to the corresponding well-tie to eliminate the body effect, the threshold difference between the two transistors $V_{TH7} - V_{TH6}$ could be neglected. Therefore, V_{DS7} is a PTAT voltage by sizing M_6 larger than M_7. The equation of voltage reference (V_{REF}) is then expressed as

$$V_{REF} = A[\Delta V_{TH} + \eta V_T \ln\left(\frac{K_4 I_{O4}}{K_5 I_{O5}}\right)] + \eta V_T \, l\, n\left(\frac{K_6 I_{O6}}{K_7 I_{O7}}\right) \quad (4)$$

where A is the ratio of R_2 to R_1, and ΔV_{TH} is the difference of V_{TH5} and V_{TH4}. Ignoring the effect of I_0 differences, the derivative of V_{REF} over temperature is given by

$$\frac{dV_{REF}}{dT} = A[\frac{d\Delta V_{TH}}{dT} + \eta \frac{k_B}{q} \ln\left(\frac{K_4}{K_5}\right)] + \eta \frac{k_B}{q} \ln\left(\frac{K_6}{K_7}\right) \quad (5)$$

Zero temperature sensitivity could be achieved by adjusting the parameter of PTAT and CTAT terms in equation (5). For example, the CTAT coefficient could be modified by the resistor ratio A which is smaller than 1 for $R_2 < R_1$, so as to improve the stability of reference voltage over a wide temperature range with small process variation.

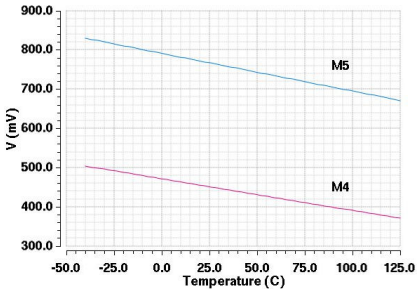

Fig. 2 Simulation result of threshold voltages of M_5 and M_4 vs. temperature.

A. Process variation

The process variation could affect both the reference voltage and its TC. As equation (4) and (5) show, the reference voltage and its TC are η-dependent, which is not constant and depends on the gate oxide and depletion-layer capacitances [4]. Fortunately, the variation of η is not intense [13]. Thanks to the proposed structure which employs NMOS transistor pairs to generate the CTAT and PTAT voltages, the variation of $K_4/K_5 * I_{o4}/I_{o5}$ and $K_6/K_7 * I_{o6}/I_{o7}$ are not large either. Also, the reference voltage is associated with the ΔV_{TH} of M_5 and M_4. Since M_4 and M_5 have different channel doping and hence different threshold voltages, ΔV_{TH} shows a certain level of variations. Fig. 3 shows the simulated ΔV_{TH} of M_4 and M_5 in different corners, which varies less than 40mV. The TC of ΔV_{TH} only varies slightly with corners as well. Furthermore, the variation of ΔV_{TH} will be reduced by R_2/R_1 for $R_2 < R_1$ in the proposed design, which is shown in (4) and (5). Therefore, the proposed CVR circuits works with small variations. Fig. 4 and Fig. 5 display the 200-times Monte-Carlo simulation results of V_{REF} and its TC without trimming, respectively, where the former's average μ_{VREF_SIM} = 202.28 mV, and standard derivation σ_{VREF_SIM} = 9.79 mV verify the small reference voltage variation of the proposed design. The simulation results of TC with μ_{TC_SIM} = 14.49 ppm/°C and σ_{TC_SIM} = 3.72 ppm/°C also display its relatively stable temperature sensitivity.

B. DC Offset of Op-Amp

The offset voltage of the amplifier affects the reference variation as well. Assuming a voltage V_{os} added to V_N in Fig. 1 models the offset, the relationship between V_P and V_N is then:

$$V_P = V_N + V_{os} \quad (6)$$

Thus, equation (4) can be revised as

$$V_{REF\_OS} = A[\Delta V_{TH} + \eta V_T \, l\, n\left(\frac{K_4 I_{O4}}{K_5 I_{O5}}\right)] + \eta V_T \, l\, n\left(\frac{K_6 I_{O6}}{K_7 I_{O7}}\right) + AV_{os} \quad (7)$$

From (7), it is obvious that the effect of the offset voltage of the Op-Amp can be relaxed if R_2/R_1 is smaller than 1. The transistors are sized to achieve small offset as well. Table I shows all the transistor sizes of the proposed CVR circuit.

C. Minimum Supply Voltage

The minimum supply voltage of the proposed CVR is

$$V_{DDmin} = V_{DS} + V_{GS} + V_N \quad (8)$$

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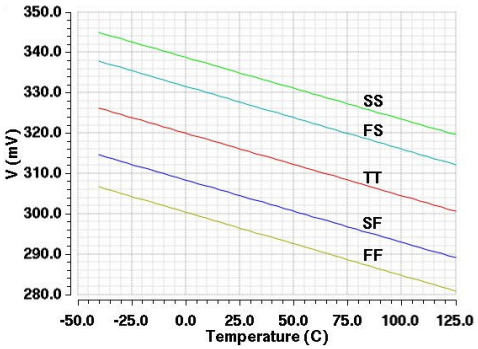

Fig. 3 Simulated ΔV_{TH} (i.e., V_{TH5}-V_{TH4}) in different corners.

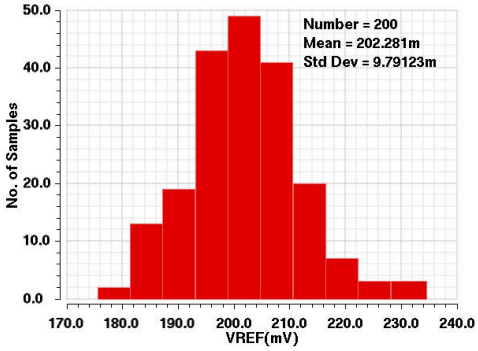

Fig. 4 -Monte-Carlo simulation result of V_{REF} without trimming.

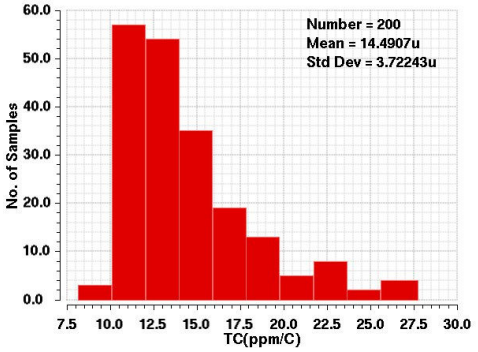

Fig. 5 Monte-Carlo simulation result of TC without trimming.

TABLE I
THE TRANSISTOR SIZES OF THE PROPOSED CVR CIRCUIT

Transistor	W/L(μm/μm)	Transistor	W/L(μm/μm)
M_1	4×2/8	M_2	2×2/8
M_3	4×2/8	M_4	3/8.8
M_5	2/3	M_6	8×2/9
M_7	2/9	M_{B1}	2/10
M_{B2}	2/10	M_{B3}	2/10
M_{B4}	2/10	M_{B5}	4/10
M_{B6}	4/10	M_{P1}	4×2/10
M_{P2}	2×4/4	M_{P3}	2×4/4
M_{P4}	6/10	M_{P5}	6/10
M_{P6}	6/8	M_{P7}	6/8
M_{P8}	4×2/10	M_{P9}	4×2/10

where V_{DS} is the drain-source voltage of transistor M_2 or M_{P1} depending on which one is larger, and V_{GS} is the gate-source voltage of transistor M_4 or M_{P2} depending on which one is higher. All these transistors are working in subthreshold region ($V_{DS} \geq 0.1$ V and V_{GS} lower than V_{TH}), and the minimum supply voltage does not exceed 0.6V in this design.

D. *Trimming Circuit*

The trimming circuit is added so as to further compensate the process variation and mismatch induced errors. Fig. 6 shows the trimming circuit. Six different size transistors, doubling the size to next, are placed in parallel with M_6. For the TT (typical-N & typical-P) corner, the switch S3 is on and others are off, shunting the corresponding transistor to circuit and adjusting the size of M_6 to optimize V_{REF}'s TC. Under the two boundary conditions, i.e. all switches are on and off, the result could cover several times of temperature sensitivity as shown in Fig. 5, i.e., 276.55 ppm/°C with all-switch-off and 575.834 ppm/°C with all-switch-on, respectively, indicating its sufficient trimming redundancy for testing purpose.

E. *PSRR Analysis*

The usage of the amplifier achieves high PSRR at low frequency for the CVR. The compensation capacitor C_C which is connected between V_{DD} and the output of the amplifier helps stabilize the current source at higher frequency, hence improving the PSRR [14]. Moreover, the CVR output capacitor C_o does not affect the loop stability, and can hence be enlarged

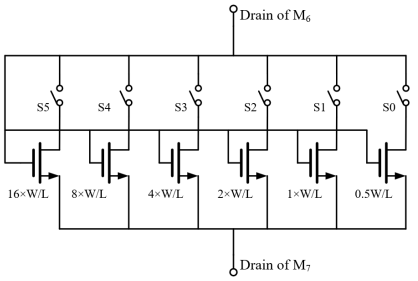

Fig. 6 Trimming circuit of M_6.

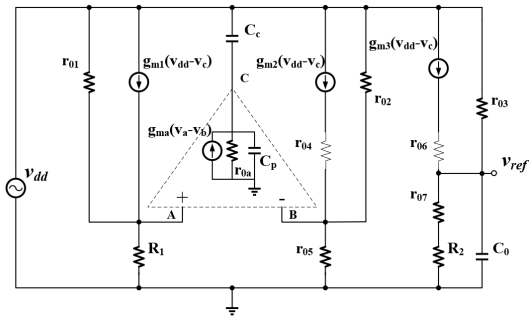

Fig. 7 The small-signal model for calculating PSRR of proposed circuit

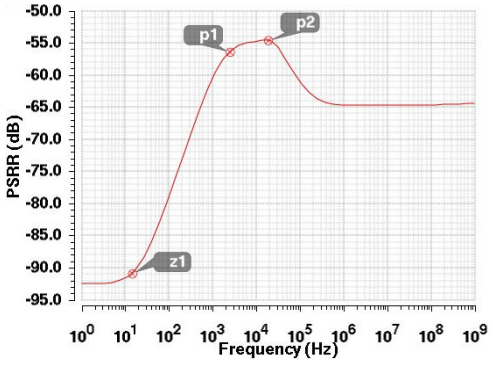

Fig. 8 The simulated curve of PSRR.

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to achieve high PSRR. Fig. 7 shows the small-signal model for calculating PSRR, where the transistors are replaced with small-signal symbols. g_{m1}-g_{m3} and r_{01}-r_{07} are the transconductances and the output resistances of M_1-M_3 and M_1-M_7, respectively. M_4 and M_6 run as source follower, and their output resistances r_{04} and r_{06} could be neglected. The whole amplifier is simplified as the g_m cell, the equivalent output resistor r_{0a} and the output parasitic capacitor C_p. Comparing with the larger capacitor C_C, the parasitic capacitors of the two input nodes are not considered. According to table I, we have $g_m=g_{m1}=2g_{m2}=g_{m3}$. The derived simplified v_{ref}/v_{dd} formula is shown in (9), which contains two poles and one zero, ignoring high-frequency zeros and poles led by parasitics. Due to the amplifier, DC value of v_{ref}/v_{dd} is large; due to compensation capacitor C_C reduced by $1/g_m r_{03}$, the zero z_1 is pushed to higher frequency; due to output capacitor C_o, the pole p_1 is reduced. All these effects help with improving the PSRR. Fig. 8 shows the simulated PSRR (i.e., $20*\log_{10}(v_{ref}/v_{dd})$), with the important poles and zero labeled. High PSRR is achieved in this design.

$$\frac{v_{ref}}{v_{dd}} = g_m R_z \frac{R_x - R_y}{R_x} \frac{(1+\frac{s}{z_1})}{(1+\frac{s}{p_1})(1+\frac{s}{p_2})} \tag{9}$$

$$R_x = \frac{1}{g_m g_m [2\,(R_1 \parallel r_{01}) - (r_{05} \parallel r_{02})]}$$

$$R_y = R_x \parallel r_{0a} \qquad R_z = r_{03} \parallel (r_{07} + R_2)$$

$$z_1 = \frac{1}{r_{0a}(C_p + \frac{1}{g_m r_{03}} C_c)} \qquad p_1 = \frac{1}{R_z C_0} \qquad p_2 = \frac{1}{R_y(C_p + C_c)}$$

III. Measurement Results

The proposed design is fabricated in a standard 0.18-µm CMOS process. Fig. 9 shows the chip photo and the active area is 340 µm*220 µm = 0.075 mm^2. One randomly selected chip was trimmed during the test, and then the same code was applied for all the measured samples. Fig. 10 shows the one-time-trimmed reference voltage V_{REF} vs. temperature in the range of -40ºC to 125ºC for 18 samples, showing that V_{REF} was distributed in a 5 mV narrow range. Fig. 11 demonstrates the statistics of V_{REF} distributions of the tested chips, and its average μ_{VREF} = 218.3 mV, standard derivation σ_{VREF} = 0.97 mV and σ_{VREF}/μ_{VREF} = 0.45% verify the small variation of this design. Fig. 12 shows distribution of TC. The average TC μ_{TC} is 23.47 ppm/°C, and the standard derivation σ_{TC} is 9.06 ppm/°C.

The measured current consumption vs. supply voltage is shown in Fig. 13 and the power consumption is 30.5 nW at 0.6 V supply. Fig. 14 shows the plot of V_{REF} vs. supply voltage, i.e. V_{DD} at room temperature, from 0 to 2.0 V. The line sensitivity (LS) of a random chip is 0.40%/V with V_{DD} from 0.6 to 2.0 V. Fig. 15 shows the measured PSRR which is -66.4 dB, -42.4 dB and -42.3 dB at 10 Hz, 1k Hz and 10M Hz, respectively. Table I summarizes and compares the proposed design with other works published recently. The proposed design achieves balanced performances in TC, variation, line sensitivity, PSRR and power consumption over a wide temperature range. The relatively high area cost, mainly caused by the large resistors R_1 and R_2 could be mitigated with reduced width and length proportionally by sacrificing certain accuracy and matching. Furthermore, the MIM capacitor areas could also be optimized by using MOS capacitor, which has higher capacitance density.

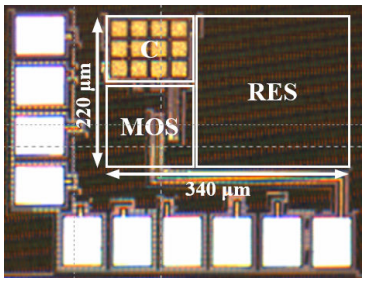

Fig. 9 Chip photo in 0.18-µm CMOS technology.

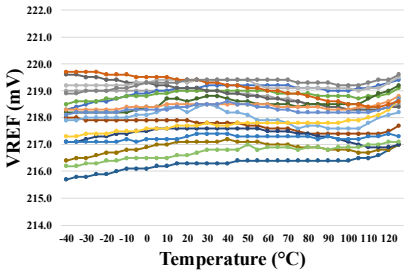

Fig. 10 Measured V_{REF} vs. temperature of one-time-trimmed 18 samples.

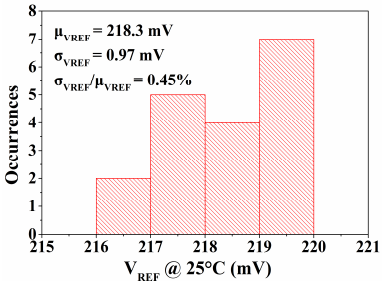

Fig. 11 Distribution of V_{REF} at 25°C.

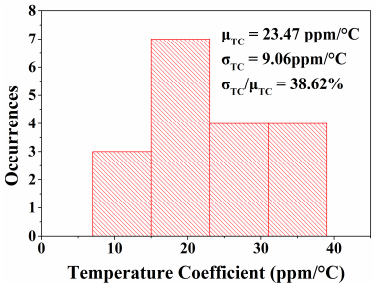

Fig. 12 Distribution of TC.

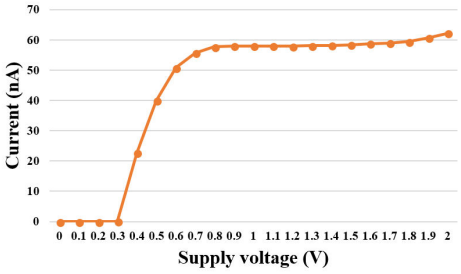

Fig. 13 Measured result of current consumption vs. supply voltage.

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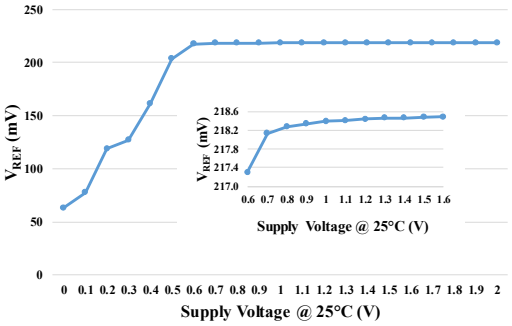

Fig. 14 Measured V_{REF} vs. supply voltage

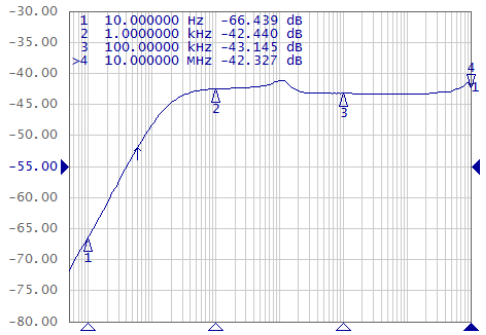

Fig. 15 Measured PSRR of proposed design.

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER WORKS

	This work	[4] JSSC'2013	[6] TVLSI'2017	[8] VLSIC'2011	[9] ISSCC'2017	[10] TVLSI'2017	[13] ISSCC'2015
Tech (nm)	**180**	180	180	180	180	180	350
Type	**CMOS**	Sub-BGR	CMOS	Sub-BGR	BGR	CMOS	BGR
V_{DD} (V)	**0.6 ~ 2.0**	0.7 ~ 1.8	1.1	0.8 ~1.6	1.3 ~ 1.8	0.8 ~ 2.2	1.4 ~ 3
Power (nW)	**30.5**	52.5	4.6	37	9.3	360	29
V_{REF} (mV)	**218.3**	548	755	240	1252	489	1176
σ/μ (%)	**0.45**	1.05	0.64	0.85	1.24	0.5	0.2
TC (ppm/°C)	**8.4 (Best)**		20 (Best)	5.5 (Best)	8 (Best)	6.5 (Best)	3.2 (Best)
	34.0 (Worst)	114 (Avg.)	89 (Worst)	90.1(Worst)	53 (Worst)	18.0 (Worst)	9.8 (Worst)
	23.5 (Avg.)		34 (Avg.)	51.2 (Avg.)	23 (Avg.)	14.17 (Avg.)	15 (Average)
Temp. (°C)	**-40 ~125**	-40 ~ 120	-15 ~ 140	-20 ~ 120	0 ~ 110	-30 ~ 110	-10 ~ 110
LS (%/V)	**0.40**	N/A	0.64	0.51	0.31	0.076	0.198
PSRR (dB)	**-66.4 @ 10 Hz**					-75 @ 100 Hz	
	-42.4 @ 1k Hz	-56 @ 100 Hz	-9 @ 10 Hz	-81 @ 50 Hz	-41 @ 100 Hz	-61 @ 100k Hz	N/A
	-43.1 @ 100k Hz		-47 @ 1M Hz		-43 @ 10k Hz	-59 @ 10M Hz	
	-42.3 @ 10M Hz					-51 @ 60M Hz	
Area (mm^2)	**0.075**	0.0246	0.0598	0.034	0.055	0.018	0.48

IV. CONCLUSION

A subthreshold CMOS voltage reference with down-to-0.6V supply voltage designed and fabricated in a 0.18-μm CMOS process has been presented. The CTAT voltage circuit is implemented by two different-threshold NMOS in series and scaled by two resistors which could adjust reference voltage and reduce the effect of offset. The PTAT voltage is consisted of two series same-threshold NMOS with different aspect ratios. All transistors are working in subthreshold region which reduces the power consumption and supply voltage. Measured results of a prototype design have demonstrated the good balanced performances in TC, variation, line sensitivity, PSRR and power consumption over a wide temperature range.

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