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A 1-nW Ultra-Low Voltage Subthreshold CMOS Voltage Reference with 0.0154%/V Line Sensitivity

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***Abstract*—This brief presents a CMOS voltage reference for Internet-of-Things applications, which requires ultra-low power and high insensitivity to voltage variation from ambient energy harvesting. This work proposed a novel self-regulating circuit to significantly diminish the line sensitivity of reference voltage to supply voltage without using any amplifiers or passive components. All the transistors in this design work in subthreshold region for low voltage and low power operation. The proposed design is fabricated in a standard 0.18-µm CMOS process. The measurement results show that, the proposed circuit could provide an average reference voltage of 151 mV with a variation coefficient of 0.84 %. It achieves a line sensitivity of 0.0154 %/V when the supply voltage varies from 0.5 V to 1.8 V. The measured power supply ripple rejections at 10 Hz, 1 kHz, 100 kHz and 1 MHz are -73.0 dB, -49.4 dB, -49.6 dB and -49.8 dB, respectively. The average temperature coefficient is measured as 89.83 ppm/℃ with a standard deviation of 12.19 ppm/°C in a temperature range from -40 ℃ to +125 ℃. The consumed power of this design is 1 nW with a minimum supply voltage of 0.4 V at room temperature, and the active area is 0.005 mm^2.**

***Index Terms*—CMOS voltage reference, subthreshold, low voltage, low power, line sensitivity.**

I. Introduction

THE growing interest on the Internet-of-Things (IoT) has spawned several applications, such as environmental sensors and biomedical devices, where battery recharging or replacement could be a key issue. Energy harvesting from ambient light, wind or vibration is a feasible solution to powering the IoT applications, which requires the functional circuits of IoT devices working in low supply voltage, low power consumption, and having good capabilities with voltage variation due to the unstable ambient energy source. The voltage reference is a fundamental building block in IoT devices to provide a precise voltage with tolerance of process, supply voltage and temperature (PVT) variations. The Bandgap Reference (BGR) is a conventional kind of voltage reference which can output a reference voltage (V_{REF}) with small PVT variation, but can hardly work with low supply voltage and low power consumption [1]-[4]. A 29-nW BGR in [3] employs the leakage current of transistor in subthreshold region to generate the proportional-to-absolute-temperature (PTAT) voltage and produces a voltage reference of 1.176 V with a small TC. However, large resistors are used in this work to reduce the current consumption, which costs certain amount of chip area. Compared to BGR, the CMOS Voltage Reference (CVR) working in subthreshold region is more suitable for IoT applications as it requires low supply voltage, provides low reference voltage, and consumes ultra-low power [5]-[11]. Therefore, the subthreshold CVR has become a popular research topic for IoT application.

To achieve a minimum supply voltage of 250 mV, the CVR proposed in [5] replaces the analog amplifier in the conventional CMOS voltage reference circuit with a low-voltage comparator, a charge-pump circuit, and a digital control circuit. However, this CVR consumes 5.35µW at a supply voltage of 250 mV, which is too large for ultra-low power applications. In [6], a 2-Transistor (2-T) subthreshold CVR generates the reference voltage by utilizing the difference of threshold voltage in two types of transistors without amplifiers or resistors to achieve a pico-watt power consumption and a minimum supply voltage of 0.5 V. However, the upper transistor connected to VDD in such a 2-T structure circuit will suffer from the channel-length modulation effect, which could weaken the independence of reference voltage on supply voltage.

Considering this background, this brief presents a CVR with a novel self-regulating circuit to significantly diminish the Line Sensitivity (LS) of reference voltage to supply voltage without using any amplifiers or passive components. The channel-length modulation effect is minimized. The LS performance is improved significantly, and high Power Supply Ripple Rejection (PSRR) is achieved. The rest of this paper is organized as follows: Section II describes the principle and implementation of the proposed voltage reference. Section III shows the measurement results and comparisons with previous works. In Section IV, the conclusions of this work are present.

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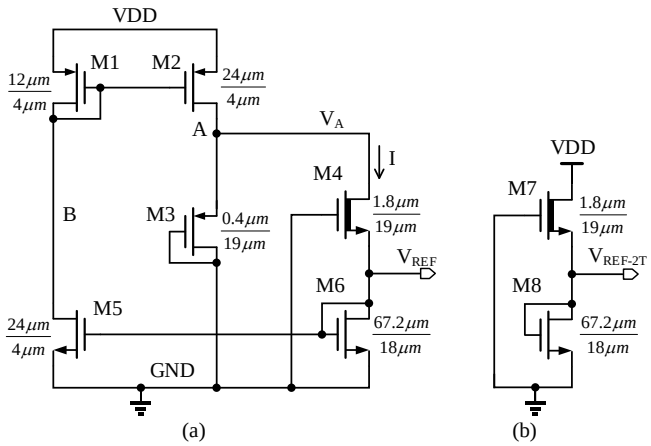

Fig. 1. Schematic of (a) the proposed CVR with self-regulating circuit, (b) CVR w/o self-regulating circuit (i.e., 2-T CVR in [6]).

II. The Proposed Design

A. Circuit Description

The proposed subthreshold CVR circuit is shown in Fig. 1(a). Transistors M1~M3 and M5~M6 are the standard 1.8 V input/output (I/O) PMOS and NMOS devices, respectively. M4 is a native 1.8 V device which has a near zero threshold voltage. To achieve the requirements of small area, low voltage and low power for IoT applications, all devices in this design are working in subthreshold region, without any operational amplifiers and passive components (resistors, capacitors) employed in the proposed circuit.

When the drain-source voltage (V_{DS}) of a transistor is over 0.1 V, the subthreshold current could be expressed as the well-known equation:

$$I_{subV_{TH}} = K\mu C_{OX}(m-1)V_T^2 \exp\left(\frac{V_{GS}-V_{TH}}{mV_T}\right) \quad (1)$$

where K = W/L is the ratio of the transistor's width (W) and length (L). μ is the mobility and C_{OX} is the oxide capacitance per unit area. m = 1 + C_d/C_{OX} is the subthreshold slope factor, where C_d is the depletion capacitance per unit area. V_T = kT/q is the thermal voltage, where k, T and q are the Boltzmann constant, absolute temperature and the elementary charge, respectively. V_{GS} and V_{TH} are the gate-source voltage and threshold voltage of the transistor, respectively.

The output reference voltage could be generated by connecting a native transistor and a standard transistor in series [5], in this design a native device for M4 and a standard device for M6. Except the near zero V_{TH}, the native devices are identical to the standard device, they have the same C_d and C_{OX}. So M4 and M6 have the same subthreshold slope factor. The current through M4 and M6 are equal, which contributes to equation (2). We can get the expression of V_{REF} from (2), as shown in (3).

$$\begin{aligned} I &= K_6\mu_6 C_{OX}(m-1)V_T^2 \exp\left(\frac{V_{REF}-V_{TH6}}{mV_T}\right) \\ &= K_4\mu_4 C_{OX}(m-1)V_T^2 \exp\left(\frac{-V_{REF}-V_{TH4}}{mV_T}\right) \end{aligned} \quad (2)$$

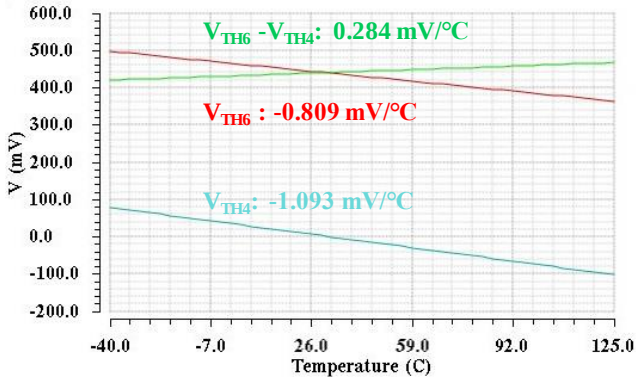

Fig. 2. Schematic simulation: V_{TH} of M4 and M6, and the difference threshold V_{TH6} - V_{TH4}.

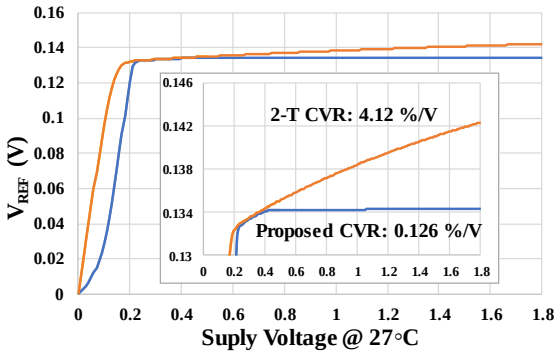

Fig. 3. Schematic simulation: V_{REF} vs. supply voltage of the proposed CVR compared with 2-T CVR.

$$V_{REF} = \frac{mV_T}{2}\ln\left(\frac{K_4\mu_4}{K_6\mu_6}\right) + \frac{(V_{TH6}-V_{TH4})}{2} \quad (3)$$

The threshold voltage of M4 and M6 are complementary to temperature, but the threshold voltage difference between the two transistors (V_{TH6} -V_{TH4}) is proportional to temperature as shown in Fig. 2. The differential of V_{REF} over T is

$$\frac{dV_{REF}}{dT} = \frac{mk}{2q}\ln\left(\frac{K_4\mu_4}{K_6\mu_6}\right) + \frac{d(V_{TH6}-V_{TH4})}{2dT} \quad (4)$$

where μ_4/μ_6 is about 1.4~1.9 in this case. By sizing K_4 and K_6, the aspect ratio of M4 and M6 appropriately, the first term of (4) could be set as negative to cancel out the second term. So, the zero-temperature sensitivity could be obtained.

The proposed CVR could start up by it-self without using extra start-up circuit. During the start-up of CVR, the leakage current of M4 feeds into M6, which raises up V_{REF} and starts up M5 and the whole CVR circuit.

B. Line Sensitivity and PSRR

The LS evaluates the independence of V_{REF} on the DC supply voltage. The minimum supply voltage and LS are critical specifications of CVRs for the IoT applications, which prefer low power and high independence to VDD. In 2-T CVR circuit shown in Fig. 1(b), the drain of M7 is connected to VDD directly, which causes the channel-length modulation of M7. Due to this second-order effect, after the start-up of 2-T CVR,

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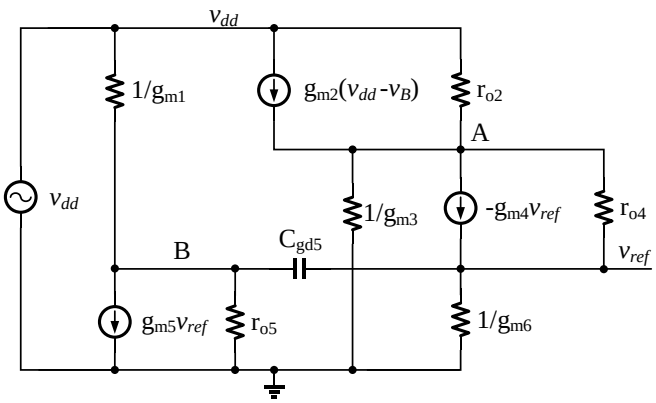

Fig. 4. The small-signal model of the proposed circuit for PSRR calculation.

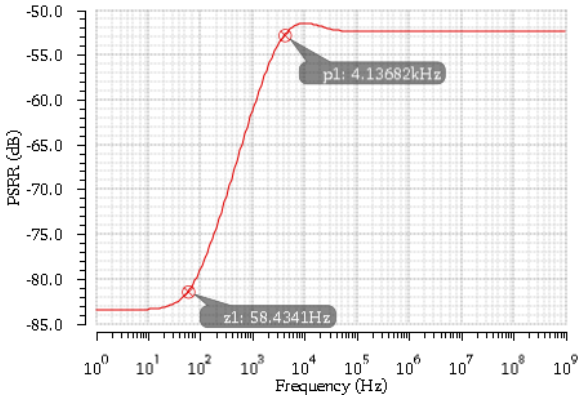

Fig. 5. Schematic simulation: PSRR of the proposed CVR with 1.8-V supply.

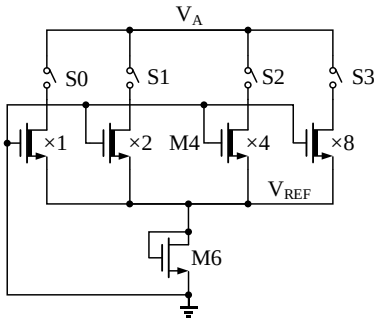

Fig. 6. Trimming circuit of M4 in the proposed CVR.

the drain-source current of M7 will keep increasing with the supply voltage growing up to 1.8 V. The variation of this current could induce the fluctuation of V_{REF}. Thus, the LS of 2-T CVR is high.

To achieve a low LS, we proposed a self-regulating circuit which consists of M1~M3 and M5 as shown in Fig. 1(a). The diode-connected M3 is an essential component of the self-regulating circuit, which makes the point A with a low impedance to ground to diminish the sensitivity of V_A to VDD. Therefore, the V_A with stable voltage could minimize the channel-length modulation effect of M4 and improve the LS of proposed CVR.

To quantitatively analyze the LS improvement of the proposed CVR, the LS of 2-T CVR could be expressed as

$$LS_{2T} = \frac{\Delta V_{REF}}{\Delta VDD} / V_{REF} \times 100\% \tag{5}$$

And the LS of the proposed CVR could be given by

$$\begin{aligned} LS_1 &= \frac{\Delta V_{REF}}{\Delta V_A} / V_{REF} \times 100\% \\ LS_2 &= \frac{\Delta V_A}{\Delta VDD} / V_A \times 100\% \\ LS &= LS_1 \times LS_2 \times V_A \times 100\% \end{aligned} \tag{6}$$

where LS_1 is the line sensitivity of 2-T sub-circuit in the proposed CVR, which equals to LS_{2T} in (5). LS_2 is the line sensitivity of the self-regulating circuit, and LS is the line sensitivity of the proposed CVR. From (5) and (6), we can see that, the LS of the proposed CVR is improved by ($LS_2 \times V_A$) times compared to the LS_2 of 2-T conventional CVR.

Fig. 3 shows the simulated V_{REF} versus V_{DD} of the proposed CVR compared with 2-T CVR. Getting supply from line-insensitive voltage V_A, the proposed CVR could achieve a LS of 0.126 %/V with an operating range of VDD from 0.4 V to 1.8 V, while the 2-T CVR has a LS of 4.12 %/V with the VDD range from 0.4 V to 1.8 V. the simulation results indicates that, the proposed self-regulating circuit could significantly improve the line sensitivity of CVR.

Fig. 4 shows the small signal model of the proposed design for PSRR calculation, where $g_{m1\text{-}6}$ are the trans-conductance of M1-6, respectively. r_{o2}, r_{o4} and r_{o5} are the output resistances of M2, M4 and M5, respectively. C_{gd5} is the gate-drain capacitance of M5 which forwards the coupled supply ripple from node B to V_{REF} and affects PSRR. To simplify the analysis, the other parasitic capacitors are neglected. The PSRR could be obtained based on the small-signal model shown in Fig. 4 and the result is approximately given by

$$PSRR = 20\log_{10}\left(\left|\frac{v_{ref}}{v_{dd}}\right|\right) \tag{7}$$

$$\frac{v_{ref}}{v_{dd}} = \frac{g_{m2}}{g_{m1}g_{m3}r_{o4}r_{o5}\left(g_{m6}+g_{m4}\right)} \cdot \frac{\left(1+\frac{s}{z_1}\right)}{\left(1+\frac{s}{p_1}\right)} \tag{8}$$

The zero and pole of PSRR function are given by

$$\begin{aligned} z_1 &= \frac{g_{m2}}{g_{m1}g_{m3}r_{o4}r_{o5}C_{gd5}} \\ p_1 &= \frac{g_{m4}+g_{m6}}{\left(g_{m1}+g_{m4}+g_{m5}+g_{m6}\right)r_{o4}C_{gd5}} \end{aligned} \tag{9}$$

As can be observed, there exists one pole and one zero in the expression of PSRR, where high frequency poles and zeros induced by parasitic factors are neglected. Fig. 5 shows the simulated PSRR of the proposed CVR, the corresponding frequencies of the pole and zero are marked in the plot.

C. *Trimming*

To optimize the TC performance due to the process variation

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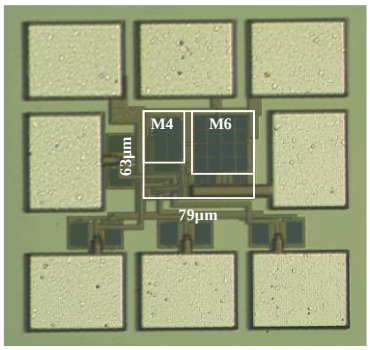

Fig. 7. Chip Microphotograph.

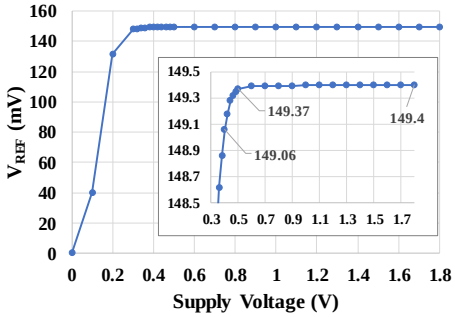

Fig. 8. Measured LS of the proposed CVR at room temperature.

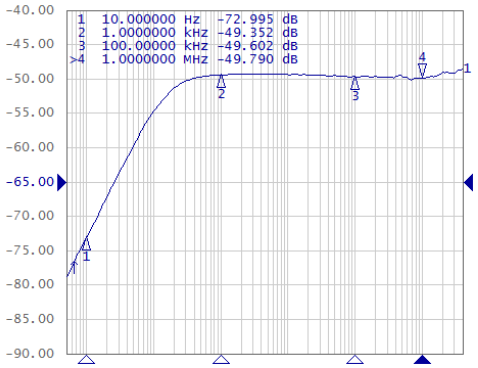

Fig. 9. Measured PSRR of the proposed CVR with 1.8-V supply.

and mismatch errors, M4 is trimmed as shown in Fig. 6 to adjust reference voltage. It based on modifying the width of M4 to modulate the CTAT slope factor. There are 4 switches, S0-S3, used for trimming. Trimming on M4 rather than M6 can reduce the area consumption of the chip. When the switch is turned on, the corresponding trimming transistor is working as M4 to increase the CTAT voltage ratio. If the switch is turned off, and the equivalent size of M4 is decreased, thus the TC of CTAT voltage is decreased. When in TT corner (typical N and typical P corner), the switch 2 is turned on and others are turned off. The control of switches in the measurement to trim TC of V_{REF} depends on the variations of V_{REF}.

III. Measurement Results

The proposed all-MOSFET subthreshold CVR is designed and fabricated in a standard 0.18-μm CMOS process. Fig. 7 shows the chip microphotograph. The active area of this design is 63 × 79 μm^2. The trimming code used in this measurement

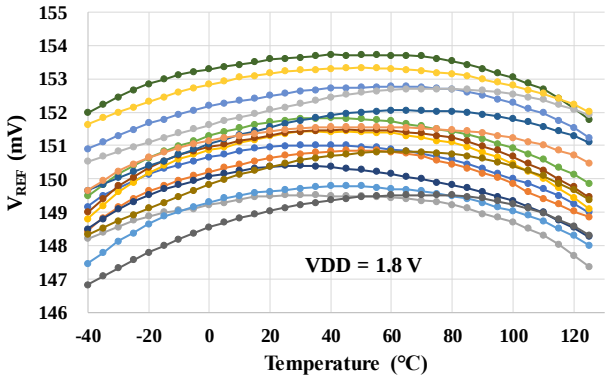

Fig. 10. Measured V_{REF} vs. temperature of one-time trimmed 16 samples with 1.8-V supply.

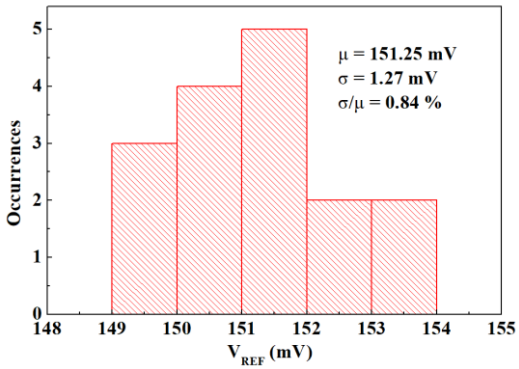

Fig. 11. Measured distribution of V_{REF} at 25 °C with 1.8-V supply.

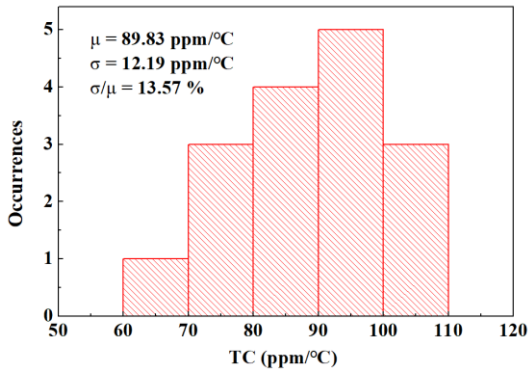

Fig. 12. Measured distribution of TC with 1.8-V supply.

was optimized by testing one randomly selected chip for a minimum TC, i.e., one-time trimming was used. The total 16 chips from the same run have been measured. Fig. 8 shows the measured line sensitivity of the proposed CVR at room temperature (i.e., 25 °C). The line sensitivity at 25 °C is only 0.0154 %/V when the supply voltage varies from 0.5 V to 1.8 V and 0.163 %/V when VDD varies from a minimum voltage of 0.4 V to 1.8V. The measured PSRR is given in Fig. 9, and the PSRR at 10 Hz, 1 kHz, 100 kHz and 1 MHz are -73.0 dB, -49.4 dB, -49.6 dB and -49.8 dB, respectively. The main difference between the measured and simulated PSRRs is the zero z_1 and the pole p_1 moving forward to the low frequency, which is caused by the parasitic capacitance at V_{REF} node. With the one-time trimming, Fig. 10 shows the measured output voltage V_{REF} versus temperature in a range of -40 °C to 125 °C. The statistics of V_{REF} distributions of the 16 tested chips are given in Fig. 11. The average of V_{REF} at 25 °C is 151.25 mV, and the

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER WORKS

	This work	[1] TCAS-I	[2] TCAS-I	[5] TCAS-II	[6] JSSC	[8] JSSC	[9] TCAS-II	[10] TCAS-II
Year	**2019**	2017	2018	2018	2012	2011	2018	2018
Tech (nm)	**180**	180	500	110	130	180	130	180
Type	**CMOS**	BGR	BGR	CMOS	CMOS	CMOS	CMOS	CMOS
Min. VDD (V)	**0.4**	1.3	2.1	0.242	0.5	0.45	1.1	0.4
Power Consumption (nW)	**1@0.4 V**	36400	79800	5350	0.002	2.6	27.5	9.6
V_{REF} (mV)	**151**	547	1.196	196	176	263.5	800	210
σ/μ (%)	**0.84**	N/A	0.62	N/A	0.72	3.9	5	0.31
TC (ppm/℃)	**89.83**	1.67 (Best) 10.55 (Worst)	5.87	134	62	142	100	82
Temp. Range (℃)	**-40 ~ 125**	-40 ~ 140	-5 ~ 125	10 ~ 90	-20 ~ 80	0 ~ 125	-40 ~ 85	-40 ~ 140
LS (%/V)	**0.0154@0.5-1.8 V** **0.163@0.4-1.8 V**	0.08	0.016	4.09	0.033	0.44	2	0.027
PSRR (dB)	**-73@10Hz** **-49.4@1kHz** **-49.8@1MHz**	N/A	-84@100Hz -37@100kHz	N/A	-53@100Hz -62@1MHz	-45@100Hz	N/A	-59@10Hz -47@1KHz -53@1MHz
Area (mm^2)	**0.005**	0.0094	0.053	0.013	0.0013	0.043	0.003	0.021
Samples	**16**	8	10	10	49	40	45	20

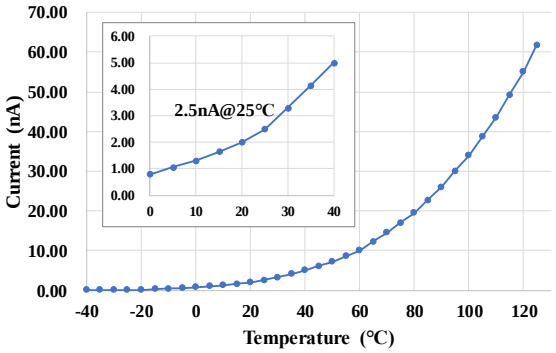

Fig. 13. Measured current consumption of the proposed CVR.

standard deviation is 1.27 mV with a variation coefficient σ/μ of 0.84 %, which shows a small variation of this design. Fig. 12 shows the TC distribution of all the 16 samples. The average TC is 89.83 ppm/°C, and the standard deviation is 12.19 ppm/°C with a variation coefficient σ/μ of 13.57 %. The measured current consumption versus temperature is given in Fig. 13. The minimum power consumption at 25 °C is about 1 nW with a minimum supply voltage of 0.4 V. Table I summarizes and compares the performance of the proposed design with prior state of the art. The proposed design achieves ultra-low power consumption and very small chip area with good variation performance. Excellent line sensitivity and PSRR showing the high independence of reference voltage to supply voltage. Compared to [6], the proposed CVR shows an improved LS, and an enlarged operation temperature range. As paid for the trade-off, the area is increased by 3.8 times and power consumption increased from pW to nW.

IV. CONCLUSION

This brief proposed an ultra-low power CMOS voltage reference with a novel self-regulating circuit, which can significantly diminish the channel length modulation effect on the 2-T CVR and scale down the LS by several times. All transistors in this design are working in subthreshold region without using any amplifiers or passive devices to achieve nano-Watt power consumption and operation at ultra-low supply voltage. The proposed voltage reference shows competitive line sensitivity, power supply ripple rejection and chip area for ultra-low power IoT applications.

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