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An All-MOSFET Voltage Reference With -50dB PSR @ 80 MHz for Low Power SoC Design

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***Abstract*—This brief presents a voltage reference (VR) for modern low power system on chip (SoC) applications, where high frequency supply ripple can degrade system performance. With a compact MOSFET low-pass filter, which was developed along with a feedback technique for a wide bandwidth PSR, the VR achieves PSR better than 50 dB for frequencies of up to 80 MHz not achieved in previous works. The proposed all-MOSFET VR was fabricated in a standard *0.18 µm CMOS* process. It achieves a temperature coefficient (TC) of 19 ppm/°C from − 30 °C to 80 °C. The line regulation is 0.098 %/V for a step from 1.1 V to 2.3 V supply voltage with 550 nW power consumption at room temperature and an area of 0.0180 mm^2.**

***Index Terms*— High PSR, All-MOSFET, Sub-1 V, Resistorless, Non-Bandgap, Low power**

I. Introduction

THE dynamic range of systems is getting substantially smaller due to scaling down of supply voltages in advanced CMOS technologies and the high demand for low power mobile devices. Also, the noise from high frequency switching converters and from high speed digital circuits, common in recent SoC applications, has resulted in high frequency supply ripples [3]. These ripples, when not sufficiently rejected, can be detrimental to system performance, especially in RF applications [1]–[3].

As a crucial part of modern SoC applications, voltage references (VRs) must be able to reject the supply ripple from noisy circuits [1]. Most techniques designed to make VRs more immune to supply noise may require an additional amplifier [6], RC filters, long channel transistors [1], cascode structures [5] or an additional gain stage [4]. Hence, these solutions come at the cost of chip area and power consumption.

With the proliferation of human body networks and the rise in the internet of things (IoT), low power and minimal chip area is now a necessary VR design requirement. Due to this, the traditional bandgap reference (BGR) has become a less attractive solution. Weak inversion designs, [8]–[10] which have become very attractive for low power applications may result in up to 15% variation in the reference voltage [8]. This is due to the inferior transistor ratio matching of weak inversion designs compared to strong inversion designs [11], [12] and the inaccuracies of weak inversion transistor models. Furthermore, the ultralow power (nanowatt) VR solutions that have been proposed recently [7]–[10], do not achieve the high PSR over wide frequencies required in modern SoC applications.

This work presents a low power non-bandgap voltage reference, which only uses MOSFETs. In the proposed VR, a proportional-to-absolute-temperature (PTAT) voltage is converted to a current proportional to $\mu_p T^2$. This current is used to extract a temperature-stable reference voltage from the V_{SG} of a diode-connected PMOS. Using feedback and a compact all-MOSFET passive low-pass filter a PSR better than −50 dB for frequencies up to 80 MHz is achieved.

The rest of the brief is arranged as follows: Section II presents the principle of operation of the VR. Section III presents results and discussion while Section IV summarizes the advantages of the novel all-MOSFET-based VR for low power SoC applications presented in this brief.

II. Principle of Operation

A composite transistor is used to generate a PTAT voltage, which is then converted to a current proportional to $\mu_p T^2$. This current serves as a bias current for the whole VR. Finally, a diode-connected PMOS transistor is used to generate the reference voltage. Fig. 1. shows the conceptual block diagram of the proposed VR.

A. Composite Transistor PTAT Generator

The PTAT voltage is generated using the difference between the V_{SG} of two PMOS transistors biased in sub-threshold region. The composite transistor shown in Fig. 2a provides the desired PTAT voltage for the biasing of the VR. This circuit was first introduced in [12]. To eliminate the body effect through the source to the body of each transistor, the transistors are implemented in their own wells.

The drain current, I_D, of a MOSFET in weak inversion based on the channel diffusion current is given by the expression:

$$I_D = I_s \left(\frac{W}{L}\right)\left(1 - e^{-\frac{V_{DS}}{V_T}}\right) e^{\frac{V_{GS}-V_{TH}}{mV_T}} \quad (1)$$

where $I_s = (m-1)\mu C_{ox} V_T^2$ is the characteristic current, m is the slope factor in subthreshold and $V_T = \frac{kT}{q}$ is the thermal voltage.

For $V_{DS} \geq 4V_T$, the effect of the V_{DS} on the current can be neglected [12], [13]. From the Fig. 2, using (1), V_{PTAT} can be expressed as;

$$V_{PTAT} = V_{SG1} - V_{SG2} = mV_T \ln(NK) \quad (2)$$

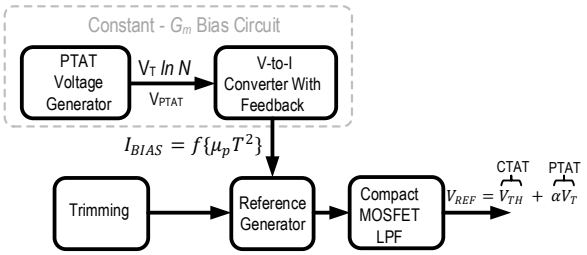

Fig. 1: The conceptual bock diagram of the proposed VR circuit. The composite transistor PTAT voltage generator puts forth the voltage needed to convert to a bias current for the whole VR. Finally, a diode-connected PMOS transistor (in the reference generator) is used to generate a temperature independent reference

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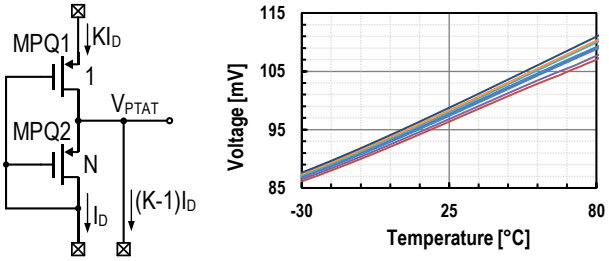

(a) Circuit schematic *(b) Simulated V_{PTAT} across process corners*

Fig. 2:Composite transistor PTAT generator

where $N = \frac{S_{MQ_2}}{S_{MQ_1}}$, $S_x = \left(\frac{W}{L}\right)_x$ and K is the ratio of the currents through MPQ1 and MPQ2. Fig. 2b shows the simulation results for the PTAT voltage of Fig. 2a across process corners.

B. Constant-G_m Bias Circuit (CGBC)

In Fig. 3, a voltage-to-current converter is used to convert the PTAT voltage from the composite transistor into a current proportional to $\mu_p T^2$ for biasing of the VR. With the exception of transistors MPQ1 and MPQ2, which are biased in weak inversion, all other transistors operate in strong inversion to ensure better transistor ratio matching [11], [12].

For $MP1$ and $MP2$ in strong inversion,

$$V_{SGMP1} - V_{SGMP2} = V_{PTAT} = mV_T \ln KN \tag{3}$$

$$I_{BIAS} = \frac{k_p}{2}(mV_T \ln KN)^2 S_{MP1}\left[\sqrt{\frac{S_{MP1}}{S_{MP2}}} - 1\right]^2 \tag{4}$$

where $k_p = \mu_p C_{ox}$. I_{BIAS} is determined by the aspect ratios (S_{MP1}, S_{MP2}, S_{MP1} and S_{MP2}) and the current ratio K.

The expression for the temperature dependence of mobility [14] is given by:

$$\mu(T) = \mu_0 \left(\frac{T}{T_0}\right)^{\alpha_\mu}, \tag{5}$$

where μ_0 is the mobility at temperature T_0, and α_μ is the mobility temperature exponent.

From (4) and (5) the TC of I_{BIAS} is given by:

$$TC_{I_{BIAS}} = \frac{\left(\frac{\partial I_{BIAS}}{\partial T}\right)}{I_{BIAS}} = \frac{2 + \alpha_\mu}{T}. \tag{6}$$

As seen in Fig. 5b, the bias current decreases with increasing temperature. This is because α_μ is above −2 in *IBM* 0.18μm.

Unlike the conventional constant-gm bias circuit which has only one feedback loop, an extra feedback path is added by transistors $MN0$ and $MP0$. This helps minimize the voltage

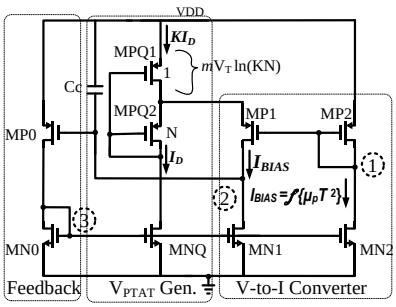

Fig. 3:Constant-Gm Bias Circuit (CGBC)

difference between Nodes 1 and 2 by regulating the gate voltage of $MN1$ without requiring $MN1$ to be diode connected as in the case of the conventional bias circuit. The feedback helps increase the loop gain and hence improves the PSR of the bias circuit.

A loop compensation capacitor (C_C) is inserted at the high impedance Node, 2 and VDD. This creates a dominant pole formed by C_C and $g_{mMP1} r_{dsMP1} R_A // r_{dsMN1}$. Also, C_C can be connected between Node 2 and Node 3 rather than between Node 2 and VDD (or GND). Such connection makes use of the Miller effect introduced by the gain from Node 2 to Node 3.

C. Generating the Reference Voltage (V_{REF})

The complete voltage reference circuit is shown Fig. 4. Since transistor $MP6$ works in the strong inversion, the reference voltage (V_{REF}) can be expressed as:

$$V_{REF} = V_{SGMP6} = |V_{THMP6}| + \sqrt{\frac{2MI_{BIAS}}{k_p S_{MP6}}}. \tag{7}$$

The V_{REF} temperature dependence is mainly due to the temperature dependence of V_{THMP6}, I_{BIAS} and of μ_p. The V_{TH} decreases linearly with temperature [14] as a first order approximation given by the expression:

$$V_{TH}(T) = V_{TH0} - \alpha_{V_{TH}}(T - T_0) \tag{8}$$

where V_{TH0} is the V_{TH} at temperature T_0, and $\alpha_{V_{TH}} = \left.\frac{\partial V_{TH}}{\partial T}\right|_{T=T_0}$.

From (7), I_{BIAS}, which is dependent on k_p ($\mu_p C_{ox}$), eliminates the effect of mobility (μ_p) temperature dependence on the output, V_{REF}. Also, since the I_{BIAS} varies with the square of temperature through V_T, the V_{REF} in (7) can be expressed as:

$$V_{REF} = V_{THMP6} + \alpha V_T, \tag{9}$$

$$\alpha = mln\,KN\sqrt{M\frac{S_{MP1}}{S_{MP6}}}\left[\sqrt{\frac{S_{MP1}}{S_{MP2}}} - 1\right]^{-1}. \tag{10}$$

The TC of the output reference voltage, determined by differentiating (9) while taking note of (8), is

$$\frac{\partial V_{REF}}{\partial T} = -\alpha_{V_{TH}} + \frac{k}{q}\alpha. \tag{11}$$

V_{REF} as seen in (9), does not depend on μ_p, resulting in a better thermal stability. The value of $\alpha_{V_{TH}}$of large channel PMOS in *IBM 0.18μm* CMOS process is 0.990 mV/℃.

By setting (11) to zero, the zero temperature coefficient (ZTC) is achieved based on the expression;

$$\frac{k}{q}\alpha = \alpha_{V_{TH}}. \tag{12}$$

As can be seen, (12) is valid within some approximations and simplified transistor characteristics. This first-order condition for a ZTC has been calculated by neglecting non-ideal effects. Henceforth, if (12) is satisfied, (9) can be written as $V_{REF} = |V_{TH0,p}| + \alpha_{V_{TH}} T_0$.

D. PSR and the Compact MOSFET Low Pass Filter (LPF)

Consider the active load in Fig. 4, the power supply noise at the VR output is a sum of the supply noise through the gate (path

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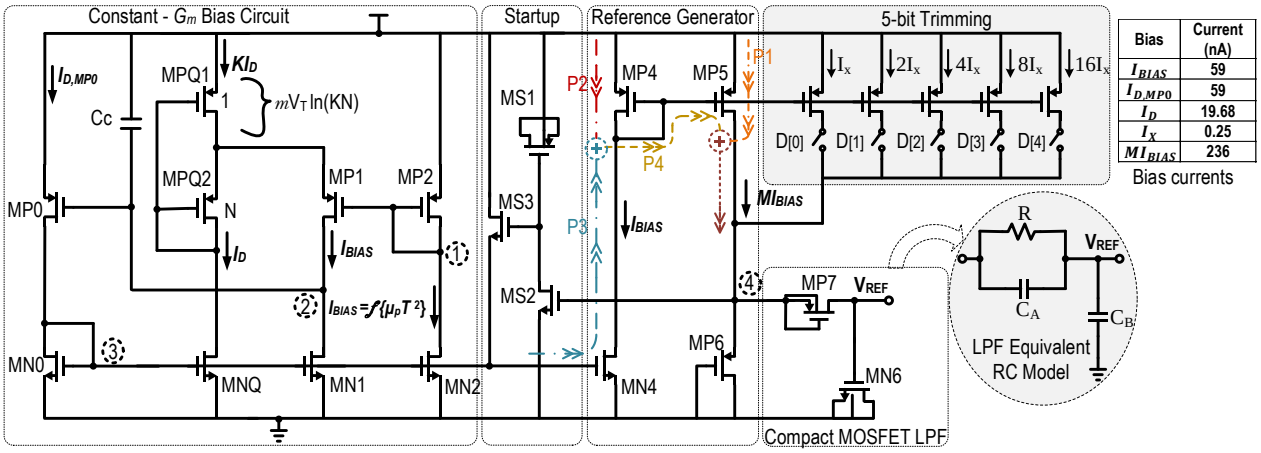


Fig. 4: Schematic of the proposed voltage reference with bias currents

P4) and the source (path P1) of $MP5$. To minimize the noise at the output, the supply ripple through P4 needs to be made equal to the noise through P1.

The expression of the supply noise through P1 to Node 4 (v_{REF1}), is given by:

$$v_{REF1} = \left(\frac{g_{mMP5}}{g_{mMP6}} + \frac{1}{g_{mMP6} r_{dsMP5}}\right) v_{dd}. \quad (13)$$

Assuming the $g_{mMP4} \approx g_{mMN4}$ the noise at Node 4 through P4 (v_{REF2}) can be approximated as,

$$v_{REF2} = -\frac{g_{mMP5}}{g_{mMP6}} (A_{CGBC} + 1) v_{dd}, \quad (14)$$

where A_{CGBC} is gain from supply to Node 3. The 1st term of (14) is due to the noise through P3 and the 2nd term is due to the noise through P2. From (13) and (14), the noise at node 4 is given by:

$$v_{REF} = v_{REF1} + v_{REF2} = \left(\frac{1}{g_{mMP6} r_{dsMP5}} - \frac{g_{mMP5}}{g_{mMP6}} A_{CGBC}\right) v_{dd}. \quad (15)$$

Also, the voltage (v_3) at node 3 can be expressed as:

$$v_3 = \left[\frac{g_{mMP0} r_{dsMP0} \left(1 - \frac{g_{mMPQ1}}{g_{mMN1}}\right) + 1}{g_{mMN0} r_{dsMP0} + 1}\right] v_{dd}. \quad (16)$$

If g_{mMPQ1} is made equal to g_{mMN1}, (16) is simplified as:

$$A_{CGBC} = \frac{v_3}{vdd} \approx \frac{1}{g_{mMN0} r_{dsMP0}} \quad (17)$$

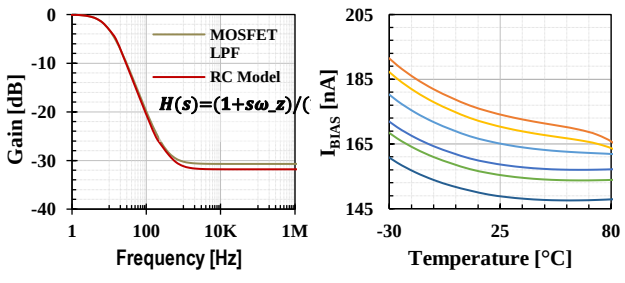
From (15), noise from supply is completely suppressed at the output when $A_{CGBC} = \frac{1}{g_{mMP5} r_{dsMP5}}$. This achieved by setting the intrinsic gain of $MP5$ as $g_{mMN0} r_{dsMP0}$ and it is feasible for frequencies within the loop bandwidth of the CGBC. At high frequencies, due the parasitic capacitances of $MN0 - MN4$, $A_{CGBC} \approx 0$, leaving $\frac{1}{g_{mMP6} r_{dsMP5}} v_{dd}$ at the output.

The compact MOSFET LPF in Fig. 4 is used to attenuate the high frequency supply noise at the output. Since the filter is made of only MOSFETs, $MN6$ (biased in strong inversion) and $MP7$ (at cut off), it occupies a smaller area compared to an RC filter of similar bandwidth. Although, RC LPF's are widely used to improve the PSR of voltage references, the MOSFET LPF offers a compact solution. From the equivalent RC model in Fig. 4, the transfer function of the LPF is simplified as:

$$H(s) = \frac{1 + sC_A R}{1 + s(C_A + C_B)R} = \frac{1 + s\omega_z}{1 + s\omega_p}, \quad (18)$$

Where $R \approx 1/g_{dsMP7}$, $C_A \approx C_{gdMP7} + C_{bdMP7}$, $C_B \approx C_{gsMN6} + C_{gdMN6}$. C_A and C_B are estimated from the basic MOSFET capacitance equations. The resistance, R ($1/g_{dsMP7}$), can be estimated by differentiating (1) while noting that $V_{SGMP7} = 0$;

$$g_{dsMP7} = \partial I_D / \partial V_{DS} = (m-1)\mu C_{ox} V_T S_{MP7} \left(e^{-\frac{V_{DS}}{V_T}}\right) e^{-\frac{|V_{THO,P}|}{mV_T}} \quad (19)$$



(a) Filter frequency response *(b) I_{BIAS} across process corners*

Fig. 5: Simulated (a) frequency response of MOSFET LPF and equivalent RC model and (b) temperature dependence of IBIAS across process corners

III. Results and Discussion

The proposed VR is implemented in the *IBM 0.18µm* CMOS process. Due to process variations and mismatches, a 5-bit binary weighted current calibration was implemented by varying the bias current at the output. The VR occupies an area of 0.018 mm^2, and the chip micrograph is shown in Fig. 6.

A. Measurement setup and Trimming

The setup for temperature performance measurement is shown in Fig. 7b. An ultra-low input bias current (TI-OPA 129) amplifier is used as an external buffer to isolate loading of the DC multi-meter from the VR. As seen in Fig. 7b, to avoid the temperature performance of TI-OPA 129 from affecting DC test results, the VR chip is mounted on a separate PCB and placed in the temperature chamber alone.

The PSR measurement setup is shown in Fig. 7a. The supply ripple injected is 400 mV$_{P-P}$ across the measured frequency (10 Hz to 80 MHz). A high speed amplifier (TI-OPA 354) is connected at the output of the VR for the PSR measurement. The amplifier is design to have a gain of 100 V/V across the measured frequency to avoid hitting the measurement

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equipment sensitivity limit.

The trimming scheme is based on measurements at two temperatures. A successive approximation process is used without exceeding three trimming steps. The 5-bit digital trim codes are generated externally using Altera Cyclone III FPGA. The trim value for each sample is initially set to 16 (code 10000) and then the V_{REF} is measured at both the minimum ($V_{REF,min}$) and maximum ($V_{REF,max}$) temperatures. If $V_{REF,min} \gg V_{REF,max}$, the threshold voltage is stronger and the bias current is increased. The bias current is decreased if $V_{REF,min} \ll V_{REF,max}$. The calibration process ends when $V_{REF,min} \approx V_{REF,max}$.

B. *Measurement Results*

The TC of the trimmed reference is 19 ppm to 29 ppm for supplies from 1.1 V to 2.2 V shown in Fig. 8a. Fig. 8b shows a similar plot in which the performance of five trimmed samples for temperatures ranging from −30 ℃ to 80 ℃ is shown. This means the VR is suitable for consumer applications since the typical required operating temperature range for commercial applications is from 0 ℃ to 70 ℃. From the Monte Carlo (MC) simulations shown in Fig. 9, the mean (μ) and the standard deviations (σ) are 888.39 mV and 30.58 mV, respectively, for the untrimmed V_{REF} and 893.15 mV and 1.66 mV, respectively, for the trimmed V_{REF}. This corresponds to a V_{REF} variation (σ/μ) of 3.44 % for the untrimmed V_{REF} which is comparable to the variation reported in most MOSFET VRs such as in [15] and [18]. The trimmed V_{REF} variation is 0.185 %.

Fig. 10c illustrates how measured reference voltage varies with supply voltage. The line regulation (LR) is 0.0938 %/V for voltages above 1.1 V at room temperature. Fig. 10a shows the measured output ripple for 100 kHz, and 1 MHz input supply ripple at 400 mV_{P-P} amplified 100 times.

The PSR performance between 10 Hz and 80 MHz is shown in Fig. 10b, where the PSR with and without the MOSFET LPF from simulation and experimental testing are compared. For the experimental testing, the PSR without the compact MOSFET LPF is more than 28 dB for frequencies up to 30 MHz due to the feedback path, while the PSR with the compact MOSFET LPF is more than 50 dB up to 80 MHz.

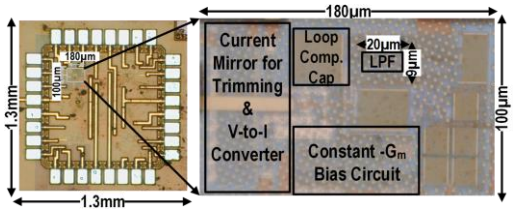


Fig. 7: Chip micrograph showing the proposed VR

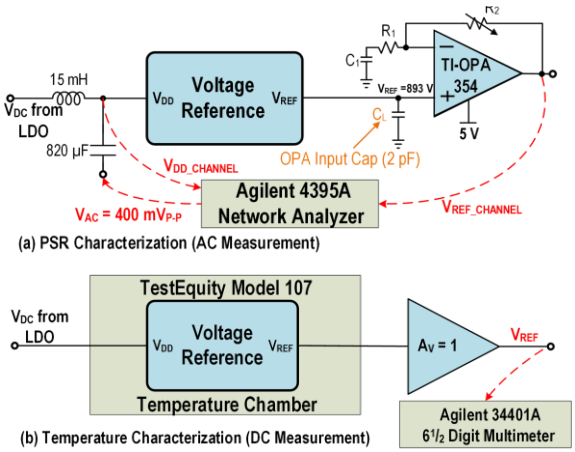
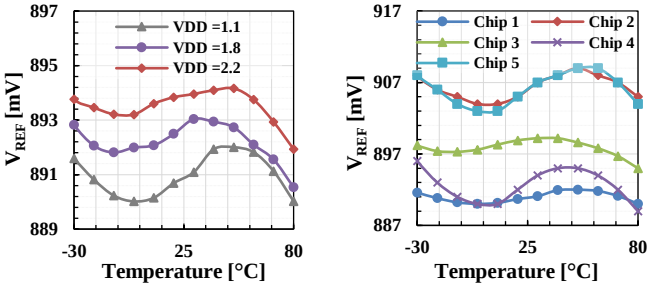
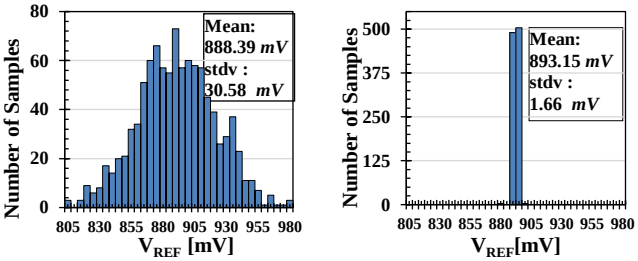


Fig. 7: Measurement setup



(a) V_{REF} for various supply voltages *(b) V_{REF} @ 1.1 V supply for 5 samples*

Fig. 8: Measured output voltage V_{REF} as a function of temperature



(a) Untrimmed V_{REF} @ 27 °C *(a) Trimmed V_{REF} @ 27 °C*

Fig. 9: MC simulation (1000 runs) of V_{REF} for mismatch and process variations

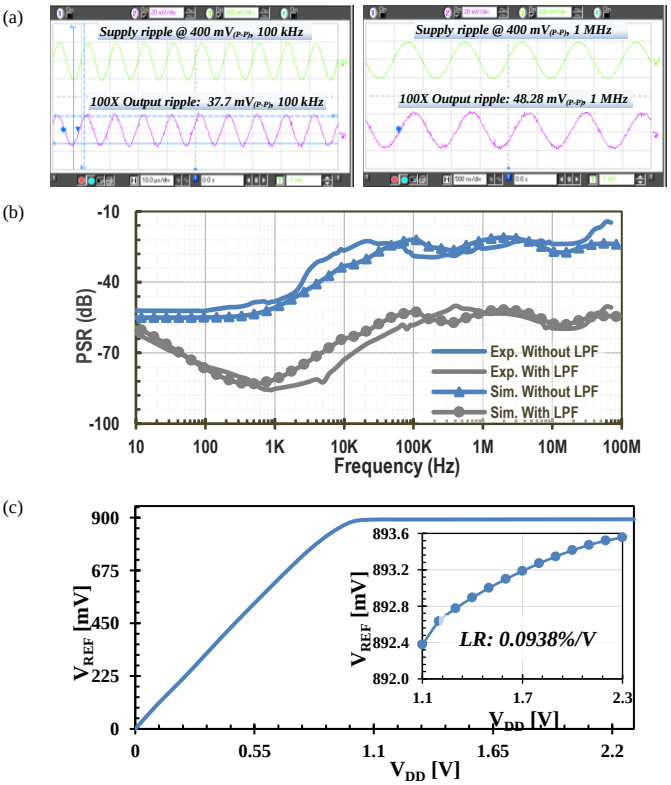


Fig. 10: (a) Measured power supply ripple response after 100X gain by the external high bandwidth amplifier for $V_{DD} = 1.1\,V$, $V_{ripple} = 400\,mV$, 100 kHz *and* 1 MHz, (b) is simulation and measured PSR from 10 Hz to 80 MHz for proposed VR @ $V_{DD} = 1.1\,V$, and (c) measured $V_{REF}$is a function of supply voltage showing an $LR = 0.0938\ \%/V$

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TABLE 1
PERFORMANCE COMPARISON OF THE PROPOSED VR WITH OTHER CMOS REFERENCES

Parameter	[7] JSSC'12	[9] JSSC'13	[15] TCAS-II'14	[16] JSSC'11	[17] JSSC'07	[18] VLSI'15	[19] TCAS-I'14	This Work
Process (CMOS)	0.13µm	0.18µm	0.11µm	0.16µm	0.5µm	0.065µm	0.18µ	**0.18µm**
Type	BGR	BGR	MOSFET with R	BGR	BGR	MOSFET with R	BGR	**MOSFET Only**
Temperature (℃)	-20 - 85	-40 - 120	10 – 90	-40 - 125	-40 - 125	-40 – 90	-40 – 120	**-30 - 80**
Supply (V)	0.75 – 1.6	1.2 – 1.8	0.24 – 0.4	1.8	1 – 5	0.75 – 1.2	1.2	**1.1 – 2**
Power (µW)	0.170	0.100	5.350	99	20	0.290	43.200	**0.550**
Vref (V)	0.256	1.090	0.195	1.087	0.190	0.474	767	**0.893**
TC (ppm/℃)	40	147	134	12	11	40	4.5	**19**
Vref (σ/µ) %	0.500	0.737	3.380	0.150	0.190	3.375	N/A	**0.185 | 3.44**
Trimming	yes	no	no	yes	no	yes	yes	**yes | no**
LR (%/V)	N/A	N/A	0.8	N/A	0.004	0.242	0.054	**0.093**
PSR (dB)								
@100Hz	-70	-62	N/A	-74	N/A	-40	-84	**-75**
@100kHz	N/A	-10.0	N/A	N/A	N/A	-25	-57	**-58**
@10MHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	**-60**
@80MHz	N/A	N/A	N/A	N/A	N/A	N/A	N/A	**-50**
Active Area (mm^2)	0.0700	0.0294	0.0130	0.1200	0.4000	0.0198	0.036	**0.0180**

This shows that the techniques used in the proposed VR can immensely improve PSR over a wide bandwidth with minimum area.

Table 1 summarizes the performance of the proposed VR and compares it with previously reported CMOS voltage references. Although [7], [9], [16], and [19] have advantages in power consumption, they do not achieve a high PSR at high frequencies required in modern SoC applications. Also, the proposed VR compared with the bandgap references (BGRs) [7], [9] and the MOSFET references [15], [18] has a better TC and a higher accuracy (σ/µ).

IV. Conclusion

An all-MOSFET-based VR for low power SoC applications fabricated in standard *0.18 µm* CMOS process has been presented. The VR which achieves a PSR of −50 dB at 80 MHz consumes 550 nW at room temperature for 1.1 V supply. The high PSR over a wide bandwidth is achieved by using feedback and a compact MOSFET passive LPF. The high PSR and design flexibility, along with a more compact area, make this VR more suitable than other VRs for multifunctional SoC applications without any additional process requirements.

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