A Low-Supply-Voltage CMOS Sub-Bandgap Reference

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***Abstract*—A low-power (21 μW) bandgap reference source that is operable from a nominal supply voltage of 1.4 V is described. The circuit provides an output voltage equal to the bandgap voltage having a low output resistance and allows resistive loading. It does not use resistors or operational amplifiers. Thus, the design is suitable for fabrication in any digital CMOS technology. The circuit uses a current conveyor and current mirrors to convert the proportional to absolute temperature voltage into a current using a MOSFET. The current is converted back to a voltage by using the functional inverse of the FET $v-i$ characteristics. This makes the voltage gain linear and temperature independent. The absence of back-gate bias is the reason for achieving the low supply voltage of operation. Simulation results using the transistor models for the 0.18-μm TSMC process show that the voltage-variation over the temperature range 0 to 100 °C is $<$1 mV.**

***Index Terms*—Bandgap reference source, power supply, voltage reference, voltage regulation.**

I. Introduction

THIS paper describes a novel bandgap reference circuit that can be operated from a nominal 1.4-V power supply. It gives an output-voltage of 1.012 V close to the bandgap voltage [1] of silicon. The simple circuit does not use an operational amplifier and dissipates very low power of 21 μW. No resistors are used in its design and hence it can be fabricated in any digital CMOS process. The principle of operation of the circuit is described using the simple square-law model for the MOSFETs. Simulation results using the models of TSMC 0.18-μm technology are presented.

Bandgap reference sources [2] are widely used to define precise voltages that have a low temperature variation over commercial or military temperature ranges. Low-power circuits [3] are needed for battery operable hand-held devices. The general principle of operation of bandgap circuits is based on

$$V_{\rm BG} = V_{\rm BE} + \lambda V_T \tag{1}$$

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where $V_{\rm BG}$ represents the bandgap voltage, $V_{\rm BE}$ is the base-emitter voltage of a bipolar junction transistor, and V_T represents the thermal voltage (k_BT/q). Here the symbols k_{BT}, T, and q have their usual meaning namely, Boltzmann's constant, absolute temperature and electronic charge. Simply stated the negative temperature coefficient of $V_{\rm BE}$ in (1) is cancelled by the positive temperature coefficient of λV_T. The symbol λ is a constant which is a well defined and temperature-independent voltage-gain of an amplifier. A voltage proportional to V_T is generated as the difference in voltage-drops across two current-biased P-N junctions having a well-defined current-density ratio [4].

II. Principle of Operation

The circuit operation is explained first using simplifying assumptions that are relaxed subsequently. All the CMOS transistors in the circuit are operated in strong inversion and in saturation. Initially assume a square-law model for the MOSFETs given by

$$I = k(V_{\rm GS} - V_{\rm TH})^2. \tag{2}$$

Here $V_{\rm GS}$ represents the gate-source voltage and $V_{\rm TH}$, the threshold voltage of a FET operating with no back-gate bias. The symbol $k \equiv (1/2)\mu C_{\rm ox}(W/L)$. The symbols used have their usual meaning of gate-capacitance per unit area, carrier mobility and aspect ratio, respectively. The gate–source voltage $V_{\rm GS}$ of a transistor is equal to the sum $V_{\rm TH} + V_{\rm ON}$, where $V_{\rm ON}$ is the excess voltage needed over and above $V_{\rm TH}$ to support the channel current. All voltages and currents associated with the transistor M_j has the same subscript j except for the primary current I flowing through the transistor M_1.

In Fig. 1, Q_1 and Q_2 shown as diodes represent the emitter-base junctions of two vertical substrate PNP transistors transistors where collector and base are tied to $V_{\rm SS}$. Their junction areas are in the ratio of 1:10. Further Q_1 and Q_2 are biased by currents in the ratio of 10:1 and their voltage drops are $V_{\rm BE1}$ and $V_{\rm BE2}$ respectively. The voltage difference $(V_{\rm BE1} - V_{\rm BE2})$ is proportional to the natural logarithm of their current–density ratio J_{C1}/J_{C2}. Thus

$$V_{\rm BE1} - V_{\rm BE2} = V_T \ln(J_{C1}/J_{C2}). \tag{3}$$

Since $(J_{C1}/J_{C2}) = 100$ we get $(V_{\rm BE1} - V_{\rm BE2}) = V_T\ln(100) \approx 4.6V_T = 120$ mV at $T = 300$ K. This voltage is commonly referred to as "proportional to absolute temperature" (or simply PTAT) and is represented by the symbol $V_{\rm PTAT}$. It is difficult to obtain a much higher value than 120 mV because

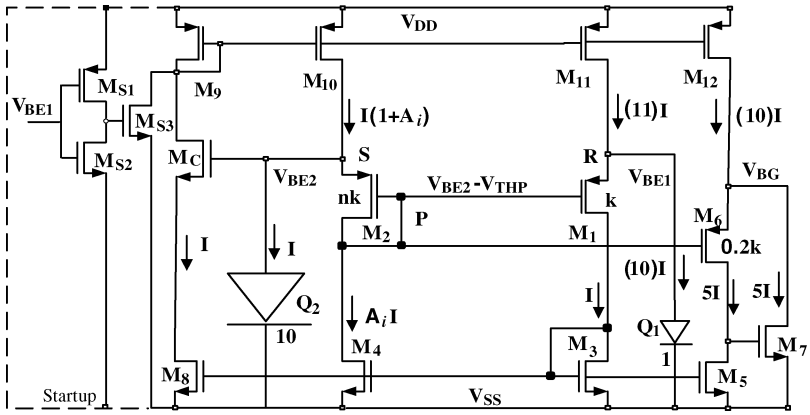

Fig. 1. Circuit diagram of the bandgap reference source.

it is logarithmically related to the current density ratio. Thus, the main task in building a bandgap reference is to amplify the PTAT voltage. From (1) for a value of $V_{\rm PTAT} = 120$ mV and $V_{\rm BE} \approx 650$ mV the voltage-gain λ needed is about 4.6 giving $\lambda V_T \approx 552$ mV. Thus, (1) gives $V_{\rm BG} \approx 1.2$ V. $V_{\rm PTAT}$ of only 120 mV is not big enough to turn on an enhancement mode MOSFET since the threshold voltage is about half a volt or more. Thus, it is customary to use a differential pair (in which threshold voltages cancel) making it possible to generate a current from $V_{\rm PTAT}$ which is the first step in obtaining voltage-gain. Subsequently this current is converted back to a voltage thereby achieving the required gain λ. Differential pairs need current biasing and in a digital technology having no resistors an active load is needed to generate an amplified single-ended output [5]. Thus, it is difficult to design the required amplifier [6], if not impossible, to keep a low supply-voltage by this conventional approach.

To overcome this limitation a pair of p-channel transistors M_1, M_2 is inserted as shown in Fig. 1. Their sources are connected to the two nodes (R, S) between which the potential difference $(V_{\rm BE1} - V_{\rm BE2}) = V_{\rm PTAT}$ is developed. This configuration of the transistors M_1, M_2, M_3 and M_4 forms a negative-impedance converter (NIC) [7]. In this application the intention is to use the circuit as a current-conveyor [8]. Here the function of M_2 is only to cancel the $V_{\rm THP}$ of M_1. This is easily arranged as follows. First the width (W_2) of p-channel transistor M_2 is scaled to be n-times that (W_1) of M_1. In Fig. 1 transistor M_2 is shown as a bigger device to emphasize this. The sources of all the p-channel transistors are connected to the body to avoid back-gate bias. This is extremely important because the circuit has to bias up with a single diode drop. Further, the n-channel transistors (M_3, M_4) form a current mirror with a gain A_i less than unity so that $V_{\rm ON2}$ is neglible small. Thus, the current I in the transistor M_1 become equal to $k{V_{\rm ON1}}^2$. Note that all the currents in the circuit are derived from this current I flowing in M_1. The n-channel current-mirror (M_3, M_5) feeds the output circuit. The mirror (M_3, M_8) provides the input current for the multiple-output p-channel current-mirror (M_9-M_{12}) which sets the bias currents in the diodes (in the ratio 1:10) as well as the output-circuit.

The current I, mirrored via the current-mirror (M_3, M_5) is forced to become equal to the drain current of the p-channel transistor M_6 by the shunt negative feedback provided by M_7. Note that the gate of the source-follower transistor M_6 is connected to the node P. Thus, the threshold voltage of M_6 is also cancelled by M_2 making the output-voltage equal to the sum of the diode-voltage $V_{\rm BE2}$ and the amplified PTAT voltage $V_{\rm ON6}$. Note that the voltage $V_{\rm ON6}$ is proportional to $\sqrt{I/k_6}$. Thus, the voltage-gain A_V needed for $V_{\rm PTAT}$ is obtained by scaling the aspect ratio (W/L) of M_6 with respect to that of M_1 as well as some current-gain (m) of the mirror (M_3, M_5). This temperature-independent gain A_V will be given by

$$A_v = \sqrt{m(W_1L_6)/(L_1W_6)}. \tag{4}$$

The output circuit configuration formed by the transistors M_{12}, M_6, M_5, and M_7 is a well-known source–follower circuit (also known as the super-source–follower or constant-current-operated source follower) [9]. This gives a low output-impedance for the bandgap reference voltage $V_{\rm BG}$ at the source of M_6. This source–follower is capable of driving resistive loads since the load-current is supplied by M_7 and not by M_6. The necessary load-current needed is set up in M_7 by M_{12}. The voltage $V_{\rm ON12} = \sqrt{I_{12}/k_{12}}$ depends upon both the current I_{12} as well as the aspect ratio chosen for M_{12}. This is typically a fraction of a volt.

The current I through M_1 was assumed to be proportional to the square of the PTAT voltage $V_{\rm ON1}$. This assumption can now be relaxed, because this current is converted back to a voltage using the functional-inverse generated as $V_{\rm ON6}$ in the source follower. The gain is both linear and temperature-independent whatever the function may be so long as the function and functional inverse are accurate [10]. This is the most important feature of the circuit. The two other basic building blocks used in the circuit are the current conveyor and current-mirrors. These do not depend on the square-law model either. The minimum power-supply-voltage is $V_{\rm BG} + V_{SD12}$ to keep M_{12} in saturation. Note that all n-channel transistors are operated with their sources grounded so that there is no back-gate bias. The key transistors (M_1, M_2 and M_6) that perform the $v - i$ function and its functional inverse $i - v$ are p-channel transistors with no back-gate bias and this is the most important reason for achieving the low supply voltage operation.

III. Circuit Analysis

We will first evaluate the primary current I flowing in M_1 from which all the currents in the circuit are derived. Writing

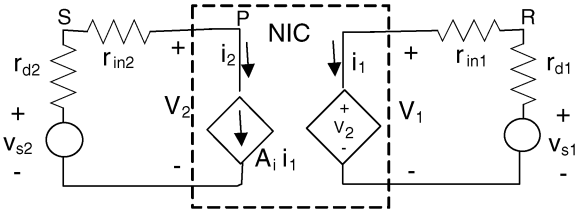

Fig. 2. Small-signal model of the NIC circuit.

the Kirchhoff's voltage law (KVL) around the loop containing the diodes (Q_1, Q_2) and p-channel transistors (M_1, M_2) gives

$$V_{\rm BE2} - V_{SG2} + V_{SG1} - V_{\rm BE1} = 0 \text{ or}$$
$$V_{\rm PTAT} = V_{\rm BE1} - V_{\rm BE2} = V_{SG1} - V_{SG2}. \quad (5)$$

Note that the threshold voltages of the transistors M_1 and M_2 cancel. Assuming a gain of A_i for the mirror (M_3, M_4) gives

$$V_{\rm PTAT} = \sqrt{I/k} - \sqrt{A_i I/nk} = V_{\rm ON1} - V_{\rm ON2} \text{ or}$$
$$I = (k/\alpha^2)V_{\rm PTAT}^2, \qquad \alpha = [1 - \sqrt{A_i/n}] \text{ or}$$
$$V_{\rm PTAT} = \sqrt{I/k_{\rm eff}} \text{ or}$$
$$I = k_{\rm eff} V_{\rm PTAT}^2. \quad (6)$$

The effect of the NIC can be taken into account by simply changing the value of k to $k_{\rm eff}$ where $k_{\rm eff} = k/\alpha^2$. For values of $A_i < 1$ and $n > 1$, the value of α is less than unity and thus $k_{\rm eff}$ is larger than k causing an increase in I. The quantity $\sqrt{A_i/n}$ should be controlled carefully so that its value is much less than unity. For $\sqrt{A_i/n} \ll 1$, $\alpha \to 1$ and $k_{\rm eff} \to k$, the NIC does not amplify the current. Now $V_{\rm ON2}$ can be ignored and the gate voltage of M_2 (node P) will be at a voltage $V_{\rm BE2} - V_{\rm THP}$.

From (1) the term λ assuming $k_6 = rk_1$ is given by

$$\lambda = \left(\frac{\sqrt{m/r} - 1/\sqrt{n}}{\alpha} \right) \quad (7)$$

where m is the current gain of the mirror (M_3, M_5), n is the ratio between (M_2, M_1), r is the ratio between (M_1, M_6). Equation (1) for this circuit becomes

$$V_{\rm BG} = V_{\rm BE2} + \left(\frac{\sqrt{m/r} - 1/\sqrt{n}}{\alpha} \right) V_{\rm PTAT}. \quad (8)$$

Fig. 2 shows the small-signal model of the circuit based on an NIC. Assume that the circuit is biased with quiescent currents flowing in the diodes and transistors as intended. Here r_{d1} and r_{d2} are the small-signal resistances of the diodes Q_1 and Q_2, and $r_{\rm in1}$ and $r_{\rm in2}$, are the small-signal input resistances of the transistors of M_1 and M_2, respectively. Let $r_1 = r_{d1} + r_{\rm in1}$ and $r_2 = r_{d2} + r_{\rm in2}$ where, r_1 and r_2 are the total resistances at the two ports of the NIC. Routine analysis of the network in Fig. 2 gives

$$i_2 = A_i i_1 \text{ where, } i_1 = \frac{v_{s1} - v_{s2}}{r_1 - A_{iq} r_2} \quad o(9)$$
$$v_1 = v_2 = v_{s2} - A_i r_2 \frac{v_{s1} - v_{s2}}{r_1 - A_i r_2}. \quad o(10)$$

Thus for the proper operation of the circuit the resistance r_1 at the current-controlled port-l (between the nodes R and $V_{\rm SS}$) must be greater than $A_i r_2$ where r_2 is the resistance at the voltage-controlled port-2 (between S and $V_{\rm SS}$).

Further the voltage-gain of the NIC $A_i r_2/(r_1 - A_i r_2)$ is arranged to be less that unity. If the transistors are operating in strong inversion where $v_{\rm GS}$ is $> V_{\rm THP}$, r_1 and r_2 are given by

$$r_1 = \frac{V_T}{10I} + \frac{1}{2\sqrt{kI}} \text{ and } r_2 = \frac{V_T}{I} + \frac{1}{2\sqrt{nkA_iI}}. \quad (11)$$

From (11) the condition $r_1 > A_i r_2$ reduces to

$$I > 4kV_T^2(A_i - 0.1)^2/\alpha^2. \quad (12)$$

Substituting for I from (6) in (12) shows that $V_{\rm PTAT}$ generated should be greater than $2(A_i - 0.1)V_T$. For a choice of $A_i = 0.6$, $V_{\rm PTAT} > V_T/\alpha$ which is easy to obtain in practice. From (6) for $A_i = 0.6$, $\alpha = [1 - \sqrt{0.6/n}]$. For a choice of $n = 10$, $a = 0.755$ and $k_{\rm eff} = 1.754k$. For $V_{\rm PTAT} = 125$ mV, the current $I \approx 0.56$ μA.

IV. Start-Up

The circuit starts up without the need for any start-up circuit. Transient analysis over process corners and temperature confirms that no start-up arrangement is needed. However, by definition the circuit has two stable operating points at $I = 0$ and $I = 1.4$ μA, or $I = 0.56$ μA, a start-up circuit is incorporated to guarantee the desired mode of operation. The startup circuit is shown in Fig. 1. We used a switch that is temporarily closed at power on, thus forcing the gate of the p-channel transistors $(M_9 - M_{12})$ to a low voltage causing a current to flow [11].This bandgap reference is easy to trim. The simplest of options is to trim the gain m of the current mirror. This is done as described in [12].

V. Design Considerations

Although the bandgap reference source is a dc circuit, its power-supply-rejection is a function of the frequency-response of the sub-circuits controlled by the devices, their gate-source and parasitic capacitances. The power-supply-noise feeds through to the various nodes including the output node via some of these capacitances. Thus, there is a need to keep the devices small to keep the capacitances small at critical nodes. At the same time device-matching considerations require that minimum width and length are not chosen for the devices used to define gains accurately. Further, minimum length is not used where high output resistance is needed to drive current-mirrors. The key issue is to manage the limited head room available for M_2 and M_3. The reason why this becomes possible is because both the diode-voltages as well as the threshold-voltages of all the transistors decrease with temperature.

The key step is the formation of the current I from $V_{\rm PTAT}$ using the current-conveyor [8]. The matching accuracy for the widths of M_1 and M_2 is not stringent because the term n, under the square-root sign in (6), is not critical so long as it is large. However, they cannot be very large because the head room available for the NIC is limited. Note that the transistor M_1 feeds the diode-connected transistor M_3. Thus, the sum $V_{\rm ON1} + V_{\rm ON3} +$

$V_{\rm THN}$ should be less than $V_{\rm BE1}$ to keep M_1 in saturation. Similarly, $V_{SG2} + V_{\rm ON4}$ must be $< V_{\rm BE2}$. Fortunately these conditions can be met.

The cascode transistor M_c helps in providing precision and high output-resistance required for driving the diode-connected transistor M_9. Transistors M_9- M_{12} are scaled such that their widths are in the ratio $1 : (1 + Ai) : 11 : 10$ as required by the design to establish the necessary bias currents in the diodes and the output-circuit as shown in Fig. 1. With a PTAT voltage of 120 mV at room temperature and the gain λ needed given by (1) for $V_{\rm PTAT}$ is about 4.

In addition to a local feedback through the NIC, there is an overall positive-feedback loop which causes the bias currents for the diodes from I. The loop-gain for this is estimated as follows. The small signal conductance g_d of the diode Q_1 carrying a quiescent current I is given by $g_d = 1/r_{d1} = (I/V_T)$. This conductance g_d varies linearly with I. The input conductance g_n looking into the source of M_1 at a quiescent current level I (as seen by Q_1) is $g_n = 1/r_{\rm in1} = 2\sqrt{kI}$. [Thinking in terms of a normalized-variable $\sqrt{x}$ and x representing the two conductances, the idea here can be easily understood by noting the following: $\sqrt{x}$ is $> x$ for $x < 1$, $\sqrt{x} = x$ for $x = 1$ and $\sqrt{x}$ is $< x$ for $x > 1$]. Thus, g_n (proportional to the square-root of I) can conceptually be made greater than g_d (proportional to I) for low values of I to cause regeneration. The two conductances become equal ($g_n = g_d$) at a current level of $I = 4kV_T^2$. The linear function is greater than the square-root function at higher values of I. Thus, the loop-gain can be made to fall below unity at the current level chosen for I. This leads to a stable-state at the required bias point. The feedback factor of the overall positive feedback is evaluated by looking at the current division ratio at the node R. This factor β is given by $\beta = [g_n/(g_n + g_d)]$. The open-loop gain being 11, loop-gain for the feedback loop 11β is computed by evaluating g_n at I and g_d at $10I$. For the choice of $I = 0.56\ \mu$A and $k = 200\ \mu{\rm A/V}^2$, $g_d = 215\ \mu{\rm S} \gg g_n = 21\ \mu$S making the loop gain less than unity and thus the circuit does settle down in the desired stable state.

VI. Simulation Results

The objective of the analysis based on square-law model was only to explain the principle of operation of the circuit and get some insight into the design details. Short-channel transistors do not have square-law characteristics. However, the equations obtained using the simple model enable an initial quantitative prototype design. The actual values needed are obtained by d-c., large-signal as well as temperature analysis. In other words, simulations verify the approximate design but optimization via iteration is needed to obtain the best performance that can be achieved. Thus, the simulation results are presented obtained using real transistor-models for the TSMC 0.18 micron technology.

The channel width W and the length L of the transistors used for simulating the circuit are given in Table I. In order to get good matching of the threshold voltages of the wide and narrow transistors, the traditional layout method is used. Here large W values are obtained by connecting many unit transistors in parallel as well as by interdigitating them in the layout. This scaling is indicated in Table I by a multiplication factor m. Other

TABLE I
Aspect Ratio (W/L) of the Transistors

Component	Size : μm /μm	Component	Size : μm /μm
Q_1	Normalized Area=1	M_5, M_7	10/1, m=5
Q_2	Normalized Area=10	M_6	5/2
M_c	5/2, m=11	M_9	8/4
M_1	5/2, m=2	M_{10}	8/4, m=2
M_2	5/2, m=10	M_{11}	8/4, m=11
M_3, M_4, M_8	10/1	M_{12}	8/4, m=10

TABLE II
Performance of the Bandgap Reference

Tecnologhy TSMC 0.18 μm V_{TP} = -0.39V, V_{TN} = 0.379V		
Specification	I = 1.5 μA	I = 0.56 μA
Supply Voltage	1.4V	1.4V
Nominal Reference Voltage	1.012V	1.08mV
Vref variation with tempt.	$\pm$ 0.25 mV	$\pm$ 0.7 mV
Vref variation with supply	$\pm$ 0.3mV	$\pm$ 0.5mV
Output noise @ 100Hz	5 μV/ $\sqrt{Hz}$	8 μV/ $\sqrt{Hz}$
PSRR @ 1KHz	66dB	53dB
Output resistance	200 Ω	200 Ω
Power Dissipation	45 μW	21 μW

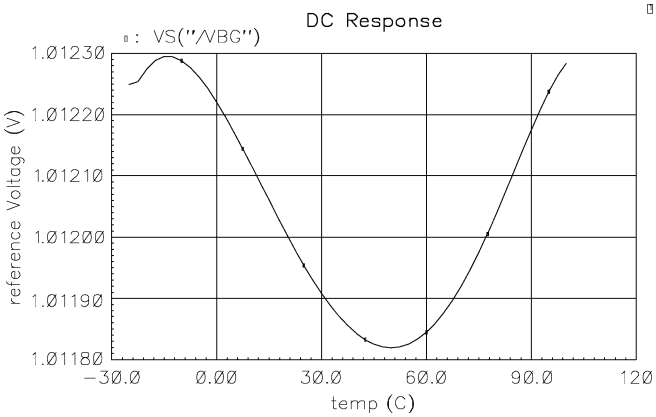

Fig. 3. Reference voltage variation with temperature.

performance details obtained from simulations of the reference source are given in Table II when the current is $I = 1.5\ \mu$A and $I = 0.56\ \mu$A. The figures show the simulation results for $I = 1.5\ \mu$A. Fig. 3 shows the reference output-voltage variation as a function of temperature in the range 0°C–100 °C. The gain for the PTAT voltage is adjusted to obtain the minimum variation over the chosen range. The maximum variation over the temperature range is less than 1 mV. Fig. 4 shows the power-supply rejection of the circuit. The low-frequency rejection is better than 50 dB. The total variation of output voltage over process variation is $\pm 1.8\%$ and thus the trim mentioned earlier is required. The spectral density of noise obtained by simulation at 100 Hz is 5 $\rm V/\mu Hz$.

Table III compares recently published reference circuits. There are two types of references: those based on bandgap [13] and others based on MOS device characteristic [14], [15] such as threshold voltage difference. These are indicated separately in Table III. Simulation results show that this circuit has the lowest temperature coefficient. The reference voltage output of 1.012 V is closer to the full bandgap voltage. In order to achieve less voltage variation most circuits need curvature compensation [16], [17]. This circuit with a power supply as

TABLE III
COMPARISON TO PREVIOUSLY PUBLISHED VOLTAGE REFERENCES

	Bandgap references	Other CMOS references		
	This work	Leung et. al [13]	De Vita et. al [14]	De Vita et. al [15]
Technology	0.18 μ m CMOS	0.6 μ m CMOS	0.35 μ m CMOS	0.35 μ m CMOS
Supply Voltage (V)	1.1 to 1.8	0.98 to 1.5	0.9 to 4	1.5 to 4.3
Vref	1.012V	603mV	891mV	670mV
Supply Current (μ A)	$<$14	$<$18	$<$ 0.055	$<$ 0.11
TC (ppm/C)	4	15	12	10
PSRR@ 100Hz	-75dB	-44dB	-59dB	-47dB
PSRR@ 10MHz	-23dB	-17dB	-52dB	-40dB

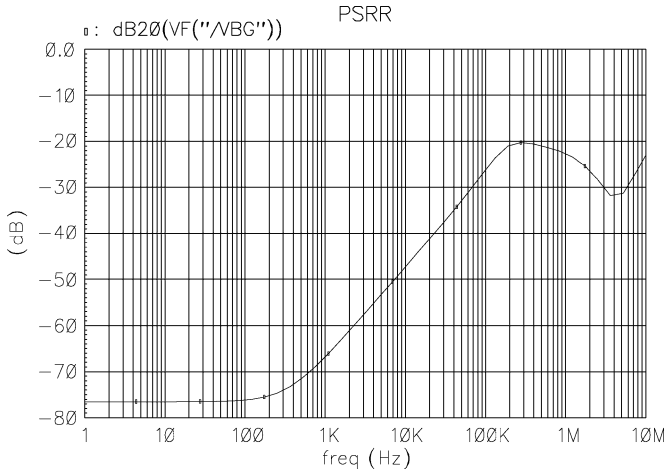

Fig. 4. Power-supply rejection ratio versus frequency.

low as 1.1 V achieves a small voltage variation of 4 ppm/°C for a large range of temperatures without additional circuitry.

VII. CONCLUSION

The principle of operation and design details of a novel CMOS bandgap reference circuit, operable from a supply voltage of nominal value 1.4 V, are presented. The circuit can be fabricated in any standard digital CMOS process. Simulation results using the TSMC 0.18-μm technology show that over process and temperature variations it would start-up and provide the reference output with low-output-resistance and can be resistively loaded. Simulation results show that this reference operates properly with a supply voltage range from 1.1 to 1.8 V. The average output voltage is 1.012 mV, and the total variation is 0.5 mV or 4 ppm/° C with a supply voltage of less than 1.5 V. The simple circuit does not use operational amplifiers or resistors. Simulation results show that this circuit can operate with low currents of 0.5 μA and dissipates 21 μW from a 1.4-V supply voltage, so it is suitable for low power wireless receiver applications.

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