An Ultralow Power Subthreshold CMOS Voltage Reference Without Requiring Resistors or BJTs

Yang Liu, Chenchang Zhan, and Lidan Wang

***Abstract*— This brief presents a novel ultralow power CMOS voltage reference (CVR) with only 4.6-nW power consumption. In the proposed CVR circuit, the proportional-to-absolute-temperature voltage is generated by feeding the leakage current of a zero-V_{gs} nMOS transistor to two diode-connected nMOS transistors in series, both of which are in subthreshold region; while the complementary-to-absolute-temperature voltage is created by using the body diodes of another nMOS transistor. Consequently, low-power operation can be achieved without requiring resistors or bipolar junction transistors, leading to small chip area consumption. The proposed CVR circuit is fabricated in a standard 0.18-μm CMOS process. Measurement results show that the prototype design is capable of providing a 755 mV typical reference voltage with 34 ppm/°C from −15 °C to 140 °C. Moreover, the typical power consumption is only 4.6 nW at room temperature and the active area is only 0.0598 mm^2.**

***Index Terms*— Low-temperature coefficient, ultralow power, voltage reference.**

I. Introduction

TEMPERATURE and voltage insensitive references are crucial for a variety of mixed-signal and RF systems. With the proliferation of mobile devices and wireless sensor networks, reliable voltage references under serious energy constraints have attracted extensive research efforts [1]–[5] recently.

The design in [1] adopts threshold voltage compensation to generate two proportional-to-absolute-temperature (PTAT) factors in order to achieve a better temperature coefficient (TC), yet requires high supply voltage and large power dissipation. The circuit in [2] merely consumes 2.6 nW in room temperature and works with supply voltage as low as 0.45 V, but the TC of 142 ppm/° is unsatisfactory. In [3]–[5], the leakage current of a transistor in subthreshold region is explored to generate a reference with small TC and also with nanowatt or even picowatt power consumption. However, in order to minimize the power consumption, large resistors are required in [3] which occupy a large amount of chip area. The voltage reference generators in [4] and [5] are based on the diode-connected MOS transistors which usually suffer from large process variations. As a result, the generated references show large variations and limited operating temperature range. A clock circuit is adopted in [6] to control the threshold voltage-based reverse bandgap reference, resulting in a reference voltage with excellent TC and accuracy. Still, the microwatt power consumption is not sufficiently low for ultralow power applications [7], [8]. In [9] and [10], with an appropriate current generated from two subthreshold transistors, a temperature insensitive reference voltage is provided at the intermediate point of these two transistors. For most of the articles discussed above, either resistors or special devices such as low-voltage transistors are required to implement the reference circuit. Special devices need extra fabrication steps which increases the chip cost [11], [12]. Although the temperature influence of resistors could be canceled by adopting the ratio of resistance, a tradeoff dilemma of chip area and power dissipation is brought in by using resistors [13], [14].

In this brief, we propose a novel structure of CMOS voltage reference (CVR) without bipolar junction transistors or resistors which achieves a compact area and ultralow power operation [15]. The leakage current of a subthreshold transistor is used to provide the PTAT voltage, while the body diodes of an nMOS transistor with gate-body shorted are used to generate the complementary-to-absolute-temperature (CTAT) voltage.

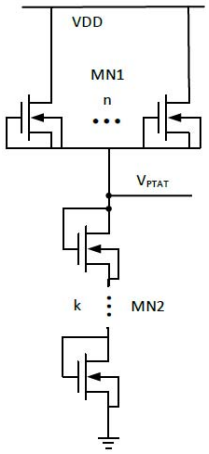

Fig. 1. Schematic of the proposed PTAT voltage circuit.

II. Proposed Voltage Reference

A typical core circuit of a temperature-independent voltage reference consists of a PTAT circuit and a CTAT circuit, which are both implemented by the regular MOS transistors in the proposed CVR design. The design considerations will be discussed in the following sections.

A. Temperature Coefficient

Fig. 1 shows the PTAT voltage generation circuit in the proposed CVR, based on the leakage behavior of the nMOS transistors [3]. Transistor MN1 with a multiplication factor n has zero gate-to-source voltage by shorting its gate and source terminals. Its subthreshold leakage current helps generate the PTAT voltage with diode-connected transistor MN2, which consists of k identical transistors operated in subthreshold region in series in this illustration.

With higher than 100 mV of V_{ds} the MOS transistor current in subthreshold region is approximately given by [2], [10]

$$I_{sub} = I_0 \frac{W}{L} \exp \frac{(V_{gs} - V_{th})}{mV_T} \quad (1)$$

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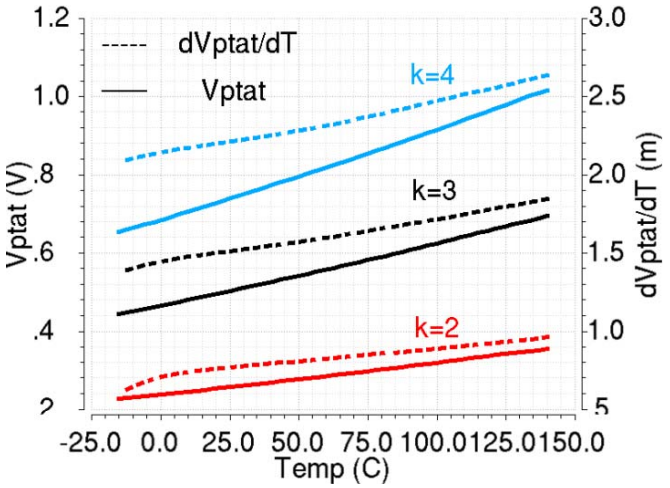

Fig. 2. Simulated PTAT voltage and the corresponding dV_{ptat}/dT with different k values for MN2.

where W and $L$are the channel width and length, respectively, and $V_{\text{T}} = KT/q$ is the thermal voltage.

The I_0 [12] is

$$I_0 = \mu c_{ox}\,(m-1)\,V_T^2 \tag{2}$$

where m is the inverse of the gate-to-surface coupling coefficient, typically having a value of 1.5–2. The term μ is the carrier mobility and C_{ox} is oxide capacitance per unit area.

With MN2 made up by k identical transistors in series, the generated PTAT voltage is readily derived as

$$V_{\text{PTAT}} = kmV_T \ln\left(n\frac{W_1}{W_2}\right) \tag{3}$$

where W_1 and W_2 are the channel width of the elementary transistor of MN1 and MN2, respectively, assuming MN1 and MN2 have the same channel length. As can be seen, the TC of V_{PTAT} can be adjusted by using different k values. Fig. 2 shows the simulated results of the PTAT voltage and the corresponding dV_{ptat}/dT with different k factors. In this design, $k = 2$ is selected for a moderate TC and voltage headroom requirement of V_{PTAT}.

Fig. 3 shows the schematic of the proposed CVR, with $k = 2$ to adjust the slope of the PTAT voltage in compensating the CTAT voltage generated by MN4. The error amplifier circuit is also depicted which uses folded cascade structure with all its transistors working in subthreshold region. The PTAT voltage generated at node A is forced to equal to B due to the error amplifier. In the right branch, instead of using a large resistor, the diode-connected transistor MN3 is used to minimize the power and area consumption. Transistor MN4 is utilized as a two-terminal device with the gate and body shorted and wired to V_{ref} while the source and drain wired to node B. The physical structure of MN4 is shown in Fig. 3 as well. Note that, the gate connection of MN4 does not affect the dc value of the CTAT voltage since the drain and source are shorted. To reduce the noise coupling from VDD and GND, we short the gate to the body. Furthermore, this connection simplifies the layout design as well. The CTAT voltage is produced by the two body diodes formed by the drain and source of MN4 to its body. The current flowthrough MN4 is

$$I_4 = I_s A_4 \exp\frac{V_{\text{ctat}}}{V_T} \tag{4}$$

where A_4 is the area of MN4 parasitic diode. I_{s} is given by [16]

$$I_s = bT^{4-N}\exp\frac{-E_g}{KT} \tag{5}$$

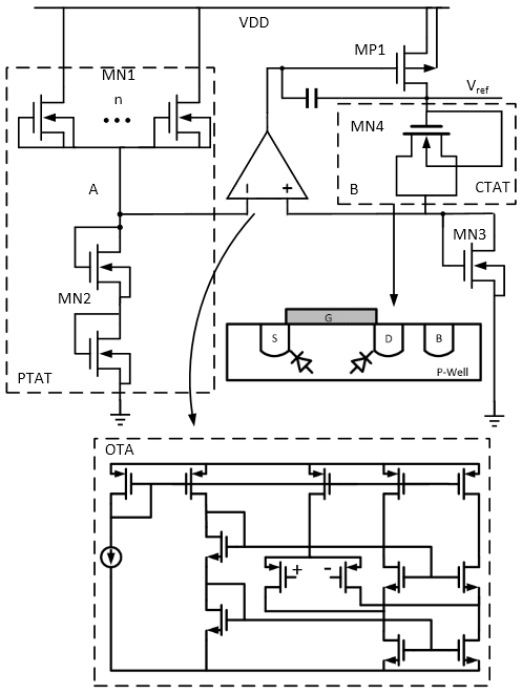

Fig. 3. Proposed CVR circuit.

where b is the proportionality factor and $E_g \approx 1.12$ eV is the bandgap energy of silicon. Adopting (1) to calculate the current of MN3, the CTAT voltage can be derived as

$$V_{\text{ctat}} = \frac{V_{\text{ptat}} - V_{\text{th3}}}{m} - V_T \ln\left(\frac{A_4 L_3}{W_3}\right) - V_T \ln\left(\frac{I_s}{I_0}\right). \tag{6}$$

The temperature insensitive reference voltage is set at V_{ref}, which can be expressed as

$$V_{\text{ref}} = C + BV_T \tag{7}$$

with

$$C = V_{\text{gap}} - \frac{V_{\text{th0}} + \alpha T_0}{m} \tag{8}$$

where α is the TC of threshold voltage, V_{th0} is the threshold voltage at 0 °K temperature, and V_{gap} is the extrapolated diode voltage at 0 °K

$$B = k(m+1)\ln\left(n\frac{W_1}{W_2}\right) + \frac{\alpha \text{q}}{\text{Km}} - \ln\left(\frac{A_4}{K_3}\right) - \ln\left(\frac{bq^2T^{2-N}}{\mu_0 c_{\text{ox}}(m-1)K^2}\right). \tag{9}$$

Hence, ignoring the high order factors, the coefficient B could be set to 0 by sizing the transistors MN1 ~ MN4 carefully. Then the reference voltage can be expressed as

$$V_{\text{ref}} = V_{\text{gap}} - \frac{V_{\text{th0}} + \alpha T_0}{m}. \tag{10}$$

As is the usual case of a CVR circuit, V_{th0} introduced by MN3 lead to more process variations of V_{ref} compared with a bandgap reference.

B. Process Variation and Trimming Circuit

Apparently, process variation challenges the performance of a voltage reference, including our proposed CVR. Neglecting the deviation of W_1/W_2 in (3) since the transistor size is large, the sensitivity to process variation is mainly contributed by the coupling coefficient determined term m. Fig. 4 shows the statistic distribution of the PTAT voltage slope factor and the PTAT voltage value at 27 °C

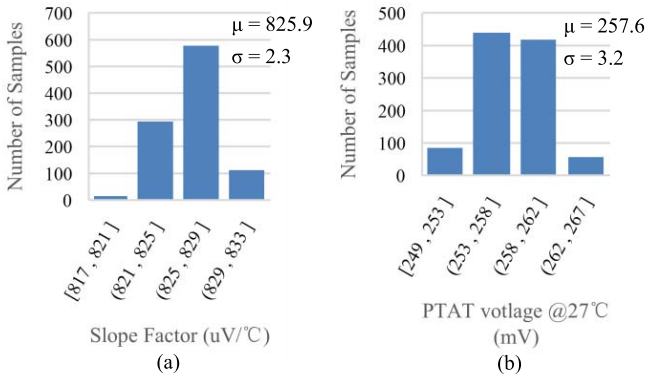

Fig. 4. Distribution of PTAT. (a) Slope factor (uV/°C). (b) Voltage at 27 °C.

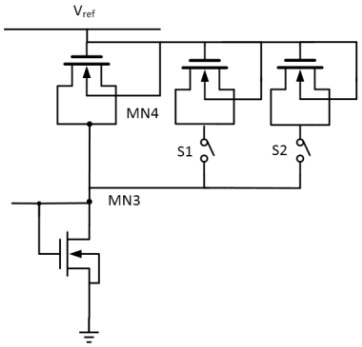

Fig. 5. Trimming circuit.

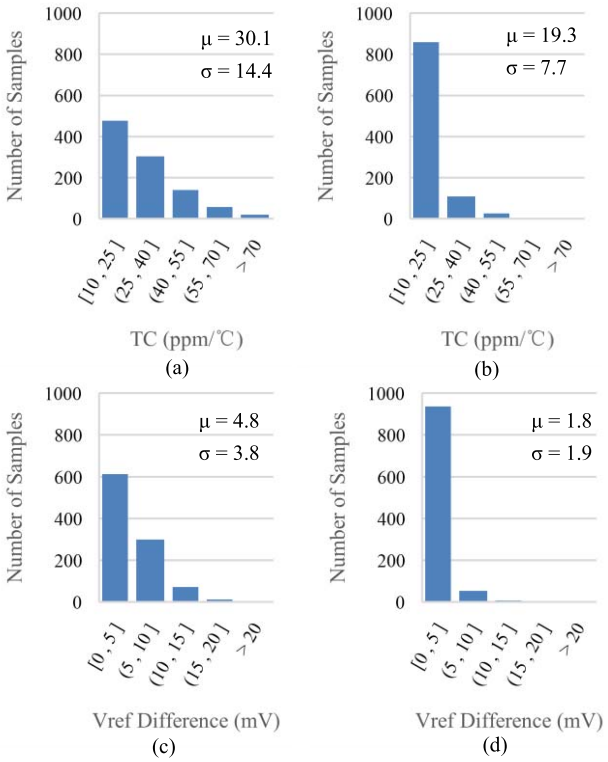

Fig. 6. Distribution of TC. (a) Without trimming. (b) With trimming. V_{ref} difference from average value. (c) Without trimming. (d) With trimming.

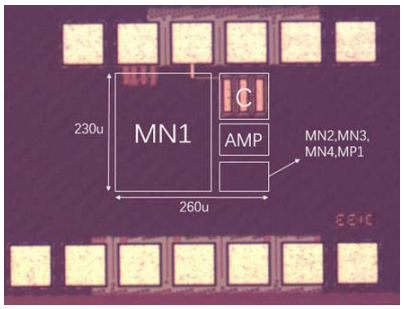

Fig. 7. Chip microphotograph of the proposed CVR circuit.

from 1000-run Monte Carlo simulations. The results show that the standard deviation of the PTAT voltage at 27 °C and its slope factor are only 3.2 mV and 2.3 μV/°C, respectively. For the slope factor which influences the temperature compensation effect, the σ/μ is only 0.28% which leads to an excellent uniformity across the process corners. Hence, the process variation contributes limited influence to the PTAT circuit.

Next, we consider the CTAT circuit. The threshold voltage of MN3 (V_{th3}) and the reverse saturation current (I_0) of the parasitic diode in (6) are all process sensitive. Hence, the CTAT voltage is strongly dependent on process variation. Therefore, a trimming scheme is adopted in the proposed design in order to get small variations in both V_{ref} and its TC. Fig. 5 shows the trimming circuit employed in this design. It is based on changing the channel width of MN4 to vary the CTAT slope factor. By switching S_1 and S_2, there are four possible channel width of MN4 to compensate for the PTAT voltage.

To verify the effect of the trimming circuit, Monte Carlo simulation with 1000-run is done to compare the results of with trimming versus without trimming. The four trimmed circuits with S_1 and S_2 being "00," "01," "10," and "11" are implemented with the untrimmed circuit (which is essentially the same as S_1 and S_2 being "00") in one schematic [13]. The best one is then regarded as the trimmed result. Fig. 6 compares the untrimmed results with the trimmed ones. Fig. 6(a) and (b) shows the TC comparison. The average TC of the untrimmed circuit is around 30.1 ppm/°C with a standard deviation of 14.4 ppm/°C. It is seen that more than 50% of the 1000-run results have larger than 25 ppm/°C TC. On the other hand, the trimmed circuit achieves a TC of 19.3 ppm/°C with 7.7 ppm/°C standard deviation. More than 80% runs provide less than 25 ppm/°C TC, demonstrating significantly improved temperature insensitivity.

For the absolute value of V_{ref}, the deviation from normal value (V_{ref} in typical corner) is adopted here to demonstrate the effectiveness of the trimming circuit. Fig. 6(c) and (d) compares the two results. The mean deviation of V_{ref} from its average value is 4.8 and 1.8 mV for the untrimmed and the trimmed circuit, respectively. Only around 60% samples of the untrimmed circuits have less than 5-mV deviation. On the other hand, there are close to 95% samples that only vary less than 5 mV after trimming.

C. Sizing

Two assumptions about MN1 and MN2 have been made to derive the PTAT voltage in (3).

1) Operating in Subthreshold Region: Biasing MN1 and MN2 in subthreshold region is the condition of the proposed PTAT circuit. However, attributed to hundreds of nano amperes leakage current of MN1 in high temperature, the transistor MN2 will work in saturation region if the ratio of channel width and length is not large enough.

2) Same Threshold Voltage: In order to obtain a PTAT voltage independent of threshold voltage, the V_{th} of MN1 and MN2 must be the same. Thus the channel length of MN1 and MN2 are set to the same value.

The sizes of the main transistors in the proposed design are summarized in Table I. The channel length of MN1 and MN2 is 5 μm, considering the balance of leakage current and chip area.

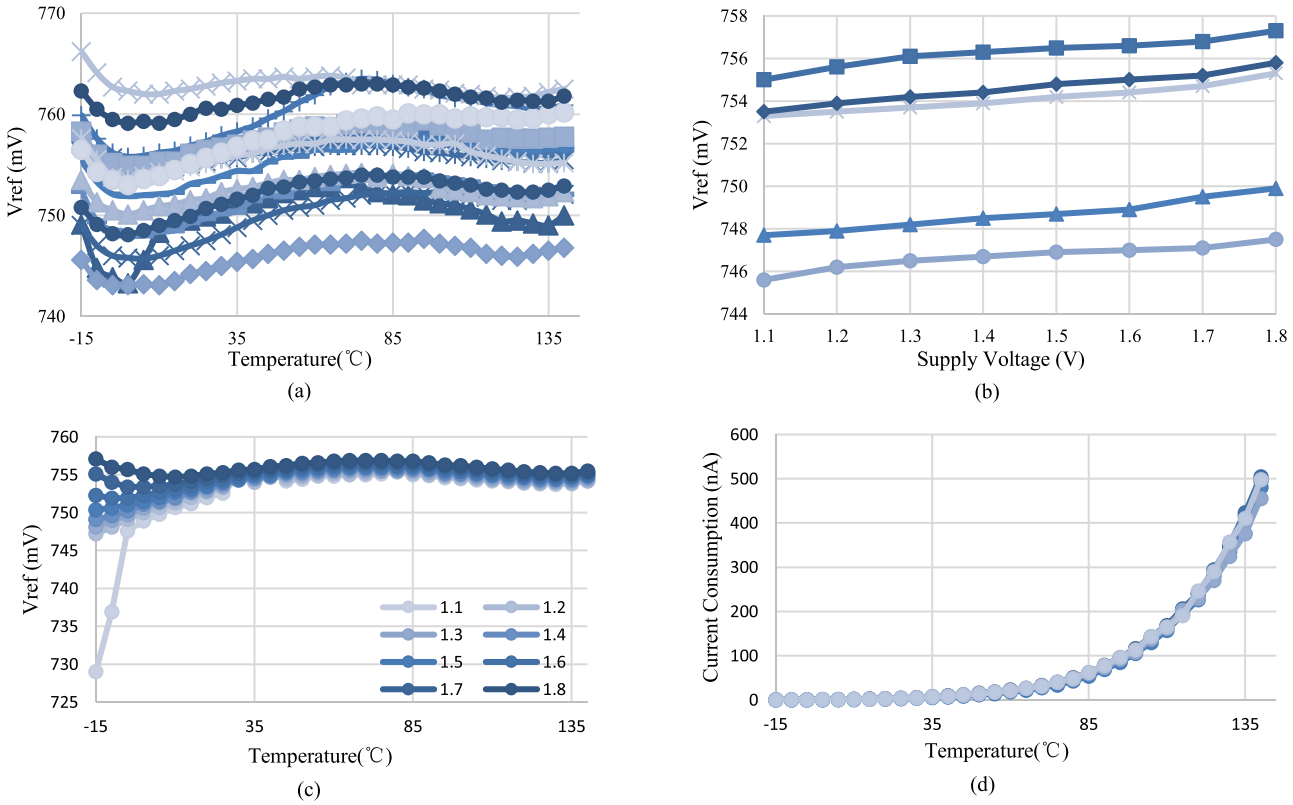

Fig. 8. Measurement results from 15 dies. (a) Curves of the reference voltage in tested dies versus the temperature. (b) Curves of the reference voltage versus supply voltage. (c) Curves of the reference voltage in one die at different supply voltages versus the temperature. (d) Curves of current consumption of 5 dies versus the temperature.

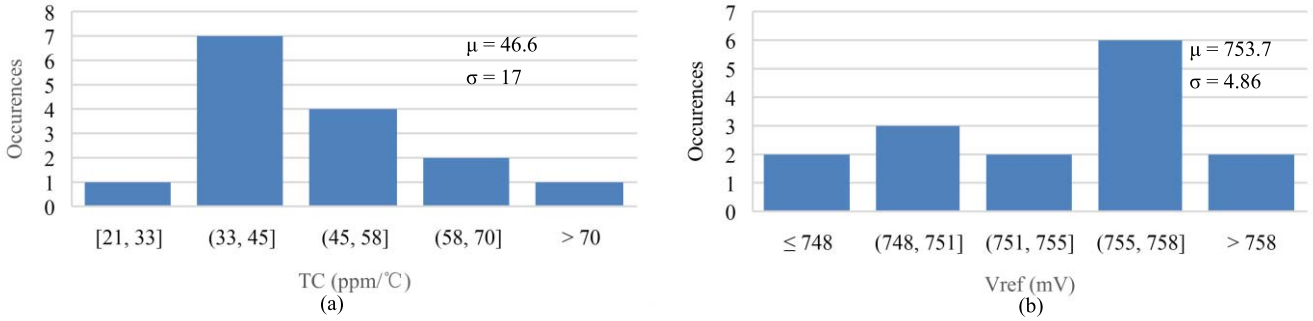

Fig. 9. Distributions of relevant figures for 15 dies. (a) TC at1.8-V supply voltage. (b) Reference voltage at 25 °C.

TABLE I
TRANSISTOR SIZE

Transistor	Channel Length	Channel Width	Finger	Multiplier
MN1	5μ	20μ	10	14
MN2	5μ	33μ	1	1
MN3	15μ	1μ	1	1
MN4	1.8μ	3μ	1	2
MP1	5μ	3μ	1	1

The channel width of MN2 is as large as 33 μ for keeping it in subthreshold region. The W/L of MN3 is as small as 1/15 μm in order to limit the current dissipation of the right branch. The size of MN4 is set appropriately to compensate for the PTAT voltage.

III. MEASUREMENT RESULTS

The proposed CVR circuit is fabricated in a standard 0.18-μm CMOS process. Fig. 7 shows the chip microphotograph. The active silicon area is 0.0598 mm^2. In this measurement, the temperature range is from −15 °C to 140 °C. As the amplifier is self-biased, the CVR cannot work well at the extreme low temperature when the biasing current is too low. More specifically, when the temperature decreases below −15 °C, the current consumption is less than 1 nA.

Fig. 8(a) shows the measured reference voltage dependent on temperature from −15 °C to 140 °C of 15 chips. Typical variation of the reference voltage is around 4 mV at 1.8-V supply voltage, leading to a typical TC of 34 ppm/°C. The measured best TC is 20 ppm/°C while the worst TC is 89 ppm/°C. Note that two-point trimming method is adopted during the measurement, i.e., the measured V_{ref} at −15 °C and 140 °C are trimmed to be as close as possible.

The measured reference voltage of five dies as a function of supply voltage at room temperature is shown in Fig. 8(b). The typical variation of V_{ref} is 2.8 mV, resulting in a line sensitivity of 0.28%/V.

TABLE II
COMPARISON WITH PREVIOUS WORKS

	This work	[3](ISSCC)	[4](VLSIC)	[5](JSSC)	[9](T-CASI)	[11](T-CASII)	[12](JSSC)
Tech(nm)	180	350	180	180	180	180	180
Year	2016	2015	2016	2017	2016	2016	2013
Power(nW)	4.6	29	0.114	0.035	16	40	100
TC(ppm/℃) Min	20	12.75	48	8	25	N/A	N/A
TC(ppm/℃) Typ	34	N/A	N/A	N/A	59.4	58	147
TC(ppm/℃) Max	89	N/A	124	53	240	N/A	N/A
Temp Range (℃)	-15 ~140	-10 ~110	-40 ~85	0 ~100	-40~85	-25~85	-40~120
Area(mm^2)	0.0598	0.48	0.00488	0.0025	0.0132	0.058	0.0294
LR(%/V)	0.28	0.198	0.38	0.31	0.033	0.11	6.5
Samples	15	10	60	60	50	30	9
Vref(mV)	755	1176	986.2	1250	118.4	240	1090
σ/μ(%)@Room Temp	0.64	0.2	1.9	0.8*	4.5	1	0.351
Min Supply Voltage (V)	1.1	1.2	1.2	1.4	0.45	0.8	1.2
PSRR (dB) @10Hz	-9	N/A	-40	-43	-50.3	-62	-62
PSRR (dB) @1M	-47	N/A	-56	N/A	N/A	N/A	N/A
Additional Requirement	N/A	BJT	N/A	0-Vth Transistor	N/A	BJT	BJT

* @0°C~100°C

Fig. 8(c) shows the curves of reference voltage versus temperature of one single die at different supply voltages. The reference voltage only varies around 2 mV under different supply voltages while the temperature is larger than the room temperature. At low supply voltage of 1.1 V, the leakage current will decrease to picoampere at low temperature, which causes the reference voltage with relatively large deviation.

Fig. 8(d) shows the curves of current dissipation versus temperature. Due to subthreshold operation, with increasing temperature, the current flow in the proposed design has an exponential growth. At room temperature, the typical current consumption is only 4.2 nA.

A brief statistical analysis is presented next, where the measured particular mean (μ) and standard deviation (σ) numbers are given. Fig. 9(a) shows the TC distributions. Due to the fact that the worst case TC is around 89 ppm/°C, the mean value of TC is 46.6 ppm/°C which is larger than the typical value (34 ppm/°C). The best TC is 20.5 ppm/°C, which corresponds to the result that the reference voltage varies only by 2.4 mV in the temperature ranges from -15 °C to 140 °C.

The reference voltage distribution at room temperature is shown in Fig. 9(b). The typical reference voltage is 755 mV, which is close to the mean value μ(753.7 mV). The standard deviation σ is only 4.86 mV, showing a σ/μ value of as small as 0.64%.

Table II summarizes the performances of the proposed CVR circuit and compares with a few state-of-the-art designs. Among the designs, the proposed voltage reference achieves very low-power consumption with a good TC and variation performances. Compared with the leakage current-based voltage reference in [2], more than 8× reduction of chip area is obtained. Note that, the power supply rejection ratio performance of this structure is not optimized. Intuitively, the V_{ptat} is a generated by dividing VDD (through MN1 and MN2), hence it is sensitive to the supply voltage. Since the operational amplifier and the CTAT branch jointly buffer the V_{ptat} to V_{ref} (and even with a gain), the V_{ref} is also sensitive to the supply voltage.

IV. CONCLUSION

An ultralow power subthreshold CMOS voltage reference implemented in a 0.18-μm CMOS process has been presented in this brief, based on a pure CMOS implementation without requiring any resistors or bipolar junction transistors. A leakage current-based PTAT technique is used and all the transistors are biased in the subthreshold region, which allow significantly low-power consumption with compact chip area consumption. The nanowatt only power consumption of voltage reference with excellent σ/μ performance makes the proposed design a very attractive choice for low-power applications.

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