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A Resistorless Low-Power Voltage Reference

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***Abstract*—A novel low-power temperature-stable voltage reference without resistors is presented in this paper, which is compatible with standard CMOS technology. In order to reduce the temperature nonlinearity in proposed voltage reference, threshold voltage and a proportional to absolutely temperature (PTAT) voltage form the basic linear-temperature components, which are achieved by resistorless threshold voltage extractor and asymmetric differential difference amplifier. Besides, a self-biased current source with feedback is used to provide stable bias currents for the whole voltage reference, which can improve the power-supply noise attenuation (PSNA) with reduced current mirror errors. Verification results of the proposed voltage reference implemented with 0.18-μm CMOS technology demonstrate that the temperature coefficient (TC) of 14.1ppm/℃ with a temperature range of -20℃ to 80℃ is obtained at 1.35V power supply, and a PSNA of 75.7dB is achieved without any filtering capacitor while dissipating a maximum supply current of 880nA. The active area is 115μm×130μm.**

***Index Terms*—resistorless, low-power dissipation, nonbandgap voltage reference, self-biased current source, power-supply noise attenuation**

I. INTRODUCTION

VOLTAGE references are essential components in many electronic systems, such as data converters, power converters, dynamic random access memories, and radio frequency circuits. Low temperature and power supply sensitivity without modification of the fabrication process are critical requirements of a high-precision voltage reference [1]-[4]. Besides, low power consumption requirement is one of the important design criteria in all systems, especially in battery-operated products or self-powered systems, such as environmental sensors, wireless micro-sensor networks, medical electronics, and energy harvesting applications [3], [5]-[6]. The demand for low-power voltage reference with high precision is increasing.

Conventional voltage references are based on bandgap reference (BGR) circuit, which is one of the most fundamental building blocks in integrated circuits [7]-[8]. A BGR circuit is usually composed by a weighted sum of V_{BE} and thermal voltage. However, due to the nonlinear temperature behavior of V_{BE}, curvature compensation approaches are essential to realize high-precision reference voltage [3]-[5], [9]-[10].

Low-power operation is difficult to achieve in structure with resistors [4]-[5]. Since the current in voltage reference is inversely proportional to the value of resistors, low-power dissipation means high-ohmic resistors. Besides, models for the resistors may not be available or reliable in standard digital CMOS process. Even if there are models for the resistors in the digital process, the area of the resistors is increased because silicide is often used to reduce the block resistance of the polysilicon and diffusion layers. Thus, that not only results in higher cost of the chip, but also worsens immunity of the reference operation to substrate noise coupling [9]. Although low power is much easier to be realized with transistors biased in subthershold regions, the process stability and design flexibility are greatly limited due to the nonlinearity of subthreshold slop parameter and absence of accurate device models, especially in digital CMOS technology [11]-[12].

With the help of complementation linear-temperature terms, a low-power nonbandgap voltage reference without any resistor is presented in this paper. All the MOSFETs in the core of proposed voltage reference are standard CMOS transistors biased in strong inversion regions. Proportional to absolute temperature (PTAT) voltage, V_{PTAT}, and threshold voltage, V_{TH}, are adopted as positive-temperature term and negative-temperature term, respectively. A self-biased current source (SBCS) with feedback is used to provide bias current for the resistorless threshold voltage extractor (RLTVE) circuit and the resistorless thermal voltage extractor circuit with adder functions. Besides, the SBCS can further improve the performance of proposed voltage reference, such as temperature coefficient (TC), and power-supply noise attenuation (PSNA). Based on the characteristics of bias current generated by SBCS, an asymmetric differential difference amplifier (ADDA) is utilized to generate thermal voltage and to achieve a weighted sum of thermal voltage and threshold voltage. In this method, all the aforementioned limitations are avoided.

II. PRINCIPLE OF PROPOSED VOLTAGE REFERENCE

In order to avoid the influence of V_{BE}'s nonlinearity temperature characteristics, threshold voltage with linear temperature dependence is adopted in the proposed voltage

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reference, whose magnitude function is modeled as [13]

$$|V_{TH}(T)| = |V_{TH}(T_0)| - a_{VT}(T - T_0) \quad (1)$$

where T is absolute temperature, T_0 is the reference temperature, $V_{TH}(T_0)$ is the threshold voltage at temperature T_0, α_{VT} is the TC of the threshold voltage, which is usually a positive constant in conventional technologies.

Another critical temperature parameter of MOSFETs is carrier mobility, whose nonlinearity temperature performance has negative effects on the performance of many references as a result of incomplete cancelation [4], [11]. Besides, the nonlinearity temperature performance of subthreshold slope parameter is also a limitation on performance [6].

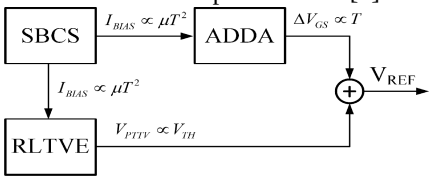

Fig. 1. Systematic block diagrams of the proposed voltage reference

Taken into consideration the influence of nonlinearity temperature components, a novel resistorless voltage reference is proposed in this paper, whose concept is shown in Fig. 1. Except for providing bias currents for other blocks, the SBCS block with feedback is implemented to generate a current I_{BIAS} proportional to μT^2, where μ is the carrier mobility. A weighted PTAT voltage, ΔV_{GS}, can be generated in ADDA with the help of currents proportional to μT^2. By this method, a PTAT voltage, V_{PTAT}, with positive linear temperature performance is successfully obtained. The complementary voltage with negative temperature behavior in the proposed voltage reference is V_{PTTV}, which is proportional to threshold voltage, V_{TH}, of MOSFETs. The RLTVE block is used to extract threshold voltage without resistors. Finally, V_{PTTV} will be injected into ADDA to realize the weighted superposition of threshold voltage and PTAT voltage. It should be noticed that the superposition function is achieved by ADDA at the same time without additional blocks. With regard to the linear temperature characteristics of both threshold voltage and PTAT voltage, there is no nonlinear temperature terms left in the output reference voltage. That makes the TC of proposed voltage reference greatly improved without complex higher-order curvature compensations. Besides, self-bias and local feedback techniques are adopted in the proposed structures to further improve the performance.

As above mentioned, the output reference voltage, V_{REF}, is formed by a weight sum of threshold voltage, V_{TH}, and PTAT voltage, V_{PTAT}, which can be expressed as

$$V_{REF} = V_{TH} + AV_{PTAT} \quad (2)$$

where A is a temperature-independent constant. Given $V_{PTAT}(T)=BT$, where B is a temperature independent constant, the condition for temperature-insensitive reference voltage, viz. $\partial V_{REF} / \partial T = 0$, can be given by

$$a_{VT} = AB \quad (3)$$

Therefore, the output voltage of the proposed reference can be stable at '$V_{TH}(T_0)+ \alpha_{VT}T_0$' without the influence of nonlinear temperature parameters.

III. Circuit of Proposed Voltage Reference

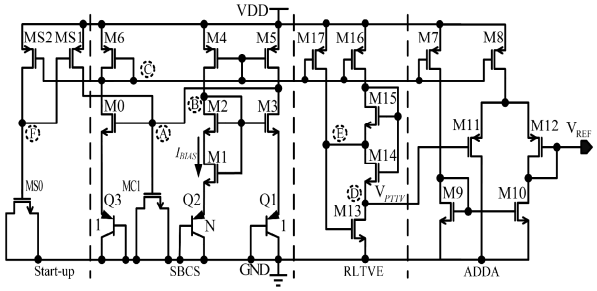

Fig. 2. Schematic of the proposed voltage reference

The implementation of proposed voltage reference is shown in Fig. 2. The detail analysis will be given in the following.

A. SBCS with Feedback

The SBCS with embedded feedback is shown in the left of Fig. 1. All the MOSFETs used in SBCS are biased in strong inversion region without the requirement of subthreshold operations. While MOS transistors M1 and MC1 operating in the triode region, the other transistors used in SBCS are biased in active region. Transistors M1 - M5, Q1 and Q2 constitute the core circuit of the proposed current source. M1 acts as a dynamic resistor converting corresponding voltage to current.

Given the ratio of current mirrors, formed by M4, M5, and M6, is 1:1:1, the source voltages of M2 and M3 should be equal with $S_{M2}=S_{M3}$, where S_i is the aspect ratio of transistor i. With the help of voltage-current characteristics of BJTs in active region, the drain-source voltage of M1, $V_{DS(M1)}$, is a PTAT voltage, $V_T \ln N$, where N is the emitter area ratio of transistors Q2 and Q1, V_T is the thermal voltage kT/q, k is Boltzmann's constant and q is an electron charge. In addition, the gate-source voltage of M1, $V_{GS(M1)}$, can be expressed as $V_{GS(M1)} = V_{GS(M2)} + V_{DS(M1)}$, where $V_{GS(M2)}$ is the gate-source voltage of M2. According to the voltage-current relationship of MOSFETs in triode region and active region, current I_{BIAS} can be given by

$$I_{BIAS} = \frac{mC_{OX}S_{M1}^2}{2S_{M2}}(V_T \ln N)^2 \left(1+\sqrt{1+(S_{M2}/S_{M1})}\right)^2 \quad (4)$$

where C_{OX} is the gate-oxide capacitance per unit area. The temperature dependence of carrier mobility can be expressed as in [4] and [13] $\mu=\mu(T_0)(T/T_0)^{\beta}$, where $\mu(T_0)$ is the carrier mobility at temperature T_0, and β is the temperature power of mobility, which is usually between -1.5 and -2. Therefore, formula (4) can represented as

$$I_{BIAS} = k_1 T^{2+b} \quad (5)$$

where $k_1=(k\ln N)^2\mu(T_0)C_{OX}[1+(1+\gamma)^{0.5}]^2 S_{M1}/(2q\gamma T_0^{\beta})=k_1' S_{M1}$ $\mu(T_0)C_{OX}/T_0^{\beta}$ and $\gamma=S_{M2}/S_{M1}$ are temperature-independent constants. The current I_{BIAS} is controlled by aspect ratios of M2 and M1. Low power consumption can be realized by small $(W/L)_{M1}$ and large $(W/L)_{M2}$. Besides, it can be noticed that bias current generated by SBCS is a nonlinear-temperature dependent term, which is related with carrier mobility. That will

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be used as bias currents for RLTVE and ADDA. With the help of the temperature characteristics of bias current, a weighted PTAT term can be achieved in ADDA. Therefore, a self-biased current I_{BIAS} is generated with the benefit of improved performance of proposed voltage reference [4], [14].

In order to further improve the stability of bias current without decreasing voltage headroom, feedback loops are adopted in the proposed SBCS to suppress the variation influence, such as power supply fluctuation, crosstalk, and so on. Combined with the core circuit of proposed SBCS, the branch, formed by transistors M0, M6, MC1, and Q3, is utilized to form closed feedback loops. Transistor MC1 is used as capacitor to make the whole loop more stable. The whole loop transfer function can be described as

$$T_0 \approx (\frac{g_{mN}}{1+g_{mN}/g_{mQ}})^2 R_{M1}[(r_{oN}+\frac{1}{g_{mQ}}+\frac{r_{oN}g_{mN}}{g_{mQ}}) \| r_{oP}] \quad (6)$$

$$P_{\text{dominant}} \approx \frac{1}{2p[(r_{oN}+1/g_{mQ}+r_{oN}g_{mN}/g_{mQ}) \| r_{oP}]C_{MC1}} \quad (7)$$

where g_{mN} and g_{mQ} are the transconducrances of NMOSFETs with the same size and current of M0 and those of the Q1 – Q3, respectively; r_{oN} and r_{oP} are the output resistances of NMOSFETs with the same size and current of M0 and those of PMOSFETs with the same size and current of M6, respectively; R_{M1} presents equivalent the on-resistance of M1; C_{MC1} is the equivalent capacitance of MC1.

With the help of feedback control in the SBCS, the voltage at nodes A and B can be clamped at the same voltage potential by properly setting the sizes of M0 and Q3. Besides, the voltage difference variations between these two nodes can be greatly reduced without the requirement of long channel devices.

The start-up circuit for the SBCS is made up of PMOS transistors MS0, MS1 and MS2, where transistor MS0 acts as a capacitor. When the proposed voltage reference is power on, the voltage at node F is low to turn MS1 on. By this method, a charge current is generated to increase the voltage at node A. When the voltage at node A is high enough to make M0 turned on, the voltage at node C is pulled down and there are currents flowing into the core circuit of SBCS to set up proper operating points. At the same time, transistor MS2 turns on to slowly increase the voltage at node F. Since the voltage at node F will be finally pulled up to supply voltage V_{DD}, MS1 will be turned off, and MS2 will enter deep-linear region. Thus, the proposed SBCS can successfully avoid degenerate states without extra power consumption and influence on the normal operation of the current generator in steady state.

B. RLTVE

The middle part of Fig. 2 is the proposed RLTVE, which is used to extract the required linear-negative-temperature term, threshold voltage. All the transistors, except M14, work in the active region. Transistor M14 is biased in triode region. Given $S_{M17}=2S_{M16}$, $S_{M13}=3S_{M14}=3S_{M15}$, the over-drive voltage of M13 and M15 should be equal, i.e. $V_{OV(M13)}=V_{OV(M15)}=V_{OV}$. According to the Kirchhoff's theorem, $V_{GS(M14)}=V_{GS(M15)}+V_{DS(M14)}$. Based on the voltage-current relationship of MOSFETs in strong inversion region, the voltage difference between nodes E and D is equal to V_{OV}. The output voltage of proposed RLTVE, V_{PTTV}, can be expressed as

$$V_{PTTV} = V_{TH(\text{M13})} \quad (8)$$

where $V_{TH(M13)}$ is the threshold voltage of M13. Therefore, V_{PTTV}, which is proportional to threshold voltage (PTTV), is successfully obtained without any resistor. This means V_{PTTV} has a strong linear negative temperature behavior without the nonlinear temperature influence of carrier mobility.

C. ADDA

With the help of the generated bias current in SBCS, a weighted PTAT term can be realized in ADDA, which is shown in the right part of Fig. 2. Besides, output reference voltage, V_{REF}, which consists of PTAT and complementary to absolute temperature (CTAT) terms, is also achieved in ADDA structures at the same time. All the transistors are biased in active region.

The proposed method used to realize PTAT is based on the bias current characteristics, rather than that based on inverse function in [15]. According to the characteristics of MOSFETs in active region, the voltage difference between the gates of M12 and M11 can be described as

$$\Delta V_{SG} = \sqrt{2/(mC_{OX})}(\sqrt{I_{M11}/S_{M11}} - \sqrt{I_{M12}/S_{M12}}) \quad (9)$$

where I_i represents the drain current of transistor i. Due to the asymmetric behavior of ADDA, the voltage ΔV_{SG} will not be zero.

The bias current for ADDA is determined by the generated current I_{BIAS} in SBCS. Given $I_{M17}=k_2I_{BIAS}$, $I_{M18}=k_3I_{BIAS}$, $S_{10}=k_4S_9$, the current through transistors M11 and M12 are $(k_3-k_2k_4)I_{BIAS}=k_5I_{BIAS}$ and $k_2k_4I_{BIAS}=k_6I_{BIAS}$, respectively. That means all of current in ADDA is proportional to $T^{2+\beta}$. Substituting (5) into (9), ΔV_{SG} could be rewritten as

$$\Delta V_{SG} = dT \quad (10)$$

where $\delta=(k_1'S_{M1}/S_{M12})^{0.5}[(k_5S_{M12}/S_{M11})^{0.5}-(k_6)^{0.5}]$, is a temperature independent constant. It can be noticed that the input voltage difference of ADDA is a PTAT voltage without the influence of carrier mobility and other process parameters. The weighting factor for PTAT term is without the requirement for exact value of device sizes except ratios. Since the process variations of ratios are quite limited, the weighted PTAT voltage is quite stable with process.

Combined with (8) and (10), the output voltage of the proposed voltage reference, V_{REF}, can be given by

$$V_{REF} = V_{TH(\text{M13})} + dT \quad (11)$$

Therefore, a resistorless temperature-stable reference voltage can be achieved in the proposed reference structure with the help of two linear-temperature voltages. Based on the characteristics of generated bias current in SBCS, a weighted PTAT voltage is realized in the ADDA. Then, the voltage is superimposed on a threshold voltage extracted by the RLTVE without additional circuit. Coefficient δ, which is only formed

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by ratios, is used to cancel the TC difference between the threshold voltage and the PTAT voltage. The effect of mobility's nonlinear temperature dependence is completely removed.

With regard to (1), the TC of the proposed voltage reference can be set to zero with the condition of $\delta=\alpha_{VT}$. The output reference voltage can be stable around '$V_{TH}(T_0)+\alpha_{VT}T_0$' by this method.

IV. VERIFICATION RESULTS AND DISCUSSION

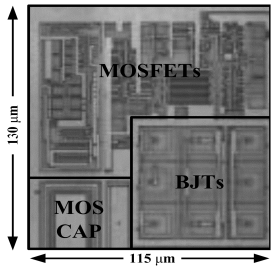

Fig. 3. Chip micrograph of the proposed voltage reference

The proposed voltage reference shown above has been successfully implemented in 0.18-μm CMOS technology. α_{VT} is about -0.94mV/℃, and V_{TH} is around 0.41V. The chip micrograph of the proposed voltage reference is shown in Fig. 3, and the active area is 115μm×130μm.

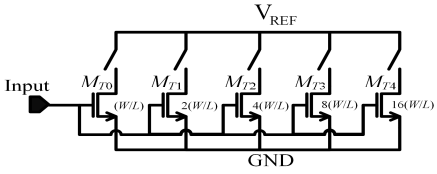

Fig. 4. Schematic of the programmable device ratio array

With regard to the performance of voltage reference, process variations and mismatches have a significant influence. As a result of the device ratios used in the proposed voltage reference, the mismatch effect can be greatly reduced with proper matching techniques during circuit implementation [14]. Besides, trimming is an important method in voltage reference to compensate the influence for process variations [5], [16]-[17]. Based on the expression of output reference voltage in the proposed structure, the equivalent sizes of devices in current mirrors are chosen as the trimming target in the proposed structure, which can be taken as a current trimming technique. The gain of the current mirror, which comprises of M9 and M10 shown in Fig. 2, is selected as the trimming object in the proposed circuit. A digital-controlled binary-weighted aspect ratio adjustment is adopted with M10, which is shown in Fig. 4 [12], [14]. The input terminal in Fig. 4 is connected to the gate node of M9 and M10. By this method, the programmable devices are placed in parallel with transistor M10. In the proposed design, the trimming is achieved by a 5-bit trimming of the equivalent aspect ratio for M10. That can adjust the gain of current mirror within ±30.8%, whereas the nominal value of the current mirror is 1. In this process, two temperature points measurement is sufficient for temperature trimming with optimized TC performance, while one temperature point measurement is sufficient for value trimming without specialized TC considerations.

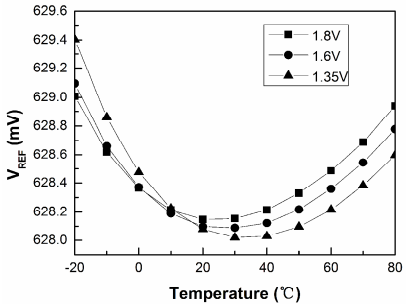

Fig. 5. Measured temperature dependence at different supply voltages

The trimmed output voltage V_{REF} of the proposed voltage reference has a deviation of 0.161% with temperature ranging from -20℃ to 80℃ at 1.6V power supply. The minimum TC is 13.6ppm/℃ and the maximum TC is 22ppm/℃ with power supply ranging from 1.35V to 1.8V shown in Fig. 5. It can also be noticed that the line regulation at room temperature is around 298μV/V. The results illustrate that the output reference voltage is quite stable with temperature and supply variations. That benefits from the presented voltage reference structure. With regard to (1) and (11), the TC of output voltage should be zero in ideal. The degenerated performances in reality are mainly introduced by the following aspects. Firstly, the exact temperature dependency of threshold voltage is not linear, whose TC decreases with temperature rising [4], [16]. Secondly, the body bias of M1, M2, M14 and M15 in Fig. 2 is different. The influence of body bias in SBCS is introduced by the threshold voltage difference between M1 and M2. As analyzed in section Ⅱ. A, the source voltage difference between M2 and M1 is equal to $V_T\ln N$. Since the difference is quite small, the impact on the generated bias current is less than 5%. Besides, the body bias difference of M14 and M15 in RLTVE can introduce ignored influence with $\Delta V_{TH}<<V_{OV}$, where ΔV_{TH} is the threshold voltage difference between M15 and M14. In the proposed design, ΔV_{TH} is set at $0.07\times V_{OV}$ to minimize the effect. The last one is the nonideality of the practical circuit.

Fig. 6 shows a similar plot of five samples without trimming and with trimming. Before trimming, the TC of output reference voltage is in the range of 14.4ppm/℃ to 44.4ppm/℃, and the average TC of 24.6ppm/℃ is achieved. With trimming aiming to minimize the temperature dependence of proposed voltage reference in five references respectively, the difference between the maximum voltage exhibited by any of these references and the minimum exhibited by any of these references between -20℃ and 80℃ is within 1.5 mV peak to peak. The TC of proposed voltage reference is from 7.4ppm/℃ to 23.2ppm/℃ with an average of 14.1ppm/℃.

Table I summarizes a comparison on the results of proposed voltage reference and other voltage references reported in literature, which were fabricated with a CMOS process without resistors. Except [5] and [18], other voltage references are realized with standard CMOS technologies. The TC of the proposed voltage reference is comparable to [4], [12], [18], but

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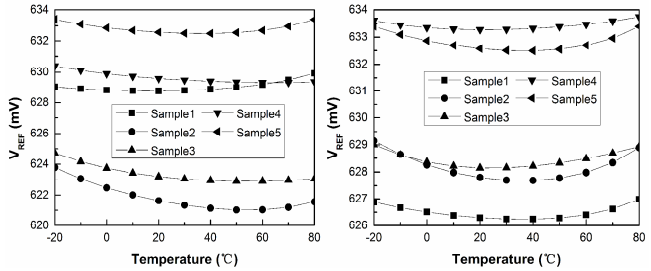
Table I
Summary of the Performance of the Proposed Voltage Reference

	Proposed	Zhou et al [4]	Osaki et al [5] *	Buck et al [9]	Ueno et al [12]	Lee et al [18] *	Zhao et al [19]
Technology	0.18μm CMOS	0.35μm CMOS	0.18μm CMOS	0.5μm CMOS	0.35μm CMOS	0.35μm CMOS	0.35μm CMOS
Accuracy Samples	5	5	9	4	17	10	1
Supply Voltage	1.35-1.8 V	1.85-4.5 V	1.2-1.8 V	3.7	1.4-3 V	1.4-3 V	2.4-5 V
Supply Current	0.88 μA (max)	65 μA (max)	0.083 μA	378 μA	0.214 μA	0.0205 μA	—
VREF (V)	0.630	0.9055	1.09	1.121	0.745	1.176	1.124
TC (ppm/℃)	14.1	14.8	147	120	15	12.75 (min)	65
Line Regulation	0.298 mV/V	—	—	—	0.015 mV/V	2.328 mV/V	3.462 mV/V
PSNA@DC	-75.7 dB	-61 dB	-59 dB	-43 dB	-45 dB	—	-49.2 dB
Chip Area (mm^2)	0.015	0.01	0.029	0.4	0.055	0.48	—

*Twin-well CMOS technology is required.



(a) (b)

Fig. 6. Measured temperature dependence of five samples. (a) Without trimming (b) With trimming

smaller than [5], [9], [19]. Although there is only minimum TC in [18] stated, the minimum TC of proposed voltage reference is 7.4ppm/ ℃ , which is better. Since transistors biased in subthreshold region are quite suitable for low power consumption applications, the supply current of [5], [12], [18] is smaller than that of the proposed voltage reference. In order to highlight the significance of comparison, those voltage references in [4], [9], [19] with only MOS transistors biased in strong inversion or cutoff region are adopted. The power consumption is the smallest among voltage references without subthreshold transistors. In addition, the PSNA is superior to other voltage references.

V. CONCLUSION

Based on the linear-temperature complementation of threshold voltage and PTAT voltage, a high-precision low-power nonbandgap voltage reference has been proposed and implemented by standard 0.18μm CMOS technology, which has no requirement of resistors or subthreshold transistors. A RLTVE circuit is presented to obtain threshold voltage of transistors. Combined with an SBCS circuit and an ADDA circuit, the input voltage difference of ADDA is made proportional to absolute temperature, and the superposition of the two linear-temperature terms is realized at the same time. Since no additional component is needed, the proposed voltage reference is completely compatible with digital CMOS technologies.

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