Low-dropout Regulator Design: Project Description

Overview

A low-dropout regulator (LDO) is a cost-effective power management IC that can create a high-quality analog supply from the unregulated input. Capacitor-free LDO, or output capacitor-less LDOs are particularly desirable since it removes the need for an external pin and PCB surface mount component.

In this project, your team will design a capless LDO in TSMC 16 nm ADFP.

Specifications

You will need to meet the following specifications in a typical design condition. A typical design condition is defined as (1) Typical NMOS, Typical PMOS, (2) 25°C temperature, (3) Supply voltage $V_{IN} = 1.8V$.

Parameters	Min	Typical	Max	Unit
Input voltage	1.62	1.8	1.98	V
Output voltage		1.2		V
Minimum output current		50		uA
Maximum output current	50			mA
Quiescent current		10		uA
DC Output accuracy	-3%		3%	percentage
Output capacitance range	0		100	pF
Power supply rejection ratio (PSRR) at DC	40			dB
PSRR at 20 kHz		25		dB

You are encouraged to meet as many specifications as possible at corner design conditions. Corner design conditions are defined as any combination of (1) process corners, (2) temperature variations, (3) supply voltage variations, (4) device mismatch.

Topology Choice

Your team will get 90% discount in your grade if you choose to use an NMOS device as output. You will get 20% bonus if you choose PMOS as the output device.

There are a lot of literature and resources on capless LDO designs. Please as you explore your design options [1]–[4].

Submission

A powerpoint slide showing the following:

1. Schematic snapshot of the LDO
2. Schematics of all test benches (ADEXL or maestro view)

3. Simulation Plan & Results
4. Specification Compliance Matrix:
5. Reference & IP location on the server.

Grading Rubric

Meeting as many specifications as possible.

Transient performance was not specified. However, better transient performance will be rewarded. Report your transient performances in waveforms, overshoot, undershoot, recovery time (5%), and FoM [5].

Example of a SCM:

	Specifications			Simulation results over PVT			
Parameters	Min	Typ.	Max	Min	Typ.	Max	Unit
Input voltage	1.62	1.8	1.98	1.62	1.8	1.98	V
Output voltage		1.2		1.165	1.203	1.230	V
Minimum output current		50			50		uA
Maximum output current	50			50	55	70	mA
Quiescent current		10		6.5	10	15	uA
DC Output accuracy	-3%		3%	-2.9%		1.0%	%
Output capacitance range	0		100	0		100	pF
Power supply rejection ratio (PSRR) at DC	40			38	50	60	dB
PSRR at 20 kHz		25		22	30	39	dB
Undershoot (50uA to 50mA in 1us)					100	340	mV
Overshoot (50 uA to 50mA in 1us)					45	200	mV
Recovery time (5% accuracy)				8.4	10	21	us
FoM					TBD.	TBD.	ps

(Meeting spec: in green. Not meeting spec: red.)

References

[1] K. N. Leung and P. K. T. Mok, “A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation,” *IEEE Journal of Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, Oct. 2003, doi: 10.1109/JSSC.2003.817256.
[2] E. N. Y. Ho and P. K. T. Mok, “A Capacitor-Less CMOS Active Feedback Low-Dropout Regulator With Slew-Rate Enhancement for Portable On-Chip Application,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 2, pp. 80–84, Feb. 2010, doi: 10.1109/TCSII.2009.2038630.
[3] S. K. Lau, P. K. T. Mok, and K. N. Leung, “A Low-Dropout Regulator for SoC With Q-Reduction,” *IEEE Journal of Solid-State Circuits*, vol. 42, no. 3, pp. 658–664, Mar. 2007, doi: 10.1109/JSSC.2006.891496.
[4] R. J. Milliken, J. Silva-Martinez, and E. Sanchez-Sinencio, “Full On-Chip CMOS Low-Dropout Voltage Regulator,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 9, pp. 1879–1890, Sep. 2007, doi: 10.1109/TCSI.2007.902615.
[5] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, “Area-efficient linear regulator with ultra-fast load regulation,” *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 933–940, Apr. 2005, doi: 10.1109/JSSC.2004.842831.