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Research Article

Design Method for Two-Stage CMOS Operational Amplifier Applying Load/Miller Capacitor Compensation

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Keywords

CMOS Analog Integrated Circuit,
Compensation Circuit,
Miller Capacitor,
Operational Amplifier,
Nulling Resistor.

Abstract

CMOS operational amplifiers (Op-amp) are present integral components in various analog circuit systems. Adding frequency compensation elements is the only critical solution for avoiding Op-amp instability. This article presents a designed two-stage CMOS Op-amp using a miller capacitor, a nulling resistor, and a common-gate current buffer for compensation purposes. All the design parameters of the proposed Op-amp were determined based on the corresponding equations of gain, slew rate, phase margin, power dissipation, etc. In order to verify the parameter values, the developed Op-amp circuit was simulated in HSPICE, possessing two critical characteristics: Op-amp with miller capacitor and a robust bias circuit. Afterwards, the expected values from the theoretical section were compared with simulation results thus proving that the advanced method in this paper was validly designed and implemented. This technique promises a real-world scale Op-amp with high unity-gain, excessive input common-mode range voltage, reasonable gain bandwidth, and a practicable slew rate.

1. Introduction

1.1. Lecture Review

Operational amplifiers (Op-Amps) are principal element in an analog system. System stability is fundamental in various research areas such as voltage stability employing voltage regulators and capacitors [1, 2]. A two-stage Op-amp utilizes miller compensation for stability, engendering a right half-plane (RHP) zero in the open-loop gain from a forward pass through the compensation capacitor, which, in turn, reduces the maximum gain-bandwidth (GBW). Several methods are applied to resolve the forward pass, including Nulling Resistor, Voltage Buffer, Current Buffer, and Current/Voltage Buffer. As the most popular and straightforward, the Nulling Resistor technique enables the implementation of MOS transistors, creating a left half-plane (LHP) zero with increased gain-bandwidth. Inversely, Voltage Buffer proves higher gain-bandwidth, while Current Buffer technique, a common-gate, boasts remarkable efficiency of the gain-bandwidth and Power Supply Rejection Ratio (PSRR) performance [3]. Moreover, the Current Buffer method can be enhanced if the cascode differential stage is designed in place of a simple differential stage. The maximum gain-bandwidth is limited by the 2nd pole, which depends on the load capacitor. The current buffer can be divided into four segments: 1- Separate and additional common-gate stages (with an LHP Zero and without RHP zero) [4]. 2- Embedded in cascode first-stage loads (with an LHP Zero and without RHP zero) [5]. 3- Embedded in CASCODED differential pairs (with an LHP Zero and an RHP zero) [6]. 4- Current mirrors stages (with an LHP Zero

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and without RHP zero) [7]. The combination of all above methods with the addition of miller compensation is applied to compensate for the right half-plane zero. Furthermore, the Voltage Buffer system is significantly accurate, showcasing a simple common-drain, generating a left half-plane zero by higher gain-bandwidth. Although, GBW is equal in both the Nulling Resistors and Voltage Buffer approaches, the latter reduces the output swing [8-10].

In order to design the Op-amps that operate the negative-feedback connection, the frequency compensation is essential for close-loop stability [11, 12]. Frequency compensation produces a risk for other performance parameters; therefore, well-implemented Op-amp is required for a compensation strategy. However, attaching a miller capacitance series to the Nulling Resistor is one method of creating an RHP zero. Moreover, the minimal value of Miller capacitance is imperative in reducing noise and improving output power. Consequently, optimization of the noise and output power systems play major roles in the Op-amp design [13-16].

Two-stage CMOS is the most common configuration utilized when designing Op-amps [17]. The 1st stage is defined by a differential input and single-ended output, and the 2nd stage is considered as an inverted output stage. The gain of both stages is achieved between 40dB to 100dB. The addition of an RC network to the system results in frequency compensation, while removing the feed forward path from the 1st stage to the Op-amp, allows Op-amp to degrade the stability [18, 19]. During the designing stages, a well-known fault diagnosis method was utilized to check the designed Op-amps status [20, 21]. Output results of previous studies illustrated that the load capacitance increased up to 100PF can improve the frequency of PSRR [22]. Designing a CMOS Op-amp with high unity-gain bandwidth, DC gain, and output swing requires a two-stage amplifier. The problem with this configuration is reduced speed due to the extra poles and zeros. The result is found in cascode frequency compensation. This system displays greater speed and PSRR than miller compensation, adding a capacitor between the low impedance node of the 1st stage and output node of the 2nd stage. A potential advantage of this system is that the energy production takes place near the consumer, which can minimize the power losses in the distribution lines [23]. Hybrid cascode, a complicated method of cascode compensation, has higher amplifier bandwidth than the standard cascode approach and miller methodologies [24, 25]. Two-stage Op-amps are selected in this study because of their improved DC gain and ample output swing. Another method to improve frequency compensation is adding a miller capacitor to the Op-amps and using the objective function to obtain the threshold for the sale of reactive energy [26]. The issue of feedforward signal path that creates (RHP) zero in the Op-amp is addressed by designing a series resistor or voltage/current buffer with a miller capacitor [10].

1.2. Contributions

While it is important to consider all variables in a perfect design, this project focused on the optimization of the main simulated parameters as follows:

- Gain (A_V)
- Unity-gain frequency
- Power dissipation
- Input Common-Mode Range: V_{CMR}
- Output swing: $V_{out(max,min)}$
- Slew Rate: SR
- Phase margin: ϕ_M

More specifically, the acquired methodological technique was carried out in three goals:

<u>*First goal:*</u> Design and calculate the element values (W/L, Cc, and R_b) of the circuit depicted in Figure 1 and Figure 2 [27].

<u>*Second goal:*</u> Analyze the circuit and calculate the parameters, namely DC gain (A_0), Power Supply Rejection Ratio (PSRR), Common-Mode Rejection Ratio (CMRR).

<u>*Final goal:*</u> Compare simulated and manual results.

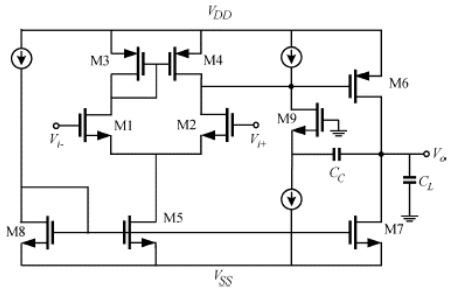


Figure 1. Two-stage operational amplifier with miller capacitor and common-gate current buffer.

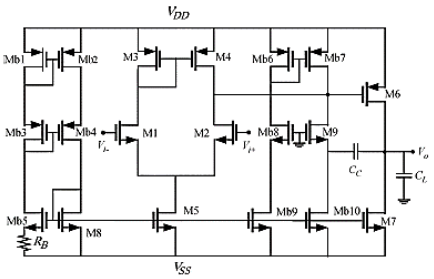


Figure 2. Operational amplifier with bias current circuit.

2. System Design and Modeling

2.1. Operational Amplifier Compensation

Typical two-stage Op-amp (Figure 1) can be illustrated as the following diagram [28]:

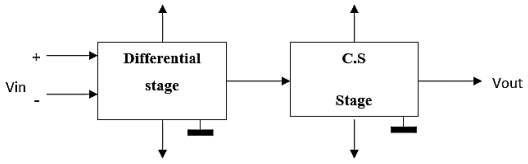


Figure 3. Typical two-stage Op-amp

According to Figure 4, the 1st stage is a differential amplifier, and the gain and pole frequency of this stage can be calculated by Eq. (1).

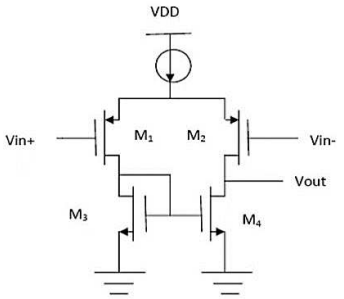


Figure 4. COMS differential input stage

$$A_1 = g_{m1}\left(r_{ds2} \,||\, r_{ds1}\right),\ \omega_1 = \frac{1}{C_{out}\left(r_{ds2} \,||\, r_{ds4}\right)} \quad (1)$$

The dominant pole (C_{out}) of this stage is defined for Derain-Bulk (C_{DB}) capacitances of M_4 and M_2 transistors. The other pol and zero created by M_3 and M_1 can be disregarded. According to Figure 5, the 2nd stage is a common-source (C.S), and applying the composition of the cascade has capability to increase the gain, specifically after having compensation by miller in this stage. Although high gain leads to lower bandwidth, this article proposed the trad-off between gain and bandwidth. The gain and pole frequency of this stage is obtained by Eq. (2). The dominant pole is related to the Drain-Bulk capacitor (C_{DB}) of M_6 and M_7 transistors [29].

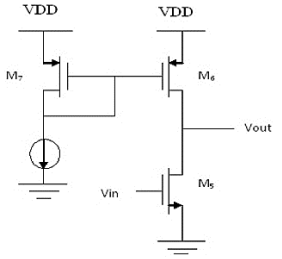


Figure 5. Common-source amplifier stage.

$$A_2 = g_{m6}\left(r_{ds7} \,||\, r_{ds6}\right),\ \omega_2 = \frac{1}{C_{out}\left(r_{ds5} \,||\, r_{ds6}\right)} \quad (2)$$

Single-stage amplifiers usually have an acceptable frequency response with a phase margin of 90°, supposing that GBW (gain-bandwidth) is 10 times more than pole value. According to the low DC gain of single-stage operational amplifiers, they require at least two or more stages to have a multipolar system. Poles contribute to the phase reduction and phase margin might incline to zero before reaching unity-gain frequency, therefore, negative or zero phase margin indicates an oscillated system. Compensation methods are explained by techniques and processes to increase the phase margin that causes the stability of close-loop circuit. After designing an Op-amp and its connections in the different stages, Op-amp would be exposed to instability. In this case, some methods were presented for compensation of this instability. Hence, two important methods are explained in the following.

2.1.1. Techniques of Operational Amplifier Compensation

- Parallel Compensation

In this primary technique of an Op-amp compensation, a capacitor is designed in parallel with an output load resistance of the common-source stage to correct the pole. Since implementing the large value of capacitances takes up much of the space on a chip, this method is usually not approved in the integrated circuits [30].

- Pole Splitting_Single Compensation Miller Capacitor (SCMC)

A miller compensation capacitor decreases the value of the dominant pole for a two-stage Op-amp and propels the output poles away from the source. This phenomenon is named pole splitting, and it is an accustomed method in the design of operational amplifiers. Moreover, a miller compensation capacitor (Cc) is connected in parallel with the 2nd stage as demonstrated in Figure 6. Miller theory proved in Figure 7 that a parallel impedance with a gain stage can be replaced by two impedances located from input to ground and from output to ground.

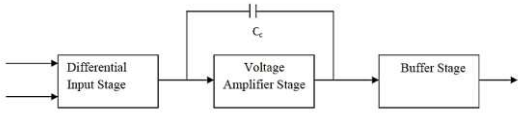


Figure 6. Implementation of pole splitting (miller compensation)

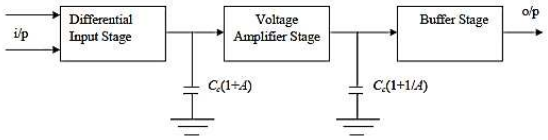


Figure 7. Miller equivalent circuit in Figure 6

In this case, the equivalent input capacitor value is Cc(1+A) where A is the gain of a stage. In order to apply a large capacitance to decrease the dominant pole, another small capacitance (capacitor compensation) is required with a high gain. Before starting pole splitting, the pole values are:

$$\omega_1 = \frac{1}{R_1 C_1}, \omega_2 = \frac{1}{R_2 C_2} \quad (3)$$

Where C_1, R_1, C_2, and R_2 are output resistances and capacitances of each stage. After compensation, these frequencies were changed as shown below:

$$\omega_1 = \frac{1}{R_1\left(C_1 + C_C\left(1+A\right)\right)}, \omega_2 = \frac{1}{R_2\left(C_2 + C_C\left(1+\frac{1}{A}\right)\right)} \quad (4)$$

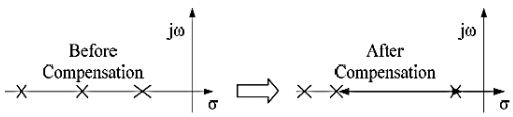


Figure 8. Pole splitting

While increasing compensation leads to sustainability, decreasing the dominant pole caused bandwidth reduction. Therefore, this method drawback is existing some difficulties to maintain the bandwidth.

- Miller Capacitor Compensation with R_Z

The presence of zero in the conversion function is able to increase the phase shift and the speed of reducing the gain value, in turn, causes the movement to an instability. There are some methods to eliminate this effect, and one of them is applying a series resistor with the miller capacitor. In this technique, the zero should be moved to remove the effect of the first non-dominant pole. In fact, the value of R_Z is

selected to equalize the zero-frequency value with the first non-dominant pole-frequency value [31].

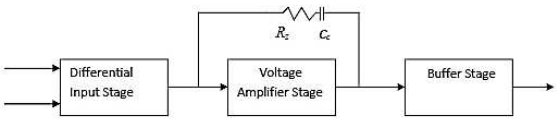


Figure 9. Adding the R_Z in series with compensation capacitor

The advantages of an operational amplifier with current buffer are: 1- Good GBW, 2- High PSRR, 3- Improved slew rate (low Cc value), 4- Area efficient (low Cc value), 5- Power and area trade-off, 5- No output swing reduction (unlike voltage buffer), and its disadvantages are: 1- Gain reduction, 2- Low noise performance, 3- Increased offset.

2.1.2. Techniques of Operational Amplifier Design

To simplify the design process, many high-order effects were excluded, and the following equations were calculated in the simulation design [32].

$$I_D = \frac{u_{n.p}C_{ox}}{2}\left(\frac{W}{L}\right)V_{eff}^2,\ g_m = \sqrt[2]{2u_{n.p}C_{ox}\frac{W}{L}I_D},\ g_m = \frac{2I_D}{V_{eff}} \quad (5)$$

$$V_{eff} \xrightarrow{NMOS} V_{GS} - V_{th},\ V_{eff} \xrightarrow{PMOS} V_{SG} - V_{th}$$

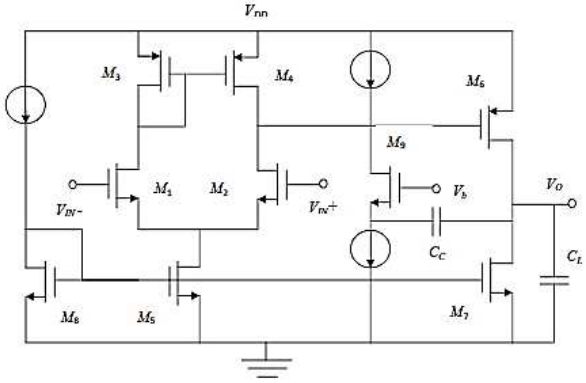


Figure 10. Two-stage CMOS Op-amp with a miller capacitor and a common-gate current buffer

According to Figure 11 and its conversion function (Eq. (6)), for a proper design of MOSFET, V_{eff} parameter should be defined between 200mV and 250V for ambient temperature.

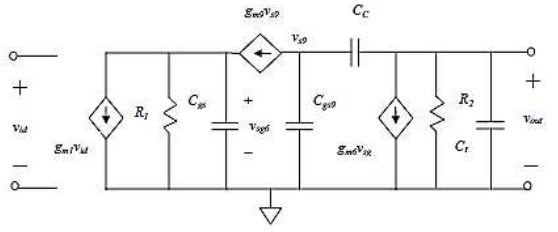


Figure 11. Equivalent small-signal circuit of the Op-amp in Figure 10

$$A(s) \cong \frac{\omega_u}{s} \times \frac{1 + s\frac{C_C + C_{gs9}}{g_{m9}}}{s^2\left(\frac{C_L C_{gs6}}{C_C g_{m6}} \times \frac{C_C + C_{gs9}}{g_{m9}}\right) + s\left(\frac{C_L C_{gs6}}{C_C g_{m6}} \times \frac{C_{gs6}}{g_{m6}}\right) + 1} \quad (6)$$

$$\omega_u \cong A_0\omega_{p1} = \frac{g_{m1}}{C_C} \rightarrow A_0 = g_{m1}g_{m6}R_1R_2,\ \omega \cong \frac{1}{g_{m6}R_1R_2C_C}$$

Where ω_u is unity gain-frequency, A_0 is the DC gain, and ω_{p1} is dominant pole frequency.

- Operational Amplifier Equation

According to Figure 10, V_{HR}^{out} is calculated by Eq. (7).

$$V_{HR}^{out+} = V_{DD} - V_{out(\max)},\ V_{HR}^{out-} = V_{out(\min)} - V_{SS}$$
$$V_{HR}^{out+} = V_{eff\,6},\ V_{HR}^{out-} = V_{eff\,7} \quad (7)$$

- Common-Mode Range

According to Figure 10, the common-mode range is calculated by Eq. (8).

$$V_{HR}^{CM-} = V_{CM(\min)} - V_{SS},\ V_{HR}^{CM+} = V_{DD} - V_{CM(\max)}$$
$$V_{HR}^{CM+} = V_{eff\,3} - V_m,\ V_{HR}^{CM-} = V_{eff\,5} + V_m + V_{eff\,1,2} \quad (8)$$

- Internal Slew Rate (SR)

The internal S.R is correlated to Cc.

$$SR = \frac{I_{D5}}{C_C} \quad (9)$$

- External Slew Rate

The external S.R is correlated to C_L.

$$SR = \frac{I_{D7} - I_{D5}}{C_L} \quad (10)$$

Eq. (11) is concluded by a combination of Eq. (9) and Eq. (10).

$$I_{D7} = SR(C_C + C_L),\ I_{D5} = 2I_{D1} = 2I_{D2} \rightarrow V_{eff} = \frac{SR}{\omega_u} \quad (11)$$

- Offset Voltage Minimization

Offset is created by the asymmetrical current in the output stage, for instance, I_{D6} and I_{D7} are asymmetrical with no input voltage.

$$\begin{cases} I_{D3} = I_{D4} = \frac{I_{D5}}{2},\ V_{DS4} = V_{SD3} \\ V_{SG6} = V_{SD4},\ V_{SD3} = V_{SG3},\ V_{SG3} = V_{SG6} \end{cases} \rightarrow \frac{I_{D6}}{I_{D3}} = \frac{2I_{D6}}{I_{D5}} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_3} \quad (12)$$

Reducing the asymmetrical current in the output stage:

$$\frac{I_{D7}}{I_{D5}} = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_5} \rightarrow \frac{\left(\frac{W}{L}\right)_{5,8}}{2\left(\frac{W}{L}\right)_{3,4}} = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_6} \quad (13)$$

2.2. Spectrum Density of Input Thermal Noise

The spectrum density of input thermal noise is calculated by Eq. (14) for two-stage Op-amp.

$$S_n(f) = 4kT\left\{2\left(\frac{2}{3g_{m1,2}}\right)\right\}\left[1+\frac{g_{m3,4}}{g_{m1,2}}\right],\ g_{m3} = \frac{C_C SR}{V_{HR}^{CM+}+V_{th}}$$
$$S_n(f) = 4kT\left\{2\left(\frac{2}{3\omega_u C_C}\right)\right\}\left[1+\frac{SR}{\omega_u\left(V_{HR}^{CM+}+V_{th}\right)}\right] \quad (14)$$

According to Figure 10, the Op-amp power dissipation and according slew rate is:

$$P = (2I_{D5}+I_{D7})V_{\sup} \rightarrow P = SR(3C_C+C_L)V_{\sup} \quad (15)$$

2.3. Compensation and Phase Margin Technique

According to Eq. (6), all the non-dominant poles were equal and real, and P_3 removed the conversion function of the limited pole, and final conversion function and phase margin were acquired by following equations.

$$\frac{g_{m9}}{C_C+C_{gs9}} = \frac{g_{m6}}{C_{gs6}}$$
$$B(s) = s^2\left(\frac{C_L C_{gs6}}{C_C g_{m6}}\times\frac{C_C+C_{gs9}}{g_{m9}}\right)+s\left(\frac{C_L C_{gs6}}{C_C g_{m6}}+\frac{C_{gs6}}{g_{m6}}\right)+1 \quad (16)$$

$$p_3 = -\frac{g_{m9}}{C_C+C_{gs9}} = -\frac{g_{m6}}{C_{gs6}},\ p_2 = -\frac{g_{m6}C_C}{C_{gs6}C_L},\ z = -\frac{g_{m9}}{C_C+C_{gs9}} \quad (17)$$

$$A(s) \cong \frac{\omega_u}{s}\times\frac{1}{1-\frac{s}{p_2}},\ \phi_M = \tan^{-1}\frac{|p_2|}{\omega_u} = \tan^{-1}\frac{\omega_{T6}C_C}{\omega_u C_L} \quad (18)$$

$$\omega_{T6} = \frac{g_{m6}}{C_{gs6}} = \frac{3u_p}{2L_6^2}V_{eff\,6},\ L_6 = \sqrt{\frac{3u_p V_{eff\,6}C_C}{2\omega_u C_L\tan\phi_M}}$$
$$I_{D9} = \frac{\left(\tan\phi_M\,\omega_u C_L\right)^2\left(C_C+\frac{2}{3}W_9L_9C_{ox}\right)^2}{2u_n C_{ox}\left(\frac{W_9}{L_9}\right)} \quad (19)$$

Eq. (19) indicates a trade-off between the power dissipation and compensation circuit level on the chip.

3. Theoretical Analysis

The designed circuit was carried out in six sections, as shown in Figure 12:

1. M_1 & M_4 transistors: Differential input stage.
2. M_6 & M_7 transistors: High-gain amplifier stage.
3. M_7, M_8, M_5 & M_{b1}-M_{b10} transistors: Bias current supply of transistor.
4. M_9 transistor: Resistance.
5. M_1 & M_2 gate of the transistors: Input bases.
6. M_7 & M_6 drain of the transistors: Output bases.

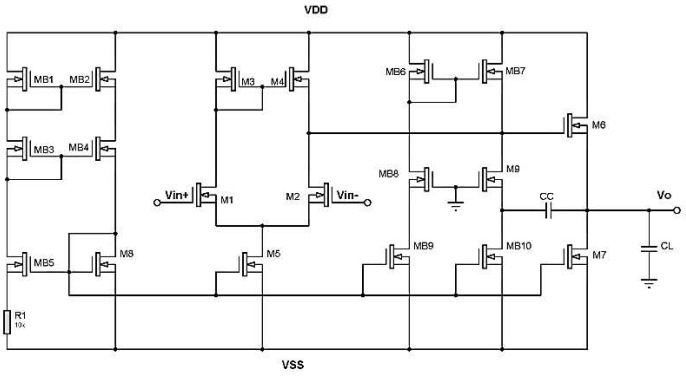


Figure 12. Op-amp with a robust bias circuit

According to Table 1, the parameters shown in Figure 12 have to be calculated in the first step, and the design process might be modified to improve the output results. Initial assumptions for NMOS and PMOS transistors are considered:

$$\xrightarrow{NMOS} K_n = 146.1\ \frac{\mu A}{v^2},\ \lambda_n = 0.3\ V^{-1},\ v_{thn} = 0.7V$$

$$\xrightarrow{PMOS} K_p = 47\ \frac{\mu A}{v^2},\ \lambda_p = 0.3\ V^{-1},\ v_{thp} = -0.9V$$

Table 1. Calculated parameters for the design process

C_C (PF)	I_5 (μA)	I_1=I_2 (μA)	I_3=I_4 (μA)	I_6 (μA)
1	5.5	2.75	2.75	44.7
$(\frac{W}{L})_{1,2}$	$(\frac{W}{L})_5$	$(\frac{W}{L})_6$	$(\frac{W}{L})_{3,4}$	$(\frac{W}{L})_7$
1.22	4.81	47.6	2.92	41.62
$(\frac{W}{L})_8$	$(\frac{W}{L})_9$	$(\frac{W}{L})_{b1-b4}$	$(\frac{W}{L})_{b5}$	$(\frac{W}{L})_{b6-b7}$
4.81	2.7	1.6	6.4	131
$(\frac{W}{L})_{b8}$		$(\frac{W}{L})_{b9-b10}$		
27		2.3		

3.1. Voltage Gain

$$A_V = \frac{V_{out}}{V_{in}} = \frac{g_{m2}}{g_{ds2}+g_{ds4}}\times\frac{g_{m6}}{g_{ds6}+g_{ds7}} = \underline{82.23\ dB} \quad (20)$$

3.2. Input Common-Mode Range

$$\begin{cases} ICMR^+ = V_{DD} - |V_{t3}| - \sqrt{\frac{2I_3}{K_3\left(\frac{W}{L}\right)_3}} + V_{t1} = 2.1\ V \\ ICMR^- = V_{SS} - \sqrt{\frac{2I_5}{K_n(\frac{W}{L})_5}} + \sqrt{\frac{2I_1}{K_n(\frac{W}{L})_1}} + V_{t_1} = 2.1\ V \end{cases} \quad (21)$$

3.3. Power Dissipation

$$\begin{cases} p_{diss}^{+} = V_{DD}(I_8 + I_5 + I_6 + I_{b6}) = 155.475\ \mu W \\ p_{diss}^{-} = V_{SS}(I_8 + I_5 + I_6 + I_{b6}) = 155.475\ \mu W \end{cases}$$
$$\rightarrow p_{diss}^{s} = 310.95\ \mu W$$
(22)

3.4. Maximum Amplitude of Symmetrical Output Signal

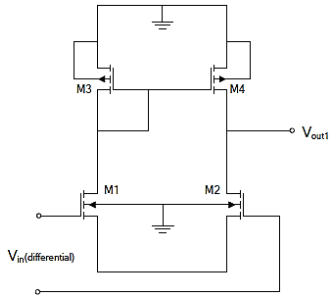
$$\begin{cases} V_{O(\max)} = V_{DD} - \sqrt{\dfrac{2I_6}{K_p\left(\dfrac{W}{L}\right)_6}} = 2.31\ V \\ V_{O(\min)} = V_{SS} + \sqrt{\dfrac{2I_7}{K_n\left(\dfrac{W}{L}\right)_7}} = 2.37\ V \end{cases} \quad (23)$$

3.5. Slew Rate

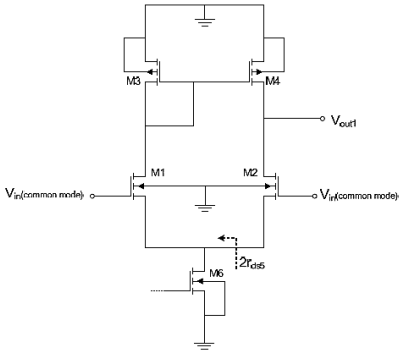
$$\begin{cases} \text{Internal } S.R = \dfrac{I_5}{C_C} = 5.5\ V/\mu\text{sec} \\ \text{External } S.R = \dfrac{I_6}{C_L} = 8.94\ V/\mu\text{sec} \end{cases} \quad (24)$$

3.6. Common-Mode Rejection Ratio (CMRR)

Equations of the common-mode and differential gains are calculated based on Figure 13(a) and (b).



(a)



(b)

Figure 13. Equivalent circuit for calculating (a) differential gain of the 1st stage; (b) common-mode gain of the 1st stage

$$\begin{cases} |A_d| = \dfrac{V_{out1}}{V_{in}(differential)} = \dfrac{gm_2}{g_{ds4} + g_{ds5}} \cong 279.63 \\ |A_c| = \dfrac{V_{out1}}{V_{in}(differential)} \cong \dfrac{r_{ds4}}{2r_{ds5}} = \dfrac{g_{ds5}}{2g_{ds4}} = 1 \end{cases}$$
$$\rightarrow CMRR = \left|\frac{A_d}{A_c}\right| = 280 \cong \underline{49\ dB}$$
(25)

3.6. Spectrum Density of Input Thermal Noise

$$\begin{cases} S_n(f) = 4kT\left\{2\left(\dfrac{2}{3\omega_u C_C}\right)\right\}\left[1 + \dfrac{SR}{\omega_u\left(V_{HR}^{CM+} + V_{th}\right)}\right] \\ V_{HR}^{CM+} = V_{eff\,3} - V_{thn} = -0.25\ V \end{cases} \quad (26)$$
$$\rightarrow S_n(f) = \underline{4.55 \times 10^{17}}$$

After determining all the parameters in the theoretical section, Figure 14 was simulated in HSPICE software to authenticate all the calculated elements in the two-stage CMOS operational amplifier employing the current buffer.

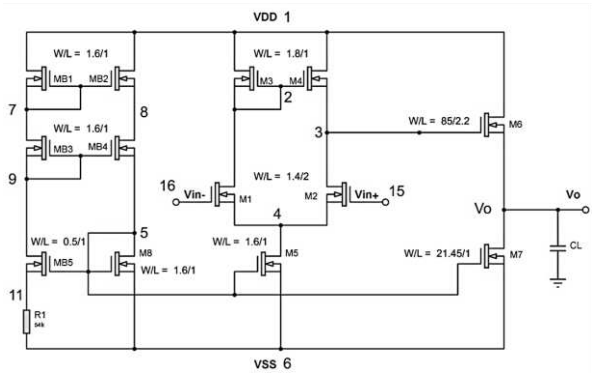


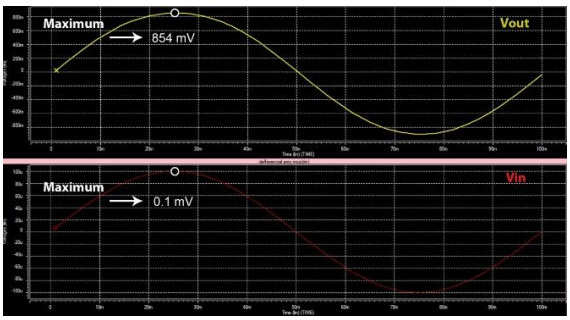
Figure 14. Two-stage CMOS operational amplifier employing the current buffer

4. Simulation Analysis

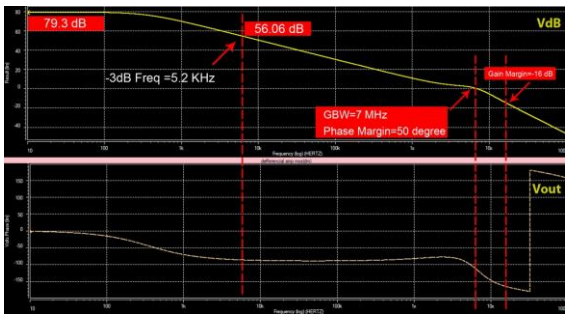
The aim of the simulation analysis using HSPICE software is to verify the simulated parameters with their values in Table 1.

4.1. Two-Stage Operational Amplifier without Compensation

First, a two-stage Op-amp was studied without compensation based on Figure 14. its gain value and frequency response were then checked, compensation was added to the circuit, and the two were compared. The following figures prove that amplifier gain is 79.3dB, and Figure 15 illustrates the frequency response, phase margin, gain margin, GBW for operational amplifier without compensation.



(a)



(b)

Figure 15. Parameter values of two-stage operational amplifier without compensation

Notably, this circuit is not perfectly stable, and it might fluctuate during the time. Table 2 is extracted from Figure 15.

Table 2. Small signal (AC) analysis of the circuit without compensation

Gain Bandwidth	ω-3dB	Unity Gain	Phase Margin	Gain
7MHz	5.2kHz	-16dB	50°	79.3dB

4.2. Two-stage Operational Amplifier with Miller Capacitor and Nulling Resistor

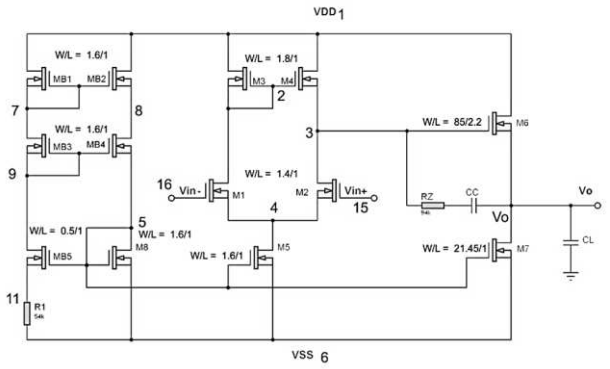
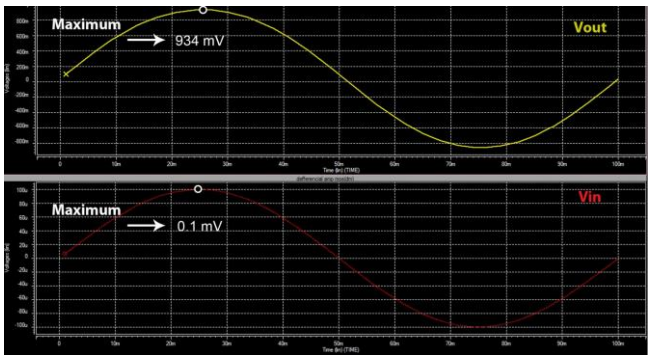
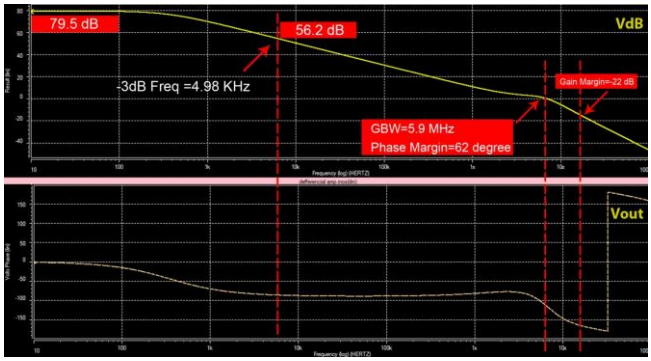


Figure 16. Two-stage operational amplifier employing miller capacitor and nulling resistor

In this design, the nulling resistor and miller capacitor were defined as R_Z= 94kΩ and C_C= 0.5PF. Figure 17 illustrates the AC analysis of the operational amplifier shown in Figure 16. The values of the obtained parameters are grouped in Table 3.



(a)



(b)

Figure 17. Parameter values of two-stage operational amplifier without C_C capacitor and R_Z resistor

Table 3. Small signal (AC) analysis of the circuit with compensation (C_C and R_Z)

Gain Bandwidth	ω-3dB	Unity Gain	Phase Margin	Gain
5.9MHz	4.98kHz	-22dB	62°	79.5dB

After comparing Table 2 and Table 3, adding compensation reduced the gain bandwidth, ω_{-3dB}, and unity gain and increased the gain and phase margin.

4.3. Two-stage Operational Amplifier Employing Current Buffer with Compensation

According to Figure 10, this section depicts two-stage Op-amp with miller capacitor and common-gate current buffer, and its analysis is similar to the simulated open-loop operational amplifier as demonstrated in Figure 18. After simulating this circuit in HSPICE, the parameters for nine transistors were acquired listed in Table 4. Afterward, the AC and DC analyses are shown in Figure 19, and 500.0736μW was calculated as a total power dissipation in the circuit.

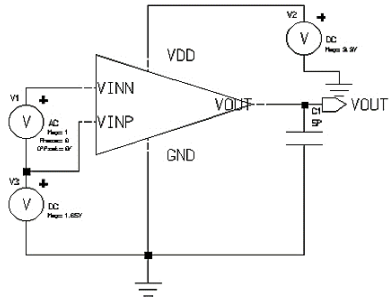


Figure 18. Proposed structure for simulated open-loop frequency response of operational amplifier

Table 4. Important parameters of nine transistors in Figure 10

Parameter	M_1 NMOS	M_2 NMOS	M_3 PMOS	M_4 PMOS	M_5 NMOS	M_6 PMOS	M_7 NMOS	M_8 NMOS	M_9 NMOS
Legion	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation	Linear
W/L	1.4/2	1.4/2	1.8/1	1.8/1	1.6/1	85/2.2	21.45/1	1.6/1	27/1
Id (mA)	0.93	0.93	-0.93	-0.93	1.86	-93.38	93.38	1.88	1
gm	11	11	10.91	10.91	23.21	499.86	619.18	23.44	3.71
Vds (V)	2.46	2.46	-1.35	-1.35	1.17	-2.43	2.56	1.35	950µ
Vgs (V)	1.32	1.32	-1.35	-1.35	1.35	-1.35	1.35	1.35	1.36
Vth (V)	1.18	1.18	-1.21	-1.21	1.21	-1.02	1.08	1.21	1.08
gds (V)	44.12n	44.12n	47.47n	47.47n	141.2n	2.02µ	4.35µ	139.1n	1.04m

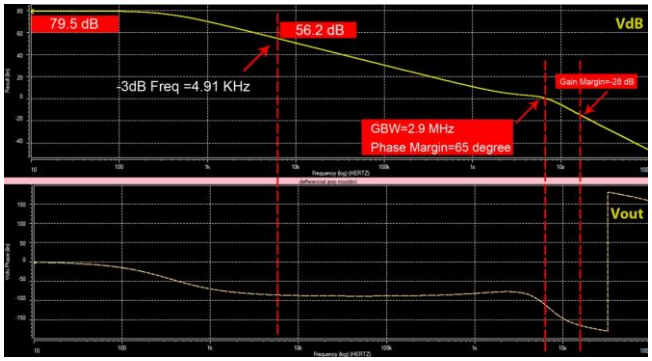


Figure 19. Op-amp frequency response in Figure 18

The phase and bode plots are delineated in Figure 19 for 2.5V and 25°C. According to this figure, the open-loop gain is ~79.5dB, and the phase margin is 65°.

4.4. Transient Results and Slew Rate

The transient results of Figure 10 will be explained in the following which has output swing voltage of 934mV and gain of 79.4dB.

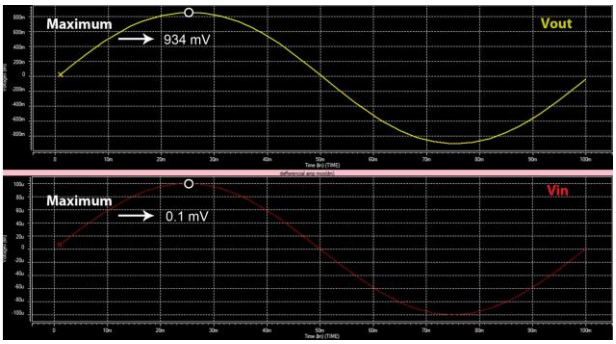


Figure 20. Transient results of Op-amp shown in Figure 10

$$\begin{cases} V_{out} = 934mV \\ V_{in} = 0.1mV \end{cases} \rightarrow Gain = \frac{934}{0.1} = 9340 \cong 79.4dB \quad (27)$$

For analyzing the slew rate, a signal was applied to the input, and the output signal was observed according to the input signal. The positive and negative slew rate was simulated based on Figure 18, and the obtained results (SR^+=3.43V/µsec, SR^-=3.03V/µsec) were demonstrated in Figure 21.

Figure 21. Calculating the slew rate in Op-amp with current buffer and miller capacitor

4.5. Comparison of Frequency Responses by Changing the Load and Compensation Capacitors Values

Table 5 indicates the various frequency responses when the values of load and compensation capacitors (C_L and C_C) are changed. The best values of both capacitors were selected after comparing the simulated parameters by HSPICE.

Table 5. Comparison of simulated parameters by changing the load and compensation capacitors

		Gain Bandwidth	Phase Margin	Unity Gain
C_L (PF)	1	3.16 MHz	80°	-28dB
	5	2.9 MHz	65°	-28dB
	10	2.56 MHz	62°	-28dB
C_C (PF)	0.25	4.17 MHz	40°	-28dB
	0.5	2.9 MHz	65°	-28dB
	1	1.65 MHz	80°	-28dB

Finally, all theoretical and simulated elements are listed in Table 6. This table proves that the proposed method optimized the final results of each parameter of the Op-amp circuit system. While in the theoretical section, some transistor parameters had approximation to calculate the corresponding equation, the ultimate results were ideally acquired. However, if this technique is utilized by a manufacturer in a real-world scenario, the simulated output will exceed the expected results. Hence, due to the limitations and failure of constructing the Op-amp system, the reasonable and acceptable results can be achieved.

Table 6. Comparison of the expected values of proposed Op-amp parameters with theoretical and simulated results

Parameter	Expected Value [27]	Theoretical Value	Simulated Value
A_V	≥80dB	82.23dB	79.5dB
GBW	5MHz	4.99MHz	2.9MHz
P_{diss}	378μW	310μW	500.07μW
Input Common-mode Range (ICMR)	±1.5V	±2.1V	2, -1.7V
Output Swing	±2.3V	2.31,-2.37V	2.41, -2.27V
Slew Rate	±5.5V/μsec	5.5V/μsec	3.43V/μsec
Phase Margin	65°	-	65°

5. Conclusion

The technique proposed in [27] for two-stage operational amplifier with a miller capacitor and a current buffer was developed in this article. All parameters, including gain, GBW, phase margin, power dissipation, ICMR, output swing, slew rate, etc. were calculated theoretically using relative equations. The main elements of all transistors in the circuit were subsequently determined and optimized based on these values. Afterward, the developed Op-amp system was simulated by HSPICE to authenticate the theoretical results. Moreover, major parameters of nine transistors and other factors were obtained through the simulation results and compared with the hypothetical output. Ultimately, comparison between the simulated/theoretical and expected achievements proves that the exceptional method in this study optimized all the elements in the Op-amp circuit design. Hence, this circuit benefits manufacturers in amplifier construction, utilizing current buffers on a practical level by reducing faults and increasing the safety and accuracy of integrators and voltage comparators.

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