An Energy-Efficient Three-Stage Amplifier Achieving a High Unity-Gain Bandwidth for Large Capacitive Loads Without Using a Compensation Zero

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***Abstract*—This letter presents a high-gain energy-efficient three-stage amplifier, which employs buffering-based pole relocation and dual-path structure. The proposed design does not rely on the introduction of compensation zero and preserves the unity-gain bandwidth (GBW) of the local feedback loop (LFL). Compared to the topologies using active-zero insertion, the 3rd pole is formed with a much smaller capacitance (parasitic capacitance), enabling it to be placed at a significantly higher frequency while consuming lower power. Moreover, the parasitic pole at the main path is bypassed by using an auxiliary path. Thus, the 3rd pole can be pushed to a higher frequency more easily than the topologies using an active zero. As a result, the GBW of the LFL in the proposed work is less limited. The proposed design improves the state-of-the-art FOM_L by 36%, LC-FOM_S by 26%, and LC-FOM_L by 218%, while preserving robustness of the performance.**

***Index Terms*—Capacitive load, energy efficiency, frequency compensation, three-stage amplifier, unity-gain frequency.**

I. Introduction

Downscaling of the CMOS process technologies has continuously enabled to reduce the power consumption of the amplifiers by lowering the supply voltage. However, the intrinsic achievable gain of the amplifiers ($g_m r_o$) is degraded due to the shorter channel length (L). Methods to obtain a high gain without increasing the channel length of transistors are, therefore, crucial to fully utilize the advanced CMOS fabrication technologies. A well-known solution to realize high-gain amplifiers is the cascode topology, vertical stacking of transistors. The cascode topology, however, demands high-supply voltages, making it unsuitable to be applied to low-supply-voltage circuits in downscaled CMOS processes. Another solution is the cascade topology, horizontal stacking of transistors. The shortcomings of the cascade topology come from the complex stability issue, which is common to multistage amplifiers. The stability issue becomes more serious when an amplifier is required to have a wide bandwidth with a low quiescent current and has to drive a large capacitive load (C_L). To tackle this issue, various frequency-compensation techniques have been demonstrated [1]–[8].

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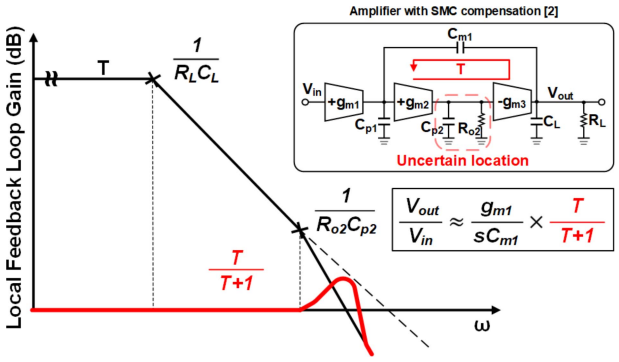


Fig. 1. Risk of instability due to the uncertain location of the pole at $1/R_{o2}C_{p2}$ in amplifiers with SMC compensation [2].

The nested Miller compensation is one of the most popular compensation methods, utilizing two Miller compensation capacitors in an inner and an outer local feedback loops (LFLs), respectively [1]. Although this method offers a robust compensation performance, high power consumption is required for the wide-bandwidth performance. As an alternative, the technique using a single Miller capacitor (SMC) was introduced to overcome this limitation by removing the inner LFL [2]. The block diagram for the amplifier using this frequency compensation method is shown in the inset of Fig. 1. This approach is likely to suffer from a risk of instability coming from the uncertain location of the pole within the Miller-compensation loop. If the pole at $1/R_{o2}C_{p2}$ is located inside the unity-gain bandwidth (GBW) of the LFL, the GBW of the LFL reduces, and peaking occurs, as shown in Fig. 1. As a result, the pole at $1/R_{o2}C_{p2}$ limits the LFL bandwidth that is achievable without the risk of instability, and it can be regarded as a band-limiting pole (BLP).

To avoid this risk, a variety of frequency compensation methods have been proposed. These methods can be classified into three groups—A, B, and C—depending on their key compensation approaches, as shown in Fig. 2. One straightforward way to solve the issue illustrated in Fig. 1 is to reduce the GBW of the LFL by inserting a damping-factor-control block (Group A in Fig. 2). As shown in Fig. 3, it can ensure stability, but at the cost of a reduction in the LFL gain by a factor of $g_{ma}R_{o2}$ compared to that of the amplifier with SMC compensation [3]. The frequency of the BLP located at $g_{ma}/C_{pb,A}$ can be increased significantly by sufficiently large g_{ma} to be located outside the GBW of the LFL. However, this approach requires a high current consumption to obtain a wide bandwidth.

Alternatively, a passive zero can be inserted for stability (Group B in Fig. 2) [4], [5]. As shown in Fig. 3, the GBW of the LFL is reduced by a factor of R_a/R_{o2} in comparison with that of the SMC compensation approach, while the BLP frequency is increased by a factor of R_a/R_{o2}. As a result, the stability of the amplifier is improved significantly. However, the passive zero implemented by a resistor and a capacitor requires a large silicon area.

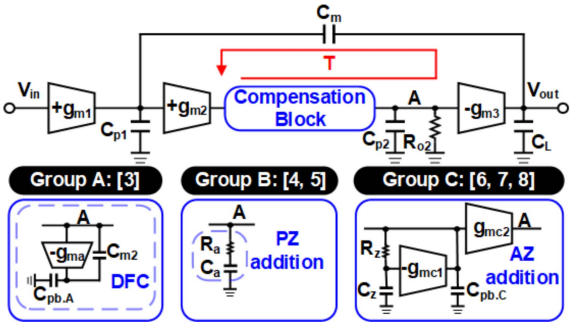


Fig. 2. Previously reported frequency compensation techniques utilizing damping factor control (Group A), passive-zero addition (Group B), and active-zero addition (Group C).

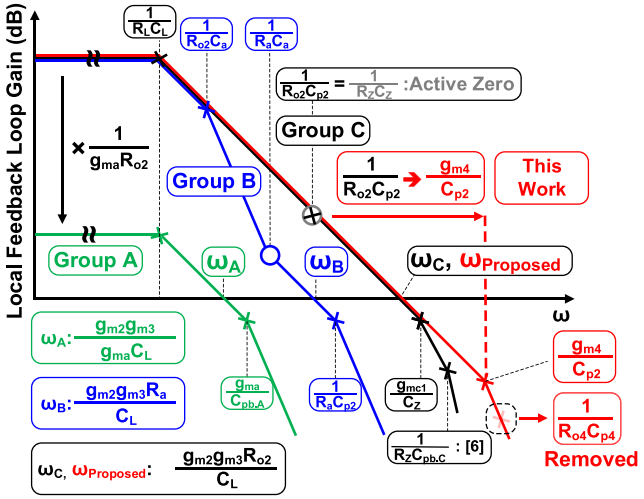


Fig. 3. Bode plots of the LFL gains for Groups A, B, and C.

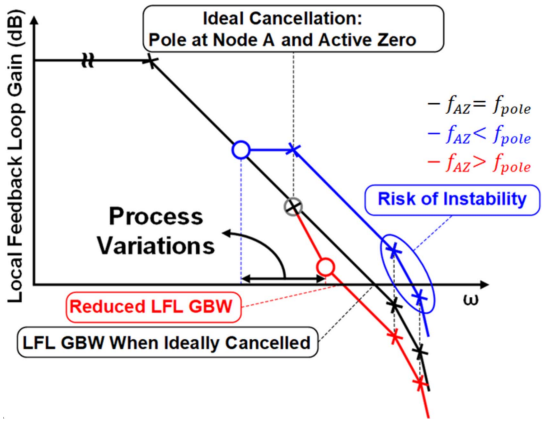


Fig. 4. LFL gain plots for the amplifier with active-zero addition (Group C) under process variations.

Instead of passive zero, an active zero can be inserted (Group C in Fig. 2) [6]–[8]. This approach aims to match the frequency of the inserted zero with the frequency of the pole at node A to negate the effect of the pole on the GBW of the LFL. If the pole at $1/R_{o2}C_{p2}$ is perfectly canceled by the zero at $1/R_ZC_Z$, the same GBW of the LFL as that of the SMC compensation approach can be obtained, as shown in Fig. 3. Note that the band-limiting 3rd pole is present at g_{mc1}/C_Z, and the value of C_Z is usually large. Therefore, g_{mc1} should be large enough to secure a sufficient separation between the 2nd and 3rd poles for good stability, incurring a large power consumption. This approach also requires passive devices, and thus suffers from a large silicon area consumption and uncertain location of the zero caused by process variations, as described in Fig. 4. If the cancellation is ideal, good stability can be achieved without reducing the GBW of the LFL (black line). However, if the frequency of the inserted active zero (f_{AZ}) is lower than the frequency of the pole at node A (f_{pole}), the BLP, and the parasitic pole at high frequencies may cause instability of LFL (blue line). When f_{AZ} happens to be higher than f_{pole}, the GBW of LFL is reduced (red line) like group B in Fig. 3. Practically, it is very difficult to achieve a perfect matching between f_{pole}, which is determined by the output resistance of a transistor amplifier and the parasitic capacitance, and f_{AZ}, which is determined by the added resistor and capacitor.

In summary, the prior works (Groups A, B, and C), which have tried to resolve the stability issues of multistage amplifiers, either reduce the GBW of the LFL or insert an additional zero that may incur various disadvantages. In this letter, we present a new amplifier design that employs buffering-based pole relocation and dual-path structure (BPR-DP) [9]. The proposed design preserves the GBW of the LFL and does not involve any compensation zero, unlike the previously proposed designs.

II. Proposed Amplifier With BPR-DP

A. Circuit Structure and Operation

Fig. 5 shows a block diagram of the proposed amplifier. The transfer function of the proposed amplifier is derived as

$$\frac{V_{\text{out}}}{V_{\text{in}}} \approx \frac{g_{m1}}{sC_m} \times \frac{\left(1-\frac{sC_m}{g_{m2}g_{m3}R_{o4}}\right)}{\left(1+\frac{sC_L}{g_{m2}g_{m3}R_{o4}}\right)\times\left(1+\frac{sC_{p2}}{g_{m4}}\right)}. \tag{1}$$

The GBW and frequencies of nondominant poles (P_2, P_3) and right-half-plane zero (Z_{RHP}) are expressed as follows, respectively:

$$GBW = \frac{g_{m1}}{C_m} \tag{2}$$

$$P_2 = -\frac{g_{m2}g_{m3}R_{o4}}{C_L} \tag{3}$$

$$P_3 = -\frac{g_{m4}}{C_{p2}} \tag{4}$$

$$Z_{RHP} = \frac{g_{m2}g_{m3}R_{o4}}{C_m}. \tag{5}$$

Since the right-half-plane zero is located at sufficiently high frequency, it has little effect on the operation of the amplifier.

Compared to the amplifier with SMC compensation, our design does not add any capacitor and resistor, which are required in the prior works [4]–[8] to insert a compensation zero. Instead, it newly includes a buffer stage (g_{m4}) and an auxiliary (AUX) path through $g_{m2.c}$. The buffer stage moves the pole of node A at $1/R_{o2}C_{p2}$ to a much higher frequency, g_{m4}/C_{p2}, as depicted in Fig. 3. Since the 2nd stage gain is preserved even at high frequencies by relocating the pole of node A, the GBW of the LFL (ω_{proposed} in Fig. 3) is maintained without reduction and becomes the same as that of Group C. Importantly, this improvement is achieved without relying on the pole-zero cancelation, unlike Group C, providing much better robustness against variations. Note that the BLP is at g_{m4}/C_{p2}, which is typically much higher than the BLP frequencies of the other topologies, allowing a wider GBW of the LFL. Compared to the BLP of Group C (g_{mc1}/C_Z), the BLP of the proposed design is created by a smaller capacitance (C_{p2}), enabling it to be placed at a higher frequency with lower power consumption. Moreover, the parasitic pole at $1/R_{o4}C_{p4}$ is bypassed by using the AUX path, and hence the BLP at g_{m4}/C_{p2} can be pushed to a high frequency more easily than the case of Group C.

The operation of the dual-path structure can be explained by examining the gain plot from node C to node A, shown in the inset of

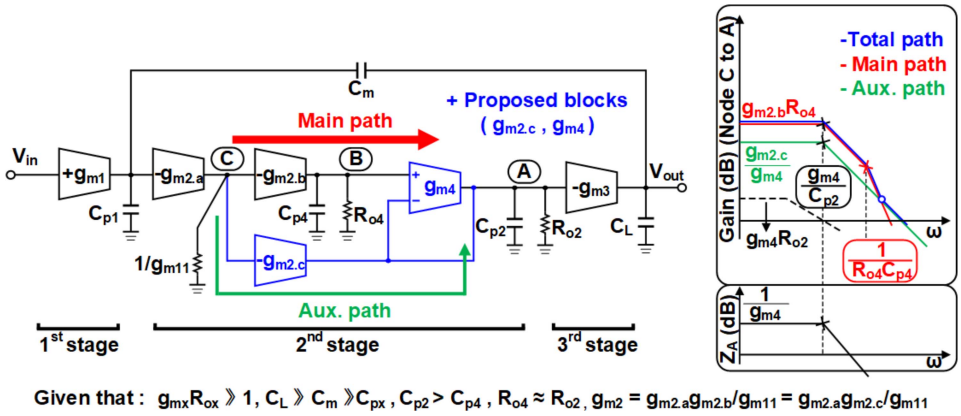
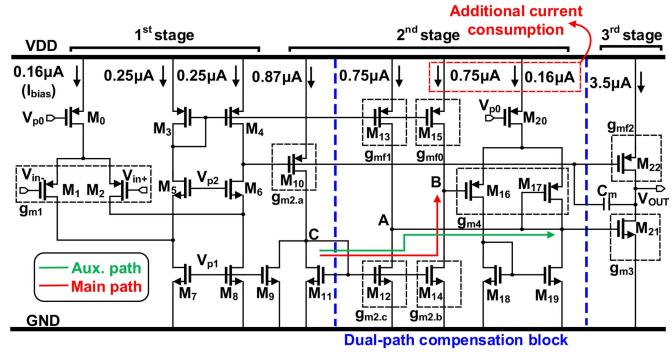


Fig. 5. Circuit diagram of the proposed amplifier. Inset: Bode plot of the gain from node C to node A.



Device	Width / Length	Device	Width / Length
M_0/M_{20}	1.6 μm / 1 μm	M_{11}	0.5 μm / 0.4 μm
M_1/M_2	8 μm / 4 μm	M_{12}/M_{14}	2 μm / 0.4 μm
M_3/M_4	0.8 μm / 1 μm	M_{13}/M_{15}	2.4 μm / 1 μm
M_5/M_6	1 μm / 0.5 μm	M_{16}/M_{17}	0.8 μm / 0.4 μm
M_7/M_8	0.8 μm / 1 μm	M_{18}/M_{19}	1 μm / 0.5 μm
M_9	1.6 μm / 1 μm	M_{21}	24 μm / 0.2 μm
M_{10}	16 μm / 0.2 μm	M_{22}	64 μm / 0.2 μm

* C_m = 400 fF (Total Compensation Capacitance)

Fig. 6. Circuit schematic and device sizes of the proposed amplifier.

Fig. 5. The transfer function from node C to node A is derived as

$$\frac{V_A}{V_C} \approx \frac{1}{\left(1+\frac{sC_{p2}}{g_{m4}}\right)} \times \left(\frac{g_{m2.b}R_{o4}}{1+sR_{o4}C_{p4}} + \frac{g_{m2.c}}{g_{m4}}\right). \quad (6)$$

The open-loop gain of the buffer, g_{m4}, becomes 0 dB at g_{m4}/C_{p2}, where the buffer stops functioning as a buffer, and the gains of the main and AUX paths start to fall. As the frequency increases further beyond g_{m4}/C_{p2}, the parasitic pole of node B at $1/R_{o4}C_{p4}$ appears in the main path, starting to drop the gain with −40-dB/dec slope. However, the AUX path, bypassing node B, is unaffected by the pole at node B and sustains the gain drop with −20-dB/dec slope. As a result, the combined operation of the main and AUX paths eliminates the effect of the parasitic pole of node B. Moreover, the gain mismatch between the main path ($g_{m2.b}$) and AUX path ($g_{m2.c}$) does not affect the phase margin because the pole and zero caused by this mismatch appear at significantly high frequencies around which the parasitic pole ($1/R_{o4}C_{p4}$) resides.

B. Circuit Implementation

Fig. 6 shows a transistor-level schematic of the proposed amplifier. The 1st stage is implemented as a folded-cascode amplifier using M_{0-8}. A current source, M_9, enhances the gain of the 2nd stage by increasing the transconductance of M_{10}. The 2nd stage includes the main path ($M_{10,11,14}$), AUX path ($M_{10,11,12}$), and the unity-gain buffer (M_{16-20}). The AUX path and the unity-gain buffer consume 0.75 μA and 0.16 μA only, respectively. M_{13} and M_{15} construct feedforward paths to improve the slew performance of the 2nd stage. The 3rd stage consists of M_{21-22}. The feedforward path through M_{22} enhances the slew performance of the 3rd stage.

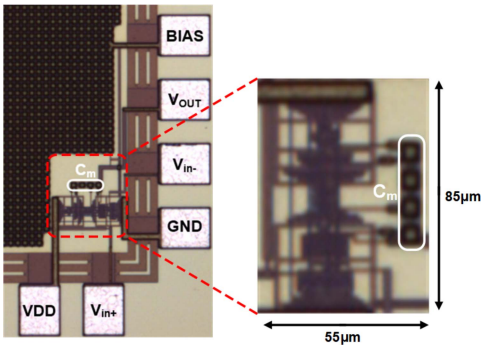


Fig. 7. Chip micrograph.

Device sizes of all the transistors and the Miller capacitor are shown on the bottom side of Fig. 6. Considerations in setting the MOSFET sizes are as follows.

1) The sizes of $M_{1,2}$ are set to reduce the noise and ensure the input pair matching.
2) The sizes of $M_{10,11,14}$ are determined for the pole generated at node C to exist at a sufficiently high frequency.
3) The sizes of $M_{16,17}$ are set to minimize the parasitic capacitors in nodes A and B.
4) The channel length of the transistors, which are used to set bias currents, such as $M_{0,20}$, $M_{3,4,13,15}$, and $M_{7,8,9}$, is larger than that of other transistors for matching.

III. Experimental Results

The chip was fabricated in 0.18-μm CMOS process, occupying an area of 0.0046 mm^2, as shown in Fig. 7. Fig. 8(a) shows the measured gain and phase responses of the amplifier over frequency when C_L is 1.3 nF. The GBW and phase margin are 680 kHz and 60.34°, respectively, while the extrapolated dc gain is higher than 120 dB. The variations of the phase margin and gain margin over C_L are shown in Fig. 8(b). When C_L becomes larger, the phase margin decreases. The proposed amplifier was validated to be stable with a phase margin greater than 50° for C_L up to 1.9 nF. The gain margin slightly improves as C_L increases. It is because the 3rd pole location and GBW do not depend on C_L, while the 2nd pole frequency changes with C_L. The GBW and phase margin variations over I_{bias} (the bias current shown in Fig. 6) for C_L of 1.3 nF are summarized in Fig. 8(c). As expected, the GBW linearly increases with I_{bias}.

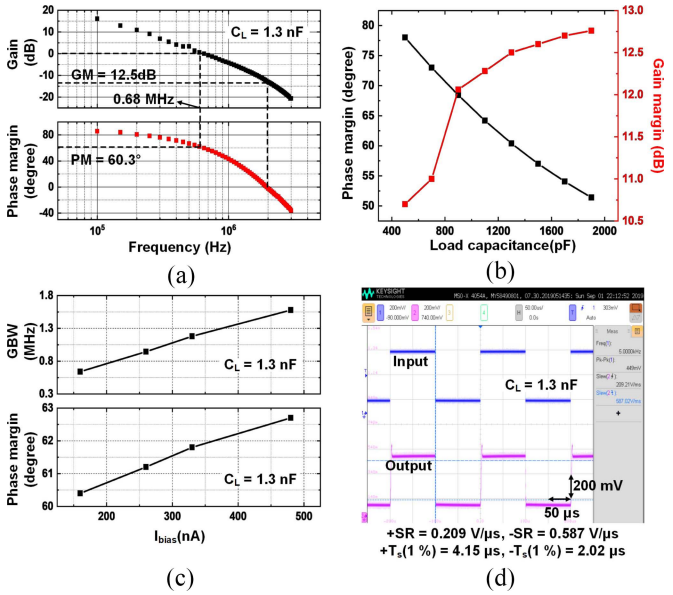


Fig. 8. Measurement results. (a) AC response. (b) Phase margin and gain margin versus C_L. (c) GBW and phase margin versus I_{bias}. (d) Step response showing the SR and settling time (T_S) for rising and falling transitions.

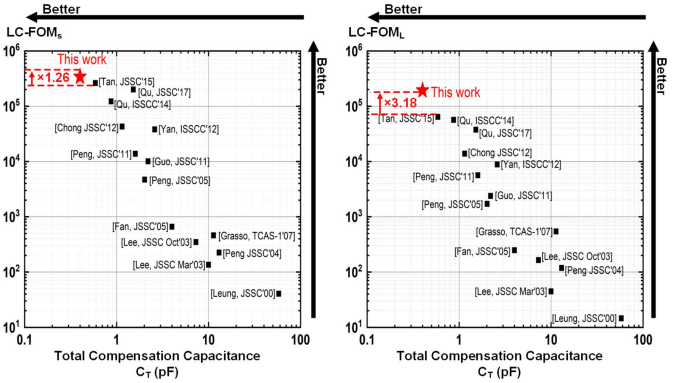


Fig. 9. Benchmark of the state-of-the-art three-stage amplifiers.

A distinctive advantage of this work is that the phase margin stays nearly constant over a wide range of I_{bias}, as shown in the graph on the bottom side of Fig. 8(c). That is because the 2nd and 3rd poles are pushed to higher frequencies along with the dominant pole as I_{bias} increases, demonstrating the robustness. Therefore, I_{bias} can be tuned for different values of C_L as required in various applications to provide the desired GBW and slew rate (SR) performances. The step response measured in the unity-gain-feedback configuration is shown in Fig. 8(d). The proposed amplifier achieves the average SR and 1%-settling time of 0.398 V/μs and 3.085 μs, respectively. Although a minor overshoot is observed during the rising transition, it is not caused by a low-phase margin but by the difference between the push (M_{22}) and pull (M_{21}) paths, as shown in Fig. 6. While M_{22} reacts at the same time as M_{10} because M_{10} and M_{22} share the same gate voltage, M_{21} reacts slower than M_{10} as its gate terminal is connected to node A. Note that there is no ringing after the overshoot, indicating that a sufficient phase margin is guaranteed. The amplifier consumes 6.7 μW from a 1-V supply.

Table I summarizes the performance of the proposed amplifier and compares it with other state-of-the-art works. The area consumption of our work is among the smallest ones because it does not use any passive components for implementing compensation zero. The dc gain of the proposed amplifier is higher than that of other designs. Since the Miller capacitor used for frequency compensation in our work is significantly smaller than that used in other designs, the proposed amplifier achieves a wide bandwidth and a high SR with consuming lower power and obtaining a better phase margin. Consequently, the proposed design outperforms in various figures of merits (FOMs), which are defined in [3]–[8]. The proposed amplifier improves the state-of-the-art FOM$_L$ by 36%, LC-FOM$_S$ by 26%, and LC-FOM$_L$ by 218%.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORKS

	[4] Peng JSSC'11	[5] Tan JSSC'15		[6] Qu ISSCC'14	[7] Yan ISSCC '12	[8] Qu JSSC'17	This Work
Technology(µm)	0.35	0.13		0.18	0.35	0.18	0.18
Chip Area (mm^2)	0.02	0.0032		0.007	0.016	0.013	0.0046
DC Gain(dB)	110	>100		>100	>100	>100	>120
Supply Voltage (V)	1.5	1.2		0.9	2	1.2	1
Power(µW)	30	12.7		6.3	144	69.6	6.7
C_T (pF)	1.6	0.587		0.87	2.6	1.52	0.4
C_L(pF)	150	330	560	500	15,000	18,000	1,300
Phase Margin(deg)	57	58	53	52.7	52.3	59.6	60.3
GBW (MHz)	4.4	4.21	3.49	1.34	0.95	1.18	0.68
Average SR(V/µs)	1.8	1.35	0.86	0.62	0.22	0.22	0.398
FOM$_S$[MHz·pF/mW]	22,000	109,222	153,648	106,349	98,656	305,172	131,940
FOM$_L$[V/µs·pF/mW]	9,000	34,894	35,550	49,206	22,917	56,897	77,223
LC-FOM$_S$[MHz/mW]	13,750	186,068	261,751	122,240	37,945	200,771	329,850
LC-FOM$_L$[V/µs/mW]	5,625	59,444	60,562	56,559	8,814	37,432	193,060

* C_T = Total compensation Capacitance , C_L = Load Capacitance

Typical FOM$_S$ and FOM$_L$ [3-8] :
$$\text{FOM}_S = \frac{\text{GBW}\cdot C_L}{\text{Power}} \quad \text{FOM}_L = \frac{\text{SR}\cdot C_L}{\text{Power}}$$

Large-Capacitive-Load FOM$_S$ and FOM$_L$ [6-8] :
$$\text{LC-FOM}_S = \frac{\text{GBW}\cdot C_L}{\text{Power}\cdot C_T} \quad \text{LC-FOM}_L = \frac{\text{SR}\cdot C_L}{\text{Power}\cdot C_T}$$

IV. CONCLUSION

Our proposed three-stage amplifier that employs BPR-DP does not rely on the introduction of compensation zero and preserves the GBW of the compensation loop. It improves FOM$_L$ by 1.36 times, LC-FOM$_S$ by 1.26 times, and LC-FOM$_L$ by 3.18 times, as well as the robustness of performance, in comparison with the state-of-the-art three-stage amplifier designs (Fig. 9).

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