Performance Improvement of Nanoscale Field Effect Diode (FED) with Modified Charge Channel: 2D Simulation and an Analytical Surface Potential Model

Arash Rezaei[1] · Ali A Orouji[1]

Abstract

The off-state currents of Side contacted Field Effect Diode (S-FED) and Double-Gate Field Effect Diode (DG-FED) structures increase for the lengths of the channel shorter than 35 nm. This is owing to the minority carrier's injection from the source and drain into the channel and the band to band tunneling phenomenon caused by the high impurities of the drain, source, and reservoirs. In this paper, a structure with a 25 nm channel length with low doping and without reservoirs has been presented. The charge channel of the proposed structure modified using Multi Gate and Extended source/drain electrode. We have called the structure as modified charge channel FED (MCC-FED). The main idea in the proposed device is to modify the charge channel for improving the electrical performance. This device achieved lower gate delay time and energy-delay production and a higher on-current and on/off current ratio compared to conventional FEDs. In addition, two-dimensional analytical models for the surface potential and the electric field at the channel surface are presented by solving the two-dimensional Poisson equation in three distinct zones in the channel with appropriate boundary conditions. To verify the validity of the proposed model, the modeling results are compared with the simulation results and appropriate matching between results demonstrates appropriate accuracy of the proposed model.

Keywords Field effect diode (FED) · Side contacted FED (S-FED) · Gate delay · Ion/Ioff ratio · Surface potential

1 Introduction

Metal–oxide–semiconductor field-effect transistors (MOSFETs) have been scaled down in the last four decades [1, 2], which opens the way for improvements in the switching speed, density, functionality, and cost of integrated chips. On the other hand, the decreased channel length is caused to increase in the leakage current and short channel effects [3–8]. Recently, new structures have been proposed to overcome the effects of the short channel in MOSFETs. One of these devices is a field-effect diode. In nanometer scales, field-effect diodes act very quickly in switching and have a high Ion/Ioff ratio and also low EDP compared to MOSFETs. The energy-delay product (EDP) is one of the important parameters in logic applications and an important factor for designing the

devices with high energy efficiency and high performance. A small amount of EDP indicates less energy consumption at the similar level of performance. Therefore, this device can be an excellent alternative in digital applications.

Field-effect diode (FED) is a structure with two gates on the channel region, called GS and GD, and the two source and drain regions with different doping [9]. The I_{on}/I_{off} current ratio is a characteristic of logic transistors. The Ion/Ioff is the figure of merit for having high performance (more Ion) and low leakage power (less Ioff) for the transistors. On the other hand, field-effect diodes have a higher Ion and lower Ioff compared to those of the MOSFETs. Hence, compared to a MOSFET with similar geometrical, this device has a higher Ion/Ioff ratio [10, 11]. Field-effect diodes have interesting applications including electrostatic discharge (ESD) [12, 13], switch, memory cells [14–17], and also can be used to design integrated circuits [18–20]. One of the advantages of field-effect diodes is their small off-state current, but for the channel length less than 100 nm, the off-state current will be increased due to the minority carrier's injection from the source and drain into the channel [21, 22].

✉ Ali A Orouji
  aliaorouji@semnan.ac.ir

1 Department of Electrical and Computer Engineering, Semnan University, Semnan, CO 3513119111, Iran

To overcome this problem, the Modified-FED and Side contacted-FED structures have been presented [22–27]. The off-state currents of the S-FED and DG-FED [28] structures increase for the channels shorter than 35 nm. This is owing to the band-to-band tunneling phenomenon caused by the high impurity of the drain and source. This effect can be relieved by decreasing the impurities, but this in turn decreases the on-state current. Hence, in this paper, a structure with low doping and without reservoirs has been presented which a well-modified charge channel (MCC-FED) using Multi Gate and Extended source/drain electrode. Our results show that the proposed structure improves the on-state current, I_{on}/I_{off} ratio, gate delay, and EDP parameters. All simulations are done by a 2-D device simulator, ATLAS, from Silvaco at the temperature of 300 K [29]. A two-dimensional analytical model for field-effect diode channel potential is also presented. In this model, using appropriate boundary conditions and solving the equations in the x and y directions, surface potential and electric field at the channel surface are obtained. On the other hand, the effect of physical parameters of a transistor such as the gate oxide thickness and the gate work-function are investigated and appropriate matching between the results of the proposed model and simulating the device with Silvaco, show the correctness of the proposed model.

2 Device Structure

The schematic cross-sections of the Modified-FED and Side contacted-FED structures are shown in Fig. 1. In a forward-biased FED, the voltage polarities of the drain and its adjacent gate are opposite. Hence, the pinch-off phenomenon does not occur in field-effect diodes, so that, unlike short channel FETs, the device will be safe from the hot electron effects [9, 30].

In these structures (Fig. 1), the regions with opposite doping as reservoirs have been added to the typical source and drain FEDs. These reservoirs in the off-state current mode, with the injection of majority carriers into the channel causes the reduction in minority carrier injected from the source and the drain regions into the channel, which improves the off-state current.

The schematic cross-section of the proposed nano-scale FED is shown in Fig. 2. As it is seen in Fig. 2, this structure has multi gates and an extended source/drain electrode, which helps to modified the charge channel and improve the gate control over the channel compared with a conventional FED. All the device parameters which are used in the simulation are listed in Table 1.

In field-effect diodes, gate junctions are biased so that the channel between the source and the drain regions, which is an intrinsic or a low-doping region, is replaced by an n-p/p-n. Since this diode is created by the field of the gates, it is called a field-effect diode. The on and off modes of the device are presented in Table 2.
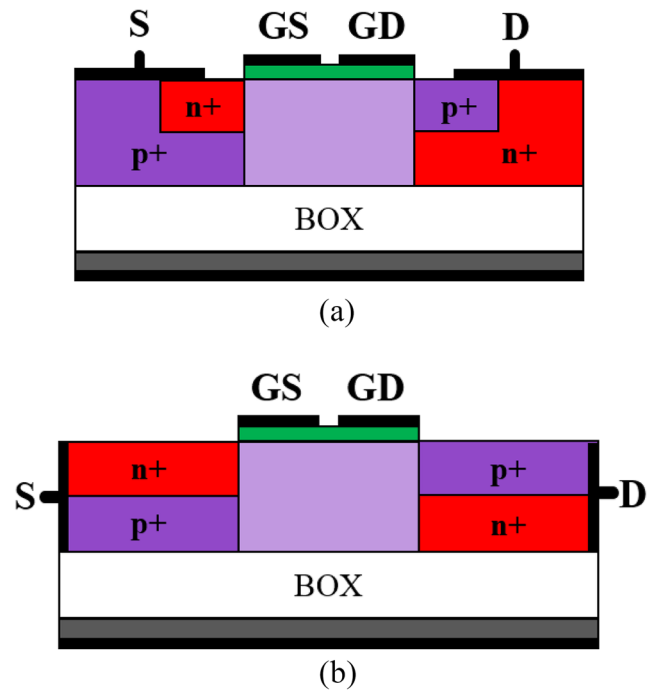

(a)

(b)

Fig. 1 The cross-section views of (a) M-FED and (b) S-FED

In the off mode, the injection of additional minority carriers occurs across forward bias coupling (n + −p on the source side) and (n-p + on the drain side), which leads to increased concentration of electrons and holes in the region p (below the GS) and the n region (below GD), respectively. This increased concentration of electrons and holes prevents the formation of the p-n reverse bias in the channel. Hence, to achieve an appropriate off mode current, the redundant electrons and holes below GS and GD should be reduced. In field-effect diodes, as source and drain regions' impurities decrease, the injection of additional minority carriers in the channel decreases, and off-state and on-state currents will be reduced as well.

But in the structures with low doping, due to control of the channel through multi gates, the charge channel is modified. Therefore, n and p areas are well created for on- and off-states, also without need to reservoirs, volume of the source and drain get larger which results in a larger on-state current.

The models used in this simulation are: Band-to-Band Tunneling (BTBT) model for accurate consideration of band-to-band tunneling effects, Shockley-Read-Hall (SRH) and Auger generation/recombination, field-dependent mobility, concentration-dependent mobility in the high doping concentration, and Band-gap-narrowing (BGN) model.

3 Result and Discussion

Figure 3 shows the electron density profile for the presented structure and the S-FED in the off-state. As shown in this

Table 1 ATLAS simulation parameters for typical device of the MCC- FED

Parameter name	Parameter description	Value in nano-scale MCC-FED
L_{ch}	Channel length	25 nm
t_{ox}	Gate oxide thickness (t_{ox})	1 nm
$L_{S/D}$	Source/Drain length	30 nm
$N_{S/D}$	Source/Drain doping concentration	10^{19} cm^{-3}
L_G	Gate length	10 nm
L_{sp}	Spacer Gates	5 nm
T_{ch}	Channel thickness	10 nm
W_f	Gate work function	4.17 eV
N_{ch}	Channel doping concentration	10^{14} cm^{-3}
$L_{GS/GD}$	Source and Drain/Gate space	2 nm
K_{OX}	SiO$_2$ Dielectric constant	3.9

figure, due to control of the channel through upper and lower gates, the charge channel is modified and also n and p areas are well created in depth of the channel in spite of the S-FED structure. Hence, the reservoirs are not necessary, so we can have larger source and drain areas than the S-FED structure, to achieve a larger current.

Figure 4(a) shows the energy band diagram for the proposed and S-FED structures at the depth of the channel in the off state. As expected, in this figure, the charge channel is improved by the multi-gate technique, and also the p-n junction is well-formed in the channel. Figure 4(b) and (c) shows the carrier concentrations of the structures.

In Fig. 5a, the drain current for the proposed device is depicted at 25 nm channel length (LG + LG + LSP), in both the on and off-states. As it is shown in the figure, using extended source/drain electrode, low doping, and multi-gate, the

injection of carriers is reduced. Hence the off-state current of the device is decreased, dramatically.

In Fig. 5b, the current-voltage curves are compared for the proposed and conventional structures, at the on-state regime. It is obviously seen that the driving ability of the proposed transistor is increased significantly. The main physical reason for improving the electrical performances of the proposed structure is the ability of the gate to control the channel and the well p-n junction formed in the channel.

Figure 6 shows the effect of a dielectric constant on the current of the MCC-FED structure in the on and off states. As shown in Fig. 6, when the dielectric constant increases, the off current increases due to tunneling in the channel area. Therefore, the I_{on}/I_{off} ratio decreases with increasing dielectric constant, so the proposed structure by the oxide dielectric has a better performance.

Intrinsic time delay of the gate, which characterizes the switching response of the transistor is an important metric for logic applications This delay is given by expression (1) using the time needed to charge the constant gate capacitor, Cg to the V_{dd} at a constant I_{on} [18].

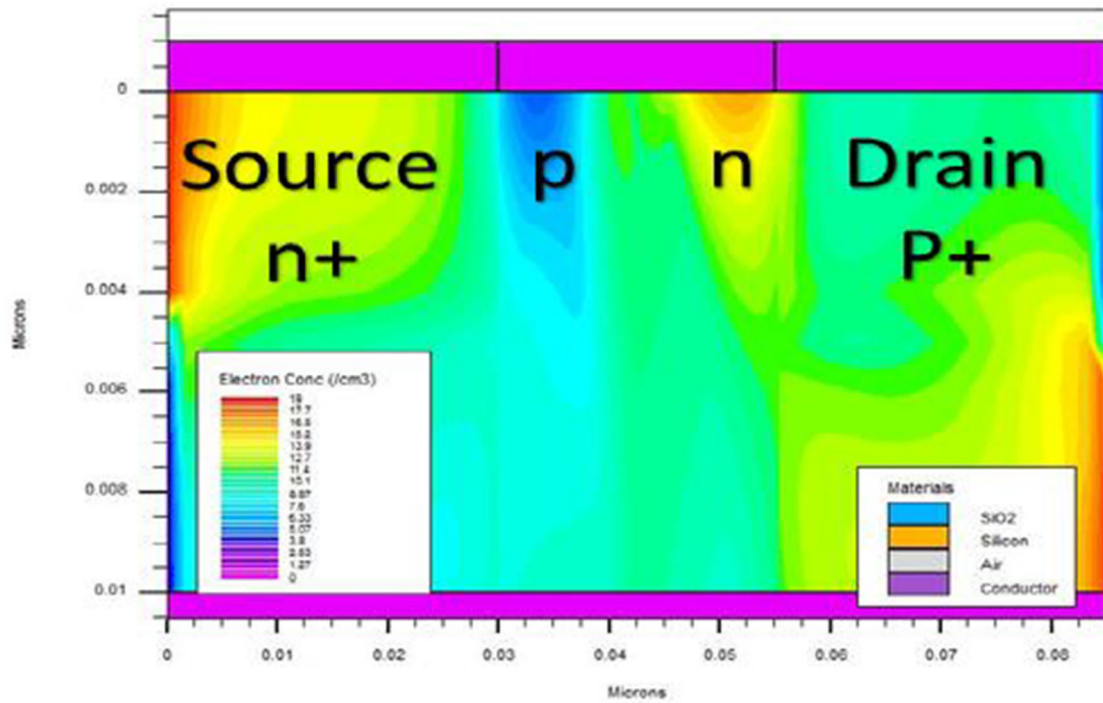$$\tau = \frac{C_g \cdot V_{dd}}{I_{on}} \tag{1}$$

The energy-delay product (EDP) is one more significant parameter in logic applications which is given using
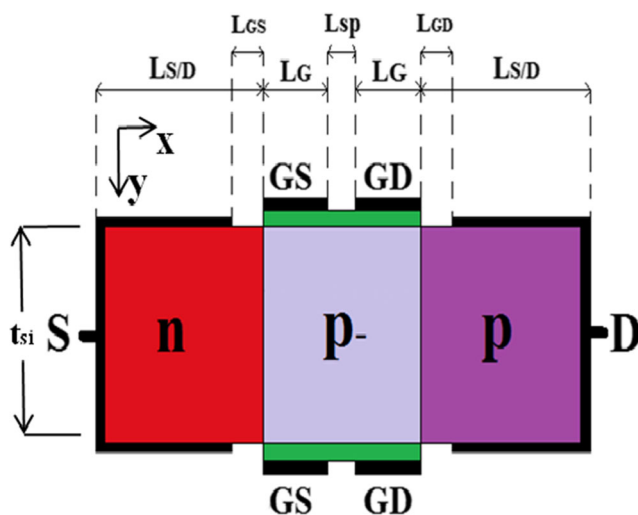
Fig. 2 Cross sectional view of the proposed FED structure

Table 2 OFF and ON states of FED

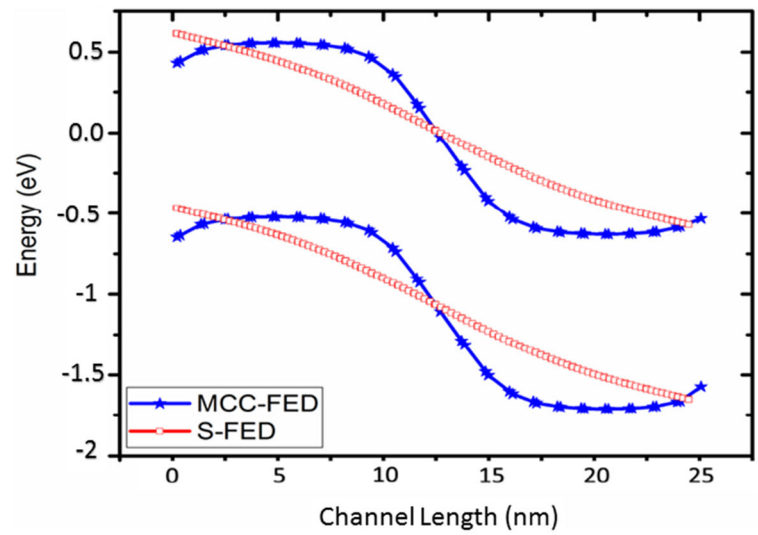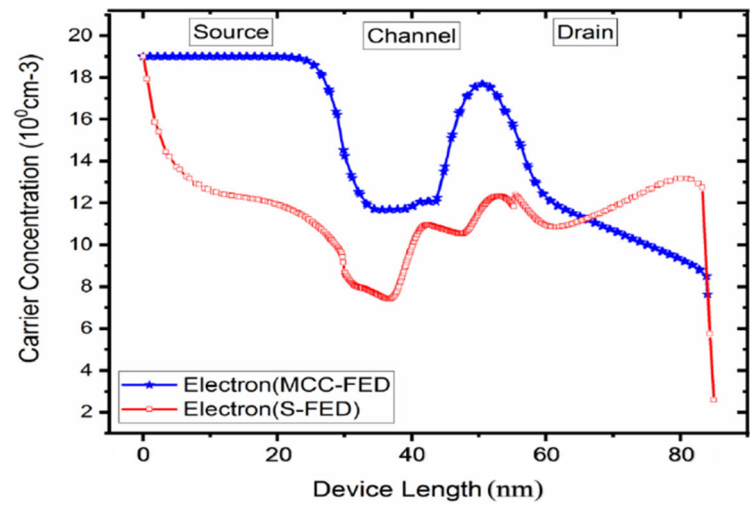| V_{DS}	V_{GS}	V_{GD}	FED configuration from S to D	state
+	+	−	n$^+$npp$^+$	on
+	−	+	n$^+$pnp$^+$	off
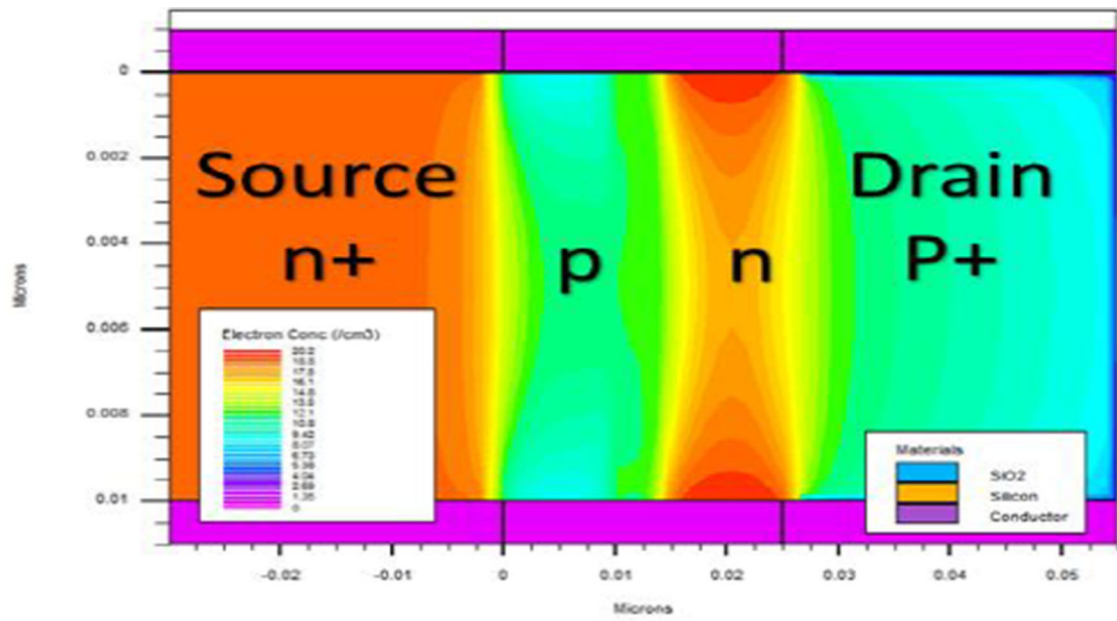
(a)

(b)

Fig. 3 A cross-sectional view of the electron density in OFF-state at (a) MCC-FED (b) S-FED structures
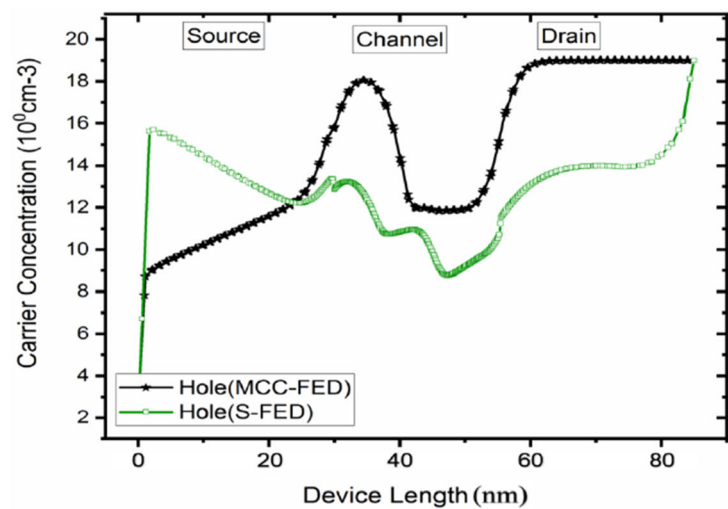
Fig. 4 (a) Energy band diagram, (b) Electron concentration and (c) Hole concentration of the MCC-FED and S-FED in the off state
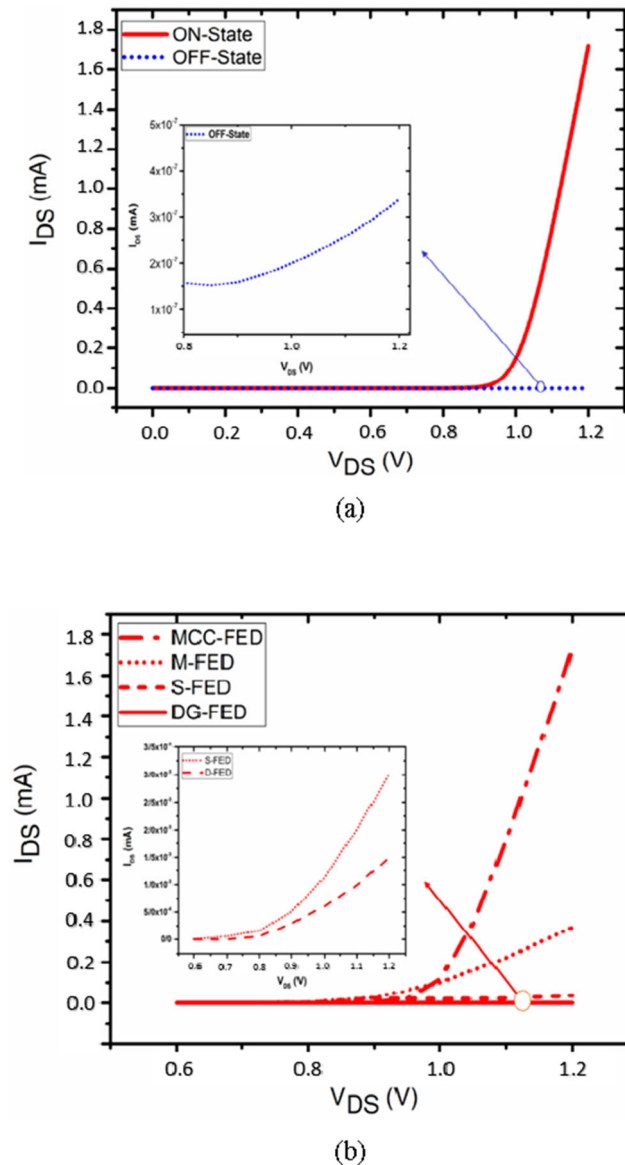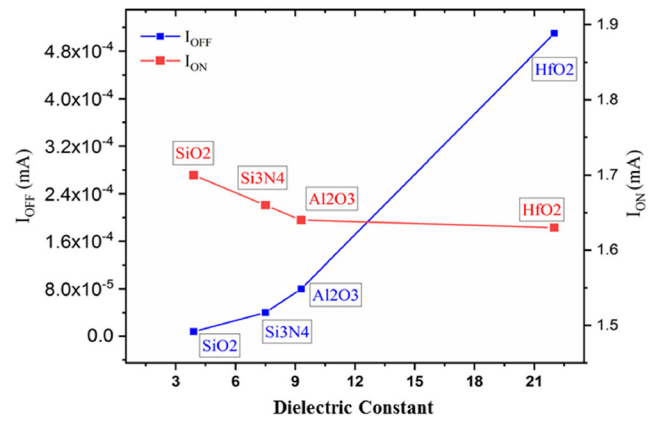

(a)

(b)

(c)

expression (2) [18]. The lower EDP means the lower energy consumption of the device.

$$EDP = \left(\frac{C_g \cdot V_{dd}}{I_{on}}\right)\left(C_g \cdot V_{dd}^2\right) \quad (2)$$

By longer L_{GS}, the control of the source and drain over these regions is increased so the output characteristic improves. As shown in Fig. 7, reduction in $L_{GS/GD}$ improves I_{on}, I_{on}/I_{off} ratio, Gate delay, and EDP. From the fabrication

Fig. 6 I_{ON} and I_{OFF} for different values of dielectric constant for the MCC-FED

point of view and optimum device performance, $L_{GD} = L_{GS}$ is chosen as 2 nm.

As shown in Fig. 8, the gate delay time of the MCC-FED, DG-FED and S-FED is compared with respect to channel length at $V_{dd} = 1.2$ V. The intrinsic capacity (C_g) is calculated according to numerical simulation results at 1GHz. The proposed structure demonstrates an excellent improvement in comparison to DG-FED and S-FED, regarding Fig. 8. Since the on current of MCC-FED is higher than conventional FED, then we expect a lower time delay for this proposed structure. According to analyzed data, the speed of the MCC-FED devices is higher than the conventional FED.

In Fig. 9, the energy-delay product (EDP) has been plotted in terms of channel length for the DG-FED, S-FED and the MCC- FED. As expected, due to the high on-state current and the low off-state current in the proposed structure, this structure has a lower EDP than the conventional FED.

As it is observed in Fig. 10, the ratio of I_{on}/I_{off} in this structure is larger than the conventional FED. Thus, it is expected to have lower power consumption and higher speed. According to the figure, decreasing the channel length will cause an increment in the off-state current due to the injection of additional minority carriers in the channel, therefore the I_{on}/I_{off} ratio will be reduced.

In Table 3, the on- and off-state currents, I_{on}/I_{off} ratio, EDP, gm, subthreshold slope and gate delay are compared for the MCC-FED, G-FED [31], DG-SFED and conventional FED. As shown in Table 3, the I_{on}/I_{off}, EDP, SS, gm and gate delay for the proposed structure have been excellently improved in comparison with the conventional FED.

(a)

(b)

Fig. 5 (a) I–V characteristic of the MCC-FED in the on ($V_{GS} = 1.2$ V and $V_{GD} = -1.2$ V) and off ($V_{GS} = -1.2$ V and $V_{GD} = 1.2$ V) states, (b) Comparison of the I–V characteristic of the MCC-FED, M-FED, DG-FED and S-FED in the on-state
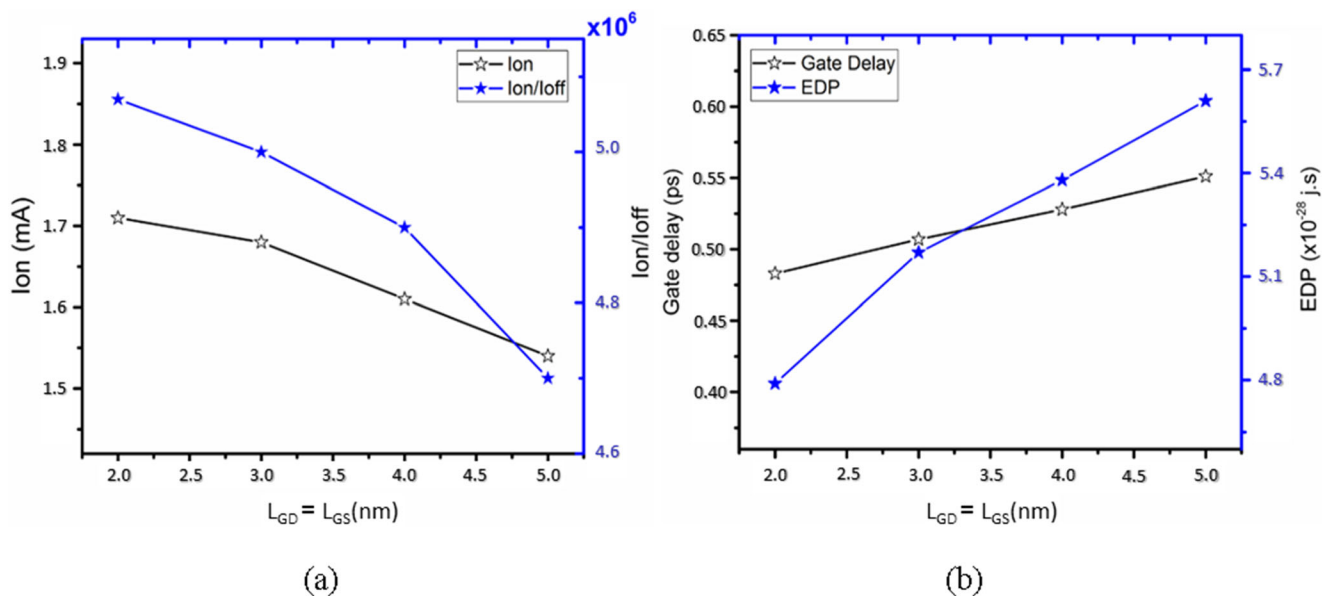
Fig. 7 Optimization of the $L_{GS/GD}$ for the proposed structure in terms of (a) ON-state current and I_{ON}/I_{OFF} ratio (b) Gate delay and EDP

4 Model Derivation

4.1 Surface Potential and Electric Field

In the proposed structure the channel is divided into three zones: 1- Area below GS, 2- Area below GD, and 3- Distance between gates. Assuming a uniform distribution of impurity density in the channel and neglecting mobile carriers, the two-dimensional Poisson equations in the channel, before the strong inversion, can be expressed as follows [32]:

$$\frac{\partial^2 \varphi(x, y)}{\partial x^2} + \frac{\partial^2 \varphi(x, y)}{\partial y^2} = \frac{q.NA}{\varepsilon_{Si}}$$
$$0 \leq x \leq L, \ 0 \leq y \leq t_{si}$$

(3)

Where Na is the doping concentration, ε_{si} is silicon dielectric coefficient, t_{si} is silicon thickness, q electric charge, and φ electrostatic potential in the channel.
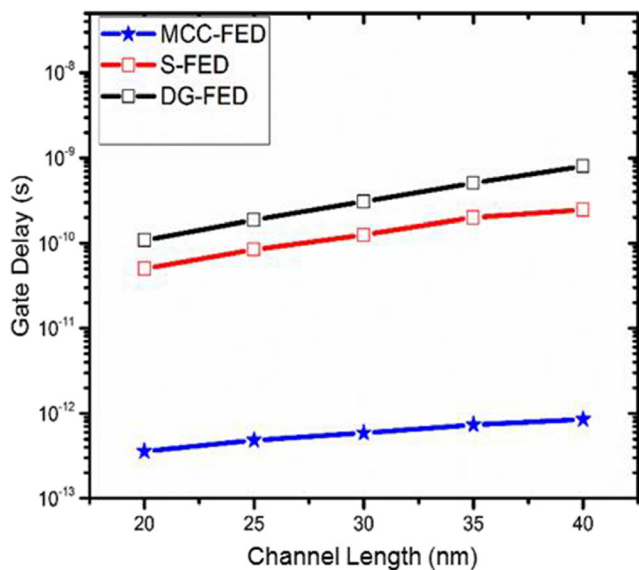

Fig. 8 The variation of gate delay (logarithmic graph) versus channel length for the MCC-FED, DG-FED, and S-FED
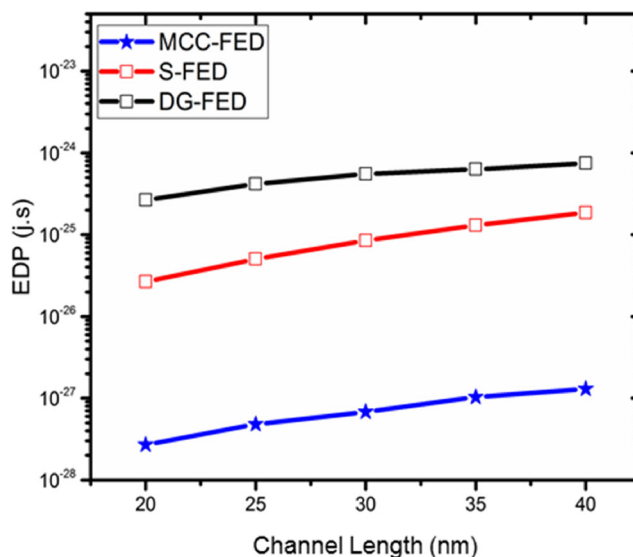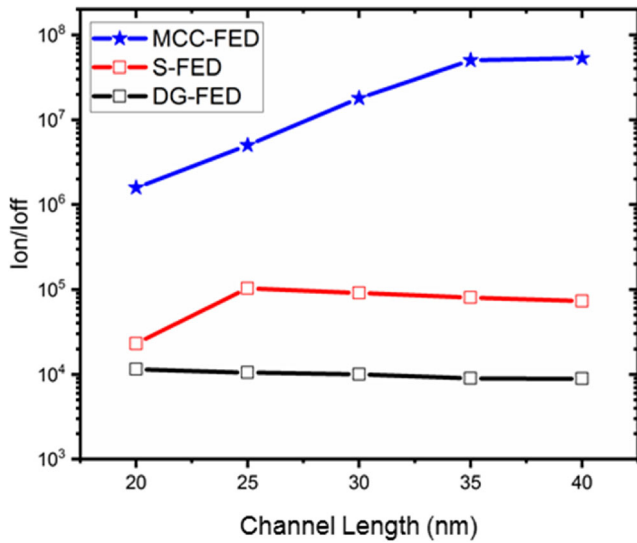

Fig. 9 The variation of EDP (Logarithmic graph) versus the channel length for MCC-FED, DG-FED, and S-FED

Fig. 10 I_{on}/I_{off} ratio (logarithmic graph) as a function of channel length for the MCC-FED, DG-FED, and S-FED

Electrostatic potential using a parabolic approximation for the area below GS and area below GD in channel regions is described as follows [33]:

$$\varphi_I(x, y) = (\varphi_{SI})(x) + Z_{1I}(x).y + Z_{2I}(x).y^2$$
$$\varphi_{III}(x, y) = (\varphi_{SIII})(x) + Z_{1III}(x).y + Z_{2III}(x).y^2 \quad (4)$$

Where φ_{SI} and φ_{SII} are surface potentials below the gates. The values of Z_{i1} and Z_{iIII} coefficients are obtained by using boundary conditions in silicon bonding with oxide (Si/SiO$_2$).

The potential distribution in the zone 3 due to the short length of this region can be assumed as a linear function of x:

$$\varphi_{II}(x) = b.x + c \quad , \quad L_G \leq x \leq L \quad (5)$$

where the values of the coefficients b1 and c1 are determined using horizontal boundary conditions.

In order to continuity sspotential and electric flux in the channel, vertical boundary conditions is expressed as follows

[34]:

$$\left.\frac{\partial \varphi_i(x,y)}{\partial y}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}.\frac{\varphi_{Si}(x)-(v_{GS}-v_{FB})}{t_{ox}}$$
$$\left.\frac{\partial \varphi_i(x,y)}{\partial y}\right|_{y=t_{Si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}.\frac{(v_{GS}-v_{FB})-\varphi_{bi}(x)}{t_b} \quad (6)$$

Where t_b/t_{ox} is the front / back side gate oxide thickness, ε_{ox} oxide permeability coefficient, and φ_b back surface potential. On the other hand, due to symmetry, $\varphi_{bi} = \varphi_{Si}$ and $t_b = t_{ox}$. Also V_{GS} and V_{GD} are the applied voltage to gates and V_{FB} is the flat band voltage as shown below [34].

$$V_{FB} = \phi_{GS}-\chi-\frac{E_g}{2}-V_T\ln\left(\frac{N_A}{n_i}\right) \quad (7)$$

Whereas ϕ_{GS}, χ, E_g, V_T, and n_i are working function of gate, electron affinity, bandgap, thermal voltage and the intrinsic carrier concentration.

By applying boundary conditions (6) to eqs. (4), the coefficients Z_{1I}, Z_{2I}, Z_{1III}, Z_{2III} are obtained as a function of the surface potential of φ_S. Then by replacing eq. (4) in eq. (3) and solving it at $y = 0$ we will have:

$$\frac{\partial^2 \varphi_{SI}(x)}{\partial x^2} = \frac{\varphi_{SI}(x)}{\lambda^2} - \frac{[(v_{GS}-v_{FB})-\beta.q.NA]}{\lambda^2}$$
$$\frac{\partial^2 \varphi_{SIII}(x)}{\partial x^2} = \frac{\varphi_{SIII}(x)}{\lambda^2} - \frac{[(v_{GD}-v_{FB})-\beta.q.NA]}{\lambda^2} \quad (8)$$

where

$$\beta = \frac{t_{ox}.t_{Si}}{2.\varepsilon_{ox}} \quad , \quad \lambda^2 = \frac{\varepsilon_{si}.t_{ox}.t_{Si}}{2.\varepsilon_{ox}}$$

By solving eqs. (8), the surface potential of the channel is acquired as follows:

$$\varphi_{SI}(x) = Ae^{-\frac{x}{\lambda}} + Be^{\frac{x}{\lambda}} + [(v_{GS}-v_{FB})-\beta.q.NA]$$
$$\varphi_{SIII}(x) = Ce^{-\frac{x-(L_G+L_{sp})}{\lambda}} + De^{\frac{x-(L_G+L_{sp})}{\lambda}} + [(v_{GD}-v_{FB})-\beta.q.NA] \quad (9)$$

Table 3 Comparison of results of the conventional FED and MCC-FED structures) $V_{drain} = 1.2$ V

| Device	Channel length	I_{ON}	I_{OFF}	I_{ON}/I_{OFF}	Gate delay (psec)	EDP (j.sec)	SS(mV/dec)	$g_m(s)$
S-FED	25 nm	3.2×10^{-3} mA	3.1×10^{-8} mA	1.03×10^5	114	5.023×10^{-26}	95	7.7×10^{-7}
DG-FED	25 nm	1.47×10^{-3} mA	1.6×10^{-7} mA	9.1×10^3	187	4.17×10^{-25}	84	1.3×10^{-7}
R-FED	25 nm	1.3 mA	0.14 mA	9.2	not turn off	not turn off	not turn off	not turn off
G-FED	25 nm	14 mA	0.9 mA	1.17	not turn off	not turn off	not turn off	not turn off
MCC-FED	25 nm	1.71 mA	3.37×10^{-7} mA	5.07×10^6	0.483	4.79×10^{-28}	76	4.2×10^{-5}
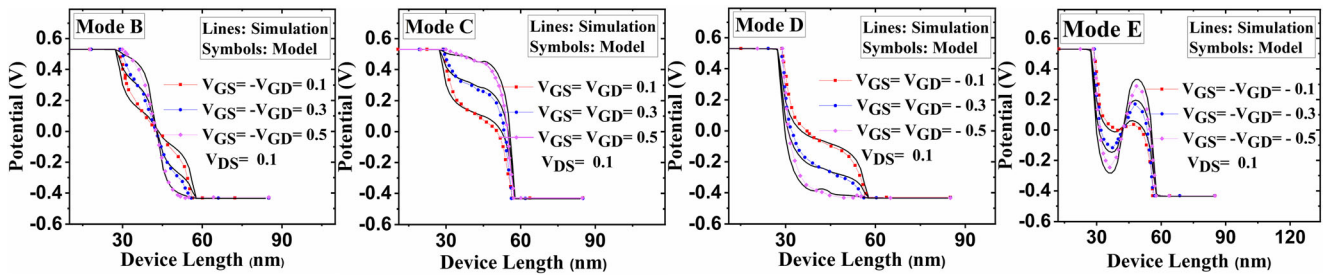
Fig. 11 Surface Potential Profiles at different gate voltages

Where A, B, C, and D are constant coefficients that is obtained by applying horizontal boundary conditions (10) to eqs. (9).

$$\varphi_I(0,0) = \varphi_{SI}(0) = \frac{Eg}{2}$$
$$\varphi_{SI}(L_{GS}) = \varphi_{SII}(L_{GS})$$
$$\frac{\partial \varphi_{SI}(x)}{\partial x}\bigg|_{x=L_G} = \frac{\partial \varphi_{SII}(x)}{\partial x}\bigg|_{x=L_G}$$
$$\varphi_{SII}(L_G + L_{SP}) = \varphi_{SIII}(L_G + L_{SP}) \quad (10)$$
$$\frac{\partial \varphi_{SII}(x)}{\partial x}\bigg|_{x=L_G+L_{SP}} = \frac{\partial \varphi_{SIII}(x)}{\partial x}\bigg|_{x=L_G+L_{SP}}$$
$$\varphi_{SIII}(L_{ch}) = v_{DS} - \frac{Eg}{2}$$

Finally, the surface potential of the channel can be calculated from Eq. (9).

The lateral electric field of E_X is calculated by an analytic derivative of the potential as follows.

Fig. 12 Surface potential profiles at different drain to source voltages

$$E_s(x) = -\frac{d\varphi_s}{dx} \rightarrow E_{sII}(x) = -b \quad , \quad L_G \leq x \leq L_G + L_{sp}$$
$$E_{sI}(x) = \frac{A}{\lambda} . e^{\frac{-x}{\lambda}} - \frac{B}{\lambda} . e^{\frac{x}{\lambda}} \quad , \quad 0 \leq x \leq L_G$$
$$E_{sIII}(x) = \frac{C}{\lambda} . e^{-\frac{x-(L_G+L_{sp})}{\lambda}} - \frac{D}{\lambda} . e^{\frac{x-(L_G+L_{sp})}{\lambda}} \quad , \quad L_G + L_{sp} \leq x \leq L$$

5 Model Validation

To investigate the proposed analytical model, the field effect diode with parameters of Table 1 is considered. Also, to confirm the proposed model, the field effect diode is simulated with ATLAS software.

The surface potential changes relative to the gate voltage is shown in Fig. 11. According to Table 2, different modes are created for positive or negative gate voltages. By applying a voltage to the gates, the potential level under the gates increases or decreases. According Fig. 11, a np connection in the channel and a total n⁺npp⁺ connection in the mode B, and similarly a n⁺nnp⁺ connection in the mode C, a n⁺ppp⁺ connection in the mode D and a n⁺pnp⁺ connection in the mode E are created throughout the device by applying a positive voltage to the gate-source and a negative voltage to the gate-drain. As shown in Fig. 11, the modeling results are in good agreement with the simulation results.

Figure 12 shows the surface potential of the field effect diode for different V_{DS}. As you can see, the analytical model is in good agreement with the simulation results.

Figure 13 shows the electric field changes relative to the drain-source voltage at the channel surface. When V_{DS} increases, the field at the boundary of the drain and channel junction is reduced, causing carrier injections. The results of the model are in good agreement with the simulation.

In Fig. 14, for different oxide thicknesses, there is a good match between the model results and the simulation results. By decreasing the oxide thickness, the gate control on the channel increases.
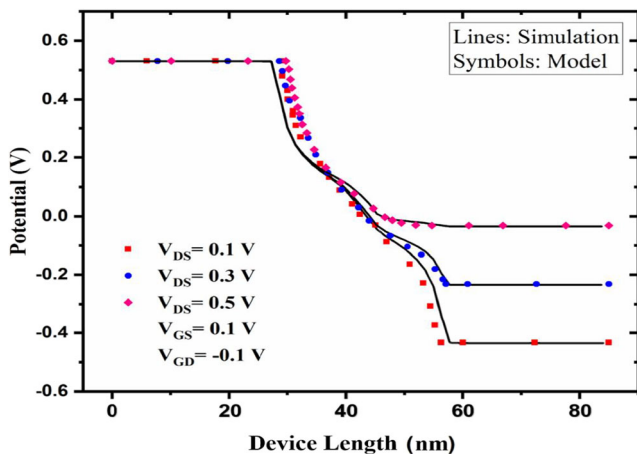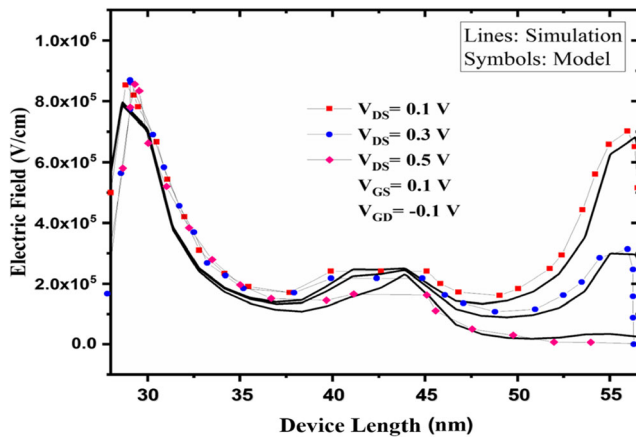
Fig. 13 Comparison of the lateral electric field profiles along the channel

Fig. 15 Surface potential profiles at different metal gate work functions

Figure 15 shows the potential distribution for the various working function of the gates on the device level. By decreasing the working function of the gates, the potential at the channel surface increases due to the flat band voltage change. Also, this image shows the modeling results and simulation results are similar.

6 Conclusion

In this paper, a new structure for field effect diodes at the 25 nm channel length is introduced. This device achieved more control on the charge channel by low doping and the multi-gate technique and extended source/drain electrode. The designed FED improved on-state current and I_{on}/I_{off} by 1000
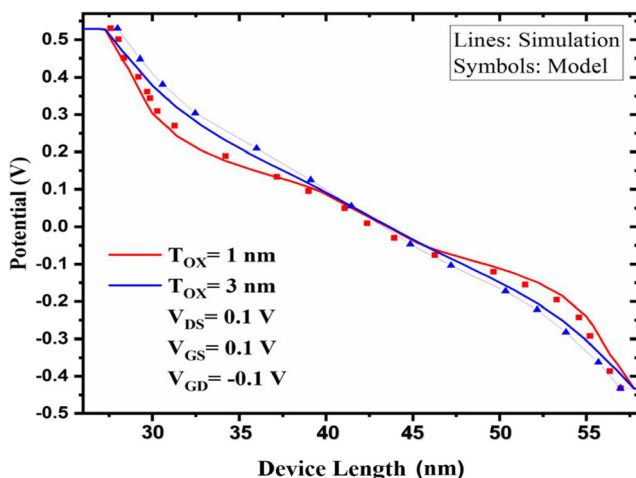
and 50 times, respectively. Moreover, the gate delay is decreased to 0.483 ps and energy-delay product from 5.023×10^{-26} to 4.79×10^{-28}. It can be concluded that the proposed structure is a promising candidate for high frequency applications. In addition, a two-dimensional analytical model with parabolic approximation for the field-effect diode channel potential is presented and Based on the electrostatic potential of the channel, an electric field is obtained at the channel surface. Channel surface potential analysis for various field effect diode parameters such as gate oxide thickness and gate work function have been done and also, the proposed model predicts their effects well.

Declarations

Fig. 14 Surface potential profiles at different oxide thicknesses

References

1. Moore GE (1975) Progress in digital integrated electronics, in Proc. Int. Electron Devices Meeting., pp. 11–13
2. Mehrad M, Zareiee M (2016) Improved device performance in nano scale transistor: an extended drain SOI MOSFET', ECS Journal of Solid State Science and Technology., 5, (7), M74
3. Yu B, Wang L, Yuan Y, Asbeck PM, Taur Y (2008) Scaling of Nano wire transistors. IEEE Trans Electron Dev 55(11):2846–2858
4. Joshi G and Choudhary A (2011) Analysis of short channel effects in nanoscale MOSFETs, International Journal of Nanoscience., 10, (01n02), pp.275–278
5. Zareiee M (2016) Modifying buried layers in nano-MOSFET for achieving reliable electrical characteristics. ECS J Solid State Sci Technol 5(10):M113
6. Kranti A, Chung TM, Raskin JP (2005) 'Gate length scaling and microwave performance of double gate nanotransistors. Intl J Nanosci 4(05n06):1021–1024
7. Zareiee M, Mehrad M (2017) A reliable nano device with appropriate performance in high temperatures. ECS J Solid State Sci Technol 6(4):M50
8. Zareiee M (2017) High performance nano device with reduced short channel effects in high temperature applications. ECS J Solid State Sci Technol 6(7):M75
9. Raissi F (1996) A brief analysis of the field effect diode and breakdown transistor'. IEEE Trans Electron Dev 43(2):362–365
10. Sheikhian I, Raissi F (2003) High-speed Digital family using Field Effect Diode. Electron Lett 39(4):345–347
11. Sheikhian I, Raissi F (2005) An Improved Differential Comparator with Field Effect Diode Output Stage. J Circ Syst Comput 14(5):931–937
12. Cao S, Salman AA, Chun JH et al (2010) 'Design and characterization of ESD protection devices for high-speed I/O in advanced SOI technology. IEEE Trans Electron Dev 57(3):644–653
13. Cao S, Chen TW, Beebe SG et al (2009) 'ESD Design challenges and strategies in deeply-scaled integrated circuits', Proc. Conf. Custom integrated circuits conference (CICC), San Jose, CA, USA, pp.681–688
14. Amirmazlaghani M, Raissi F (2009) Memory cell using modified field effect diode. IEICE Electronics Express 6(22):1582–1586
15. Yang Y, Gangopadhyay A, Li Q et al (2009) 'Scaling of the SOI field effect diode (FED) for memory application', Proc. Int. Conf. InSemiconductor Device Research Symposium, ISDRS'09, pp. 1–2
16. Badwan, A. Z., Chbili, Z., Yang, Y., et al. 'SOI field-effect diode dram cell: Design and operation', IEEE Electron Dev Lett, 2013, 34, (8), pp.1002–1004
17. Badwan, A. Z., Chbili, Z., Li, Q., et al. 'SOI FED-SRAM cell: Structure and operation', IEEE Trans Electron Dev, 2015, 62, (9), pp. 2865–2870
18. Jazayeri F, Forouzandeh B, Raissi F (2009) Low-power variable gain amplifier with UGBW based on nanoscale Field Effect Diode. IEICE Electron Express 6(1):51–57
19. Jazaeri F, Soleimani-Amiri S, Ebrahimi B et al. (2008) 'Pseudo-Linear automatic gain control system based on nanoscale field effect diode and SOI-MOSFET', Proc. Int. Conf. Design and Test workshop, pp. 154–158
20. Koyanagi M, Nakamura T, Yamada Y, Kikuchi H, Fukushima T, Tanaka T, Kurino H (2006) Three-dimensional integration technology based on wafer bonding with vertical buried interconnections. IEEE Trans Electron Dev 53(11):2799–2808
21. Rezaei A, Azizollah-Ganji B, Gholipour M (2018) 'Effects of the Channel Length on the Nanoscale Field Effect Diode Performance', Journal of Optoelectronical Nanostructures., 3. (2)
22. Sheikhian I, Raissi F (2007) Simulation results for nanoscale field effect diode. IEEE Trans Electron Dev 54(3):613–617
23. Manavizadeh, N., Raissi, F., Soleimani, E.A., et al. 'Performance assessment of nanoscale field-effect Diodes', IEEE Trans Electron Dev, 2011, 58, (8), pp. 2378–2384
24. Manavizadeh N, Raissi F, Soleimani EA et al (2012) Geometrical study of nanoscale field effect diodes. Semiconductor Sci Technol 27(4):045011
25. Touchaee BJ, Manavizadeh N (2015) An inverter gate design based on nanoscale S-FED as a function of reservoir thickness. IEEE Trans Electron Dev 62(10):3147–3152
26. Touchaei BJ, Manavizadeh N (2017) Design and Simulation of Low-Power Logic Gates Based on Nanoscale Side-Contacted FED. IEEE Trans Electron Dev 64(1):306–311
27. Rezaei A, Azizollah-Ganji B, Gholipour M (2018) Nanoscale field effect diode (FED) with improved speed and I ON/I OFF ratio. IET Circ Dev Syst 13(3):309–313
28. Hashemi SA, Pourmolla P, Jit S (2019) Double-Gate Field-Effect Diode: A Novel Device for Improving Digital-and-Analog Performance. IEEE Trans Electron Dev 67(1):18–25
29. International Device Simulation Software, SILVACO TCAD, 2015
30. Sanchez JJ, Hsueh KK, De Massa TA (1989) Drain-engineered hot-electron- resistant device structure: A review. IEEE Trans Electron Dev 36(6):1125–1132
31. Sotoudeh A, Amirmazlaghani M (2018) Graphene-based Field Effect Diode. Superlattices and Microstructures 120:828–836
32. Wang P, Zhuang Y, Li C, Li Y, Jiang Z (2014) Subthreshold behavior models for nanoscale junctionless double-gate MOSFETs with dual material gate stack. Japanese J Appl Phys 53(8):084201–084207
33. Ramezani Z, Orouji AA (2018) 'Dual metal gate tunneling field effect transistors based on MOSFETs: A 2-D analytical approach. Superlattices and Microstructures 113:41–56
34. Ramezani Z, Orouji AA (2018) Analysis and modeling of unipolar junction transistor with excellent performance: a novel DG MOSFET with N^+-P^- junction. J Comput Electron 17(2):670–681