A 20 MHz–2 GHz Inductorless Two-Fold Noise-Canceling Low-Noise Amplifier in 28-nm CMOS

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***Abstract*— In this paper, a wideband low-noise amplifier (LNA) with a two-fold noise cancellation scheme is proposed. Finetuned for advanced CMOS, the proposed LNA architecture uses a common-gate input branch to provide wideband input matching. It is followed by two stages of the common-source structure which cancels the noise and distortion of the first and second stages and relaxes the design restriction on the first noise-cancellation stage. The provided circuit-level analysis is verified by simulations. The proposed LNA is fabricated in 28-nm CMOS. It achieves a minimum noise figure (NF) of 2.5 dB and input return loss (S_{11}) < −15 dB over 0.02–2 GHz bandwidth while consuming only 4.1 mW from a 1 V supply and driving an external 50-Ω load. The −3 dB power gain (S_{21}) is 18.5 dB and IIP3 is +4.25 dBm.**

***Index Terms*— 4G/5G receivers, current reuse, cognitive radios, low-noise amplifier (LNA), noise reduction, noise cancellation, software-defined radios.**

I. Introduction

TO BE able to amplify the received RF signal at any of the supported cellular frequency bands, a wideband (WB) noise-canceling (NC) low-noise amplifier (LNA) has become a subject of intensive research in both industry and academia [1]–[4]. Replacing multiple LNAs with a single LNA not only saves the silicon area, but also the printed circuit board (PCB) footprint of volume-constrained applications, and lowers the total bill of materials (BOM). It further eliminates the antenna switch that would be otherwise necessary to route the received signal to the appropriate LNA, thus worsening the noise figure of the overall receiver.

To provide wideband input matching, a common-gate (CG) topology of the LNA input stage is one of the appealing candidates [5]. The noise factor (NF) and input impedance of the CG structure depend inversely on its transconductance, g_m, which means that the CG structure will suffer from poor noise performance if it is designed to provide the wideband input matching. Moreover, high linearity is required for multi-mode RF front-ends to reduce cross-modulation/inter-modulation because of the increased need for co-existence of adjacent blockers or on-chip leakage from its own transmitter [6]. A popular method to enhance the noise performance of a CG amplifier is a noise cancellation (NC) technique which removes the channel thermal noise of the main antenna-interfacing transistor [1], [7] [8].

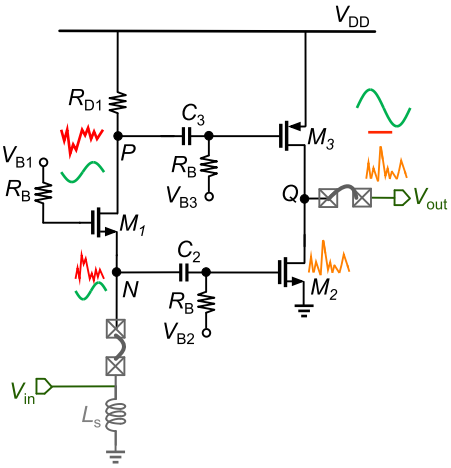

Fig. 1. Conventional wideband noise-canceling LNA.

Recently, a new approach of combining noise cancellation and noise reduction techniques was introduced in [4]. The noise reduction technique there is based on a current-reuse approach, which was applied to the CG noise-cancellation stage to reduce the channel thermal noise of the following common-source (CS) cancellation stage. Moreover, it was designed as a low-noise transconductance amplifier (LNTA) with an intention of providing high impedance for driving a passive mixer in an integrated receiver, while also being able to drive an external 50 Ω load. The noise reduction stage improves the noise performance of the CG noise-canceling structure. However, stacking up three transistors limits the available voltage swing in its output stage, thus leading to some degradation in the linearity performance.

Figure 1 shows a conventional WB-NC LNA [9], [10]. Common-gate transistor M_1 is used as an input stage so as to provide the wideband input matching to 50 Ω. The channel

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M_0	(1um/180nm)×20	R_{D0}	560Ω
M_1	(1um/30nm) × 8	R_{D1}	780Ω
M_2	(1um/180nm)× 30	R_F	20kΩ
M_3	(1um/50nm)×12	R_B	50kΩ
M_4	(1um/50nm)×8	$C_{0\text{-}5}$	1pF
M_5	(1um/50nm)×16	—	—

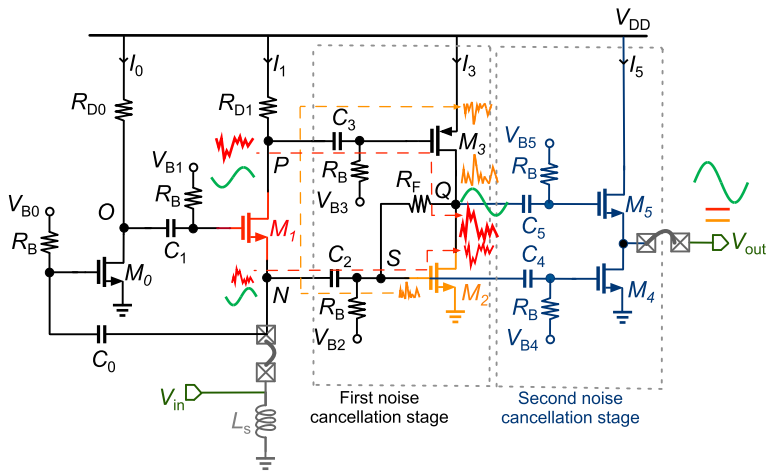


Fig. 2. Proposed two-fold noise cancellation LNA.

thermal noise of M_1 creates two out-of-phase voltage noise perturbations at nodes P and N, with the latter being smaller in amplitude. By amplifying the voltage noise N through M_2 and adding it to the voltage noise P amplified through M_3, the noise originated by the input transistor M_1 can be canceled at the output. Although this structure can effectively cancel the channel thermal noise of M_1 by means of the second stage (M_2 and M_3), the noise of the second stage is unaffected and can negatively impact the overall noise performance. This is reinforced by the fact that the input matching stage does not provide enough gain, so M_2 can now be the dominant noise source. As will be later shown in Section II-C, to meet this noise-cancellation condition, the size of M_2 should be chosen large enough, but this will add more design restrictions, such as burning more power as well as increasing the amount of parasitic capacitance at the output node.

In this paper, we propose a two-fold noise canceling LNA architecture which not only cancels the noise of the input matching transistor, as done conventionally, but it also cancels the noise of the noise-canceling transistor itself. Furthermore, the proposed complementary pMOS/nMOS structure can also cancel the transistors' distortions.

The paper is organized as follows. The proposed wideband LNA is explained in Section II, further providing an analysis of input matching, gain, noise, and linearity. In Section III, the measurement and simulation results are presented. The conclusions are drawn in Section IV.

II. Proposed Architecture

The proposed LNA architecture is shown in Fig. 2. The three stages realize the two-fold noise cancellation (NC) to further lower the noise figure (NF) while extending the bandwidth. M_1 is used as the CG structure for providing the broadband input matching. As in the prior art, the second stage is a NC complementary common-source (CS) topology consisting of M_2 and M_3, which is a pMOS/nMOS pair used to improve linearity. After applying the conventional noise-cancellation technique, the most important noise source is now due to the CS transistors in the second stage. To deal with this new challenge, the third stage, consisting of M_4 and M_5, is utilized to cancel the channel thermal noise of M_2 and M_3.

External input shunt inductor L_s (4310LC series SMD component) is used at the source of M_1 to provide a dc current path and to cancel the deleterious effect of the parasitic capacitances of transistors M_0, M_1, M_2 and M_4. Since node Q is of high impedance, its voltage can vary substantially. Consequently, the negative feedback resistor, R_F, is used to prevent the variation of dc voltage at node Q. Since the Miller multiplication of R_F makes it much larger than the input and output impedances, its effect is ignored in all analysis.

A. Input Matching

As shown in Fig. 2, the CG transistor M_1 of the first stage realizes the wideband input matching. Its input impedance of $1/(g_{m1}+g_{mb1})$ is, to the first order, independent of frequency. To simplify the ensuing notations, we lump the body effect into the main transconductance g_m. Henceforth, G_{m1} stands for $(1 + g_{m0}R_{D0})(g_{m1} + g_{mb1})$. The input impedance is calculated as:

$$Z_{in} = \frac{R_{Ls}+sL_s}{C_N L_s s^2+(R_{Ls}C_N+L_s\frac{(1+r_{ds1}G_{m1})}{(r_{ds1}+Z_p)})s+R_{Ls}\frac{(1+r_{ds1}G_{m1})}{(r_{ds1}+Z_p)}+1} \quad (1)$$

where R_{Ls} is the series resistance of L_s. C_N denotes the total parasitic capacitance seen by the input node which is damped by L_s. The input matching condition, $S_{11} < -10$ dB, will be achieved if $|Z_{in}|$ is around 50 Ω. As indicated by (1), at mid frequencies, the input impedance is $\sim 1/G_{m1}$. At very low frequencies, the input matching can be effectively influenced by external L_s, so its value should be chosen high enough to ensure good matching there.

The off-chip inductor L_s is connected to the antenna pin, thus not consuming any extra pads on the chip. It is used for dc biasing but *not* used for matching; hence its value has to be merely high enough (e.g. 1.3 μH) as not to affect the input impedance (i.e. a lower value of the inductor could only affect the lower frequency limit of the bandwidth, f_L). In this case, equation (1) can be simplified to:

$$Z_{in} \approx \frac{1}{C_N s + G_{m1}} \quad (2)$$

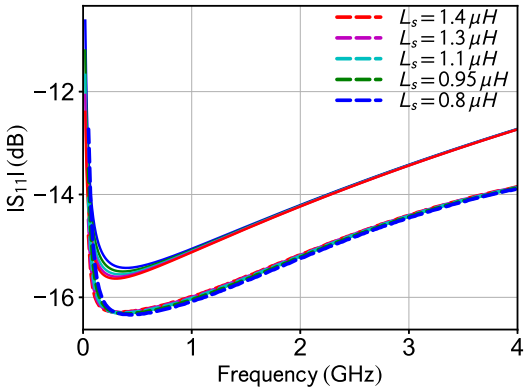


Fig. 3. Effect of external L_s on the input matching: (dotted curves) full circuit SPICE simulations, (solid curves) plots of equation (1).

According to (2), the input matching is mainly defined by M_0 and M_1. Therefore, if L_s changes, for instance from 0.8 μH to 1.4 μH, there will be no tangible change on S_{11}. This has been confirmed in full-circuit SPICE simulations shown in Figure 3, which plots the input matching characteristic S_{11} for various values of L_S. For reference, plots based on (1) are also included. A zoomed-in version concentrating on the lower frequencies is re-plotted in Fig. 4 (top). Based on this data, Fig. 4 (bottom) visualizes at what frequency (y-axis) the magnitude of S_{11} worsens by 0.5 dB for a given value of L_s (x-axis).

B. Gain Analysis

Three stages are used in the proposed structure, so a significant gain is expected. The second stage is the most effective in providing the gain and so it consumes the most current. Since the first stage should ensure the input matching condition, it draws less current. Therefore, its voltage gain cannot be very high. In addition, the third stage acts as an output buffer and so its gain cannot be substantially increased.

The equivalent small-signal impedance seen from the drain of M_1 toward the ground is termed Z_P and is equal to

$$Z_P = R_{D1}||\left[r_{ds1} + \frac{1}{sC_N}||sL_s(1+G_{m1}r_{ds1})\right]||\frac{1}{sC_P} \quad (3)$$

where C_P is the total parasitic capacitance to ground at node P. Z_Q is equal to $r_{ds2}||r_{ds3}||1/sC_Q$ where C_Q is the total parasitic capacitance at node Q. Z_{out} is defined as the output impedance, which is calculated as $r_{ds4}||r_{ds5}||1/g_{m5}||1/sC_{out}$, where C_{out} is the output parasitic capacitance. By considering the input matching condition, $1/G_{m1} = R_s$, the voltage gain of the proposed LNA is calculated as:

$$|A_v| \cong \frac{1}{2}[(G_{m1}g_{m3}|Z_P| + g_{m2})Z_Q g_{m5} + g_{m4}]|Z_{out}| \quad (4)$$

The voltage gain of the proposed LNA, A'_v, without considering the third stage, is equal to: $A'_v = \beta Z_Q$, in which β is equal to $(1/2)[g_{m2} + G_{m1}g_{m3}|Z_P|]$. As stated by the transfer function of Z_Q, the dominant pole causes Z_Q to have a large variation (Z_Q's roll-off happens at low frequencies), so its bandwidth reduces. When considering the third stage, the total voltage gain is equal to: $A_v = (g_{m5}\beta Z_Q + g_{m4}/2)|Z_{out}|$.

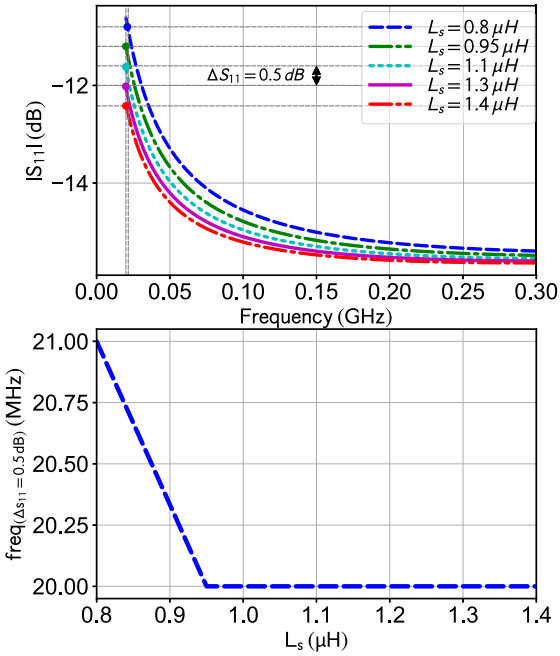


Fig. 4. (top) Zoomed-in S_{11} of Fig. 3 showing the sensitivity of low-side frequency f_L at which S_{11} changes by 0.5 dB for different values of L_s with respect to $S_{11,(L_s=1.4\,\mu\text{H})} = -12.45$ dB at 20 MHz; (bottom) the sensitivity of the lower frequency of the input matching to L_s for $\Delta S_{11} = 0.5$ dB.

The M_4's transconductance is added to $g_{m5}A'_v$ which creates a zero after the pole to neutralize its effect. Parasitic capacitance of the last stage defines the dominant pole as well as the roll-off frequency. Hence, by applying the proposed double noise-cancellation technique, although the gain of the proposed LNA increases, the bandwidth of the circuit slightly decreases due to more parasitic capacitances.

To validate the theoretical calculation derived in (4), it is superimposed on the full-circuit SPICE simulation in Fig. 5. It reveals good matching within the 3-dB bandwidth of 4 GHz. It is worth mentioning that although the g_m-boost transistor, M_0, slightly increases the parasitics at the input node, its small size does not affect the bandwidth substantially. Figure 6 shows the effect of M_0 size on the bandwidth: By increasing the size of M_0 from 10 to 20 μm, the upper cutoff frequency drops by 210 MHz, from 3.9 GHz to 3.69 GHz.

C. Noise Analysis

As mentioned above, the proposed LNA exploits the two-fold noise cancellation to lower the NF. The first (conventional) technique is applied to the CG structure. The second (new) technique is used for the CS transistors in the second stage.

1) First Noise Cancellation for CG Transistors: As mentioned, to compensate for the high NF of the CG structure, the noise cancellation technique is applied to cancel the thermal noise of the input transistor (see Fig. 1). The two noise voltages generated due to the thermal current noise of M_1 are calculated as $\overline{V}^2_{nN} = Z^2_N \cdot \overline{I}^2_{n,M1}$ and $\overline{V}^2_{nP} = -Z^2_P \cdot \overline{I}^2_{n,M1}$. Thus, the current noise (I_{n2}) generated in the second stage

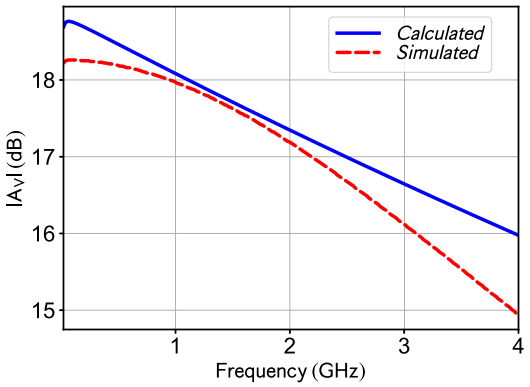


Fig. 5. Simulated and theoretically derived gain A_v.

must be canceled:

$$\overline{I}_{n2}^2 = \overline{V}_{nN}^2 g_{m2}^2 - \overline{V}_{nP}^2 g_{m3}^2 = 0 \tag{5}$$

$$\rightarrow \frac{g_{m2}}{g_{m3}} = \left|\frac{Z_P}{Z_N}\right| \approx \frac{R_{D1}}{R_s} \tag{6}$$

To reuse the current of M_2, M_3 is selected as a pMOS transistor. By applying the noise cancellation condition, the noise factor of the structure shown in Fig. 1 (i.e without yet applying the proposed third stage), $F_{(\text{fig1})}$, is equal to $F_{(\text{fig1})} \cong 1 + F_{M2} + F_{M3}$ where the noise factor terms are given by:

$$\begin{aligned} F_{M2} &= \frac{4kTg_{m2}|Z_Q|^2}{4kTR_sA_v'^2}\frac{\gamma}{\alpha} = \frac{4g_{m2}}{R_s(|Z_P|G_{m1}g_{m3}+g_{m2})^2}\frac{\gamma}{\alpha} \\ &\cong \frac{1}{R_s(g_{m2})}\frac{\gamma}{\alpha} \\ F_{M3} &= \frac{4kTg_{m3}|Z_Q|^2}{4kTR_sA_v'^2}\frac{\gamma}{\alpha} = \frac{4g_{m3}}{R_s(|Z_P|G_{m1}g_{m3}+g_{m2})^2}\frac{\gamma}{\alpha} \\ &\cong \frac{1}{|Z_P|^2G_{m1}g_{m3}}\frac{\gamma}{\alpha}. \end{aligned} \tag{7}$$

where A_v' is the voltage gain of the Fig. 1 LNA and given in Section II-B, γ is the excess noise factor in short channel devices, and α is the ratio of the transconductance g_m to the zero-bias drain conductance g_{d0}. Moreover, Z_P and Z_Q were calculated in Section II-B. Since the entire parasitic capacitance, C_N, at the input node is damped by L_s, the relationship $Z_{in} = Z_N = R_s = 1/G_{m1}$ is assumed. Thus, F_1 is approximately given by:

$$F_{(\text{fig1})} \cong 1 + \frac{\gamma}{\alpha R_s g_{m2}} + \frac{\gamma}{\alpha|Z_P|^2(G_{m1})g_{m3}} \tag{8}$$

As stated by (8), the noise performance gets better by canceling the noise effect of M_1, whereas the thermal noise of $M_{2,3}$—i.e. common source transistors—now substantially influences the noise factor. Moreover, according to (6), to fully cancel the noise of M_1, g_{m2} should be at least 8× larger than g_{m3} (i.e $R_{D1}/R_s \geq 8$), leading to a large size for transistor M_2, which increases the power and parasitic capacitance at the output node. The proposed second noise-cancellation technique is applied for both canceling out the noise of M_2 and relaxing the design constraints on the first cancellation stage (M_2).

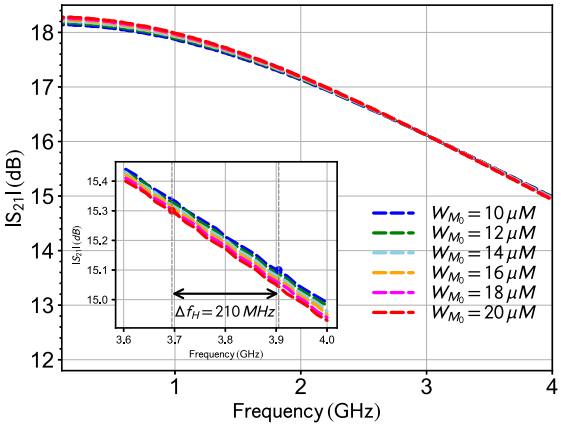


Fig. 6. Simulated S_{21} for different values of M_0.

2) Proposed Second Noise Cancellation for CS Transistors: By proposing the second noise-cancellation stage (i.e M_4, M_5), the noise of both the first and second stages (i.e the input and first noise cancellation stages) are canceled twice through the proposed two-fold noise cancellation technique.

As shown in Fig. 2, firstly, the noise of M_1 reduces significantly at node Q through $M_{2,3}$; then it is canceled completely at the output node by passing through the second noise-cancellation stage. Hence, the noise-cancellation criterion of the input transistor is calculated as:

$$\frac{g_{m2}g_{m5}Z_Q + g_{m4}}{g_{m3}g_{m5}} = \left|\frac{Z_P}{Z_N}\right| \approx \frac{R_{D1}}{R_s} \tag{9}$$

The noise current of transistor M_2 flows through the feedback resistor, R_F, to node S (i.e AC-wise, it has the same voltage as at node N) and 'instantaneously' creates two noise voltages at nodes S and Q with the same phase but different amplitudes. On the other hand, the *signal* voltage at these nodes has opposite phases and different amplitudes due to the inverting amplifier. The difference between signal and noise polarities at nodes S and Q makes it possible to cancel the M_2 noise while adding the signal contributions constructively.

The thermal current noise of M_2 is canceled twice at node Q and at the output. Firstly, the noise voltage at node S, $\overline{V}_{nS}^2$, is amplified and inverted by M_1 and M_3 and added with the already generated noise voltage at node Q, $\overline{V}_{nQ}^2$. Hence, the noise of M_2 reduces significantly at node Q. Moreover, $\overline{V}_{nS}^2$ is amplified and inverted by M_4. Also, the noise voltage at node Q, $\overline{V}_{nQ}^2$, is passed across M_5 without any change in phase. Finally at the output, these two noise voltages with opposite phases are added. Therefore, the channel thermal noise of M_2 will be canceled completely at the output provided the following condition is satisfied:

$$\frac{g_{m5}g_{m3}G_{m1}Z_PZ_Q + g_{m4}}{g_{m4}} = \frac{(R_F+R_s)|||Z_Q|}{R_s} \cong \frac{|Z_Q|}{R_s} \tag{10}$$

By canceling the thermal noise of transistors $M1$ and M_2, the most important noise sources in this two-fold noise cancellation scheme are the thermal noise of R_{D1} and the channel thermal noise of transistors M_4, and M_5. The noise factor of the proposed LNA is equal to $F = 1 + F_{R_{D1}} + F_{M4} + F_{M5}$,

where the $F_{R_{D1}}$ term is given by the following relation:

$$F_{R_{D1}} = \frac{4kTR_{D1}(g_{m3}g_{m5}|Z_Q Z_{out}|)^2(Z_{o1}/(Z_{o1}+R_{D1}))^2}{4kTR_sA_v^2} \cong \frac{4Z_Q^2}{G_{m1}R_{D1}(1+Z_Q)^2} \quad (11)$$

where Z_{o1} is the impedance seen from the drain of transistor M_1 and is equal to $Z_{o1} = [r_{ds1} + (R_s||1/sC_N||sL_s)(1 + G_{m1}r_{ds1})]$. The F_{M4} and F_{M5} terms are derived as:

$$F_{M4} = \frac{4kTg_{m4}|Z_{out}|^2}{4kTR_sA_v^2}\frac{\gamma}{\alpha} = \frac{\gamma 4g_{m4}}{\alpha R_s[(|Z_P|G_{M1}g_{m3}+g_{m2})g_{m5}|Z_Q|+g_{m4}]^2} \quad (12)$$

$$F_{M5} = \frac{4kTg_{m5}|Z_{out}|^2}{4kTR_sA_v^2}\frac{\gamma}{\alpha} = \frac{\gamma 4g_{m5}}{\alpha R_s[(|Z_P|G_{m1}g_{m3}+g_{m2})g_{m5}|Z_Q|+g_{m4}]^2} \quad (13)$$

where $g_m r_{ds} \gg 1$ and $(R_F + R_s/2) \gg Z_Q$ is assumed.

By exploiting the two noise cancellation techniques, the noise factor is given by the following formula, in which the noise-cancellation and input-matching conditions are applied for simplification:

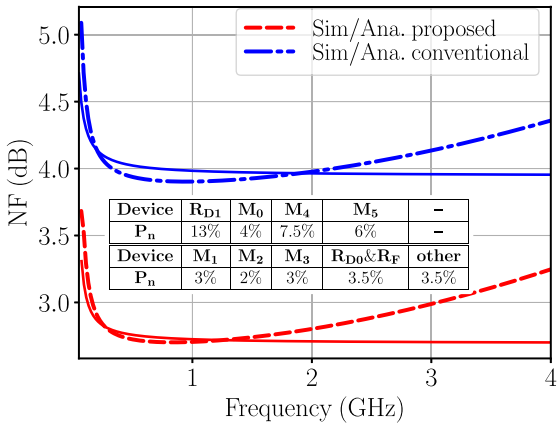
$$F \cong 1 + \frac{\gamma 4g_{m4}}{\alpha R_s[(|Z_P|G_{m1}g_{m3}+g_{m2})g_{m5}|Z_Q|+g_{m4}]^2} + \frac{\gamma 4g_{m5}}{\alpha R_s[(|Z_P|G_{m1}g_{m3}+g_{m2})g_{m5}|Z_Q|+g_{m4}]^2} + \frac{4Z_Q^2}{G_{m1}R_{D1}(1+Z_Q)^2} \quad (14)$$

The channel thermal noise of the third stage is incorporated in (14). However, the effect of the third and fourth terms of (14)—i.e. the noise effect of the third stage referred to the input—is very small because it is divided by the total voltage gain of the LNA so that it has the least influence on the total noise factor. Therefore, it is expected that the presented structure achieves a very low noise figure by virtue of meeting the noise cancellation conditions. The main drawback of the proposed structure is the additional extra branch in the LNA signal path, which slightly increases the power consumption.

The efficacy of the proposed two-fold noise-cancellation technique of Fig. 2 is depicted by the NF circuit simulation plots in Fig. 7 with superimposed analytical plots to verify the derived noise equations. It is also compared with the conventional noise cancellation presented in Fig. 1. By applying the proposed technique, the total NF improves by more than 1 dB compared to the conventional technique (e.g. Fig. 1). Moreover, this technique relaxes the design constraints on M_2, which helps to provide the noise cancellation criteria at a smaller transistor size.

D. Linearity

We have shown that by applying the two noise-cancellation techniques, the noise performance of the proposed LNA can be improved. Moreover, the nonlinearity of the CG transistor,



Device	R_{D1}	M_0	M_4	M_5	–
P_n	13%	4%	7.5%	6%	–
Device	M_1	M_2	M_3	R_{D0}&R_F	other
P_n	3%	2%	3%	3.5%	3.5%

Fig. 7. Comparison between the simulated (dotted line) and derived [solid line, formulas (8) and (14)] NF of the conventional and proposed LNA. The simulated contributions of each device of the proposed design is shown in inserted table.

including its second- and third-order products, can be modeled as a nonlinear current source between its drain and source, controlled by both V_{gs} and V_{ds}. This nonlinear current also produces two voltage drops at nodes N and P which can be defined based on Volterra series and can be completely neutralized at the output if the non-linearity cancellation conditions are satisfied [8], [11]. This analysis is not provided here; however, intuitively, meeting the noise cancellation criteria helps to decrease the intrinsic distortion generated by M_1, including g_m and g_{ds} nonlinearities.

Moreover, by biasing transistor M_1 in a "sweet spot", its third nonlinearity coefficient (i.e. g_m'' which is the second derivative of g_m) will be zero, which improves the linearity performance of the proposed LNA. The "sweet spot" biasing means that the external supply voltage for the M_1 biasing is set to its optimal value to adjust for the process spread (see Fig. 8) before the full suite of performance measurements, and is *not* adjusted afterwards. It is worth mentioning that the sweet-spot biasing only pertains to M_1 and is not relevant for the other transistors, hence its complexity is only 1-dimensional, thus manageable. More importantly, it is quite insensitive to the process and temperature variations, as verified by the simulations in Figs. 8(a) and (b), respectively. By changing the temperature, the second derivative of gm, g_m'', which has a direct effect on IIP3, shifts only slightly, 50 mV. Furthermore, since M_1 is mainly applied for the input matching, placed in the first stage, its effective gain is not high, so its linearity contribution is less dominant and the signal provided to the second stage is still small. In other words, it is biased mainly to provide the required g_m for the input matching. Moreover, Fig. 8(c) shows the variation of g_m'' versus V_{B1} for different values of V_{DD}, which also confirms the "sweet spot" of the first stage is less sensitive to the V_{DD} variations. As a result, the V_{DD} and temperature induced variations of g_{m1}'' show that M_1 is not significantly sensitive, so there is no strong need to use the g_m-constant biasing here.

Finally, it is worth mentioning that it is the $M_{2,3}$'s distortion that dominates the residual nonlinearity. It can also be modeled as a nonlinear current between their drain and source. By passing this current through R_F and R_s, two nonlinear

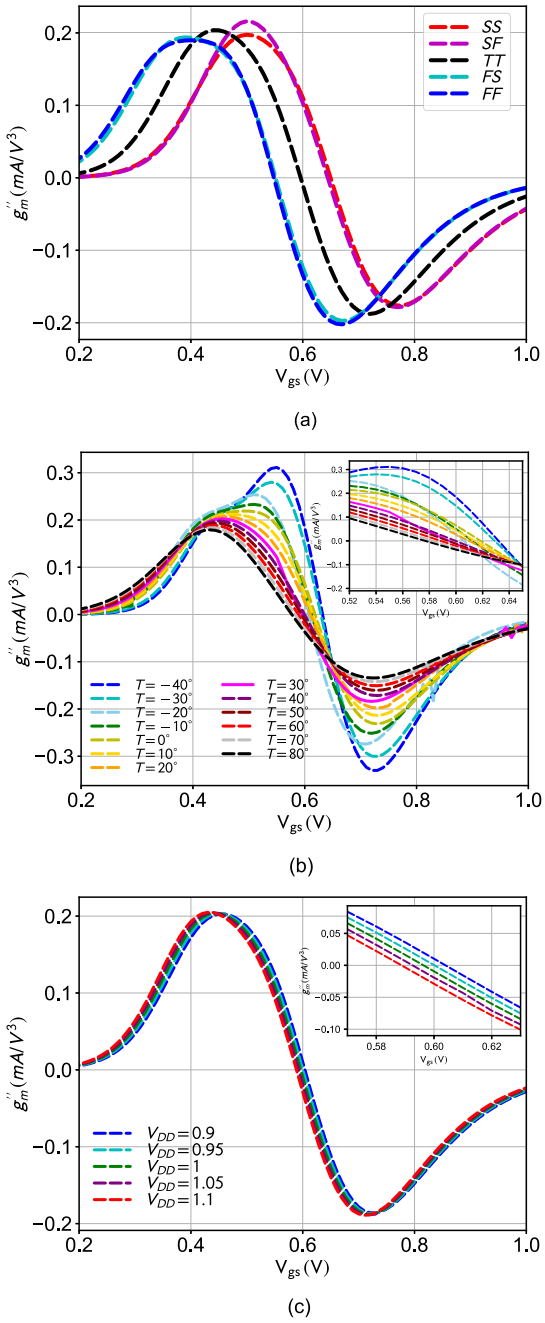


Fig. 8. (a) Process, (b) temperature, (c) $V_{\rm DD}$ variations of third-order derivatives of the drain-source DC current, i_{ds}, with respect to V_{gs} of M_1.

voltages are created at nodes Q and S, which, by extending the Volterra series at these nodes, it can be shown that the second noise-cancellation technique can help to reduce the effects of nonlinearities of $M_{2,3}$ [11], [12]. Moreover, the second-order non-linearities of nMOS and pMOS transistors ($M_{2,3}$) neutralize each other's effects. As a result, the effective IM2 decreases significantly leading to a significant improvement in the IIP2.

III. Measurement Results

The proposed 0.02–2 GHz LNA is fabricated in TSMC 28-nm bulk LP CMOS, whose microchip photograph is shown in Fig. 9. The device dimensions are shown in the table

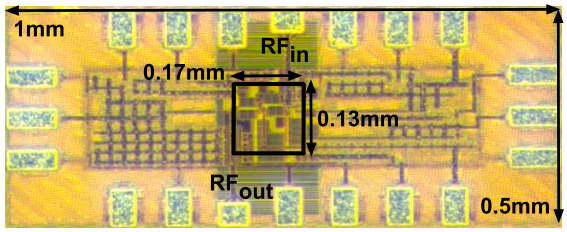


Fig. 9. Microchip photograph.

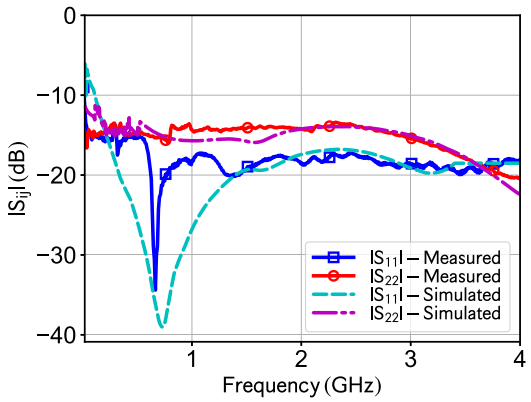


Fig. 10. Measured and simulated input and output return loss.

TABLE I
Biasing and Measured Current Consumption

V_{B0}	0.65 V	I_0	1 mA
V_{B1}	0.50 V	I_1	0.7 mA
V_{B2}	0.48 V	I_3	1.3 mA
V_{B3}	0.35 V	I_5	1.1 mA
V_{B4}	0.6 V	–	–
V_{B5}	0.7 V	–	–

in Fig. 2. Moreover, the biasing and measured current consumption are listed in Table I. Although the advanced technology node transistors provide better noise performance, their intrinsic gain, $g_m/g_{\rm ds}$, reduces because the output conductance increases as a result of poorer short-channel control. Moreover, by going from older technology to an advanced one, $V_{\rm DD}$ is normally reduced by almost half while the MOS threshold voltage, $V_{\rm th}$, does not change considerably. Hence, the available voltage headroom reduces dramatically, as does the gain. By means of the two-fold noise-cancellation technique, it is now possible to achieve a reasonably high and flat small-signal gain with a low NF performance. This LNA is able to reach 18.5 dB of maximum gain with NF of 2.5 dB, while dissipating only 4.1 mW.

Figure 10 shows the input and output return loss, $|S_{11}|$ and $|S_{22}|$, versus frequency. The use of CG transistors in the input stage provides an acceptable $|S_{11}|$. The measured $|S_{11}|$ is $\leq$-15 dB over the 0.02–4 GHz bandwidth. The simulated and measured transfer functions are plotted in Fig. 11. The 3 dB gain variation is between 18.5 down to 15.5 dB in the 0.02–2 GHz bandwidth. This architecture was designed to achieve the upper band at $f_H = 4$ GHz, as shown in Figs. 11 simulations. Unfortunately, the measurement result cannot explicitly show it because of the larger wire-bonding induc-

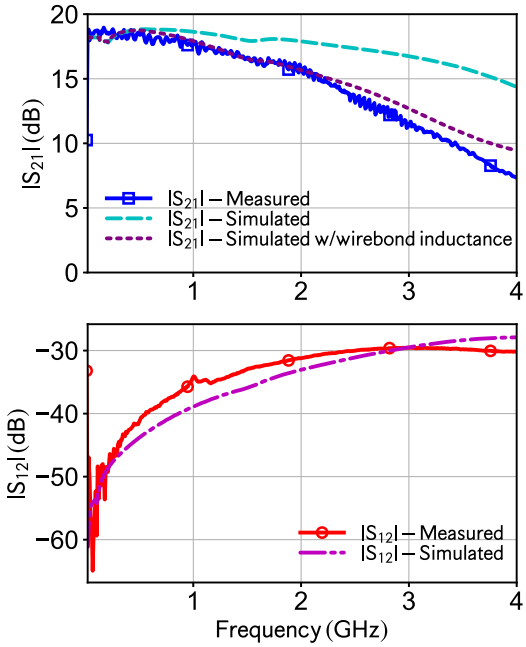


Fig. 11. Measured and simulated: (top) gain S_{21}, and (bottom) isolation S_{12}. The dotted curve in (a) is the simulated gain by considering 1 nH for the wire-bonding inductance and 700 fF for the parasitic PCB capacitance.

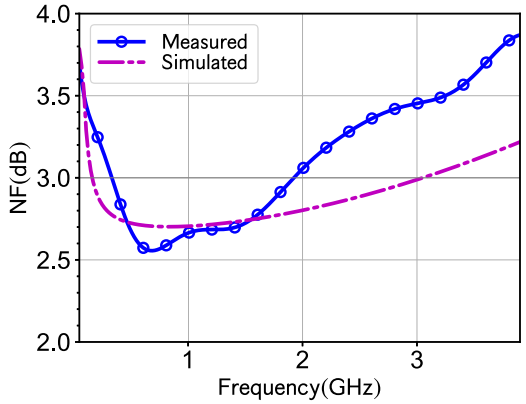


Fig. 12. Measured and simulated NF.

tance and parasitic capacitance of the pad and traces on the printed circuit board. The wire-bonding inductance decreases the upper limit of the bandwidth to 2 GHz (wire-bonding is estimated between 1 nH and 1.5 nH, also confirmed by the dotted-line simulation plot with the inclusion of wirebonding inductor). Furthermore, the pad capacitance also causes the bandwidth limitation. It is worth mentioning that this issue is irrelevant in integrated receivers or if the LNA is followed by an integrated mixer on the same die.

Figure 12 plots the NF, which exhibits a particularly close agreement with the simulations below 2 GHz, where the gain is matched as well. The NF varies from 2.5 dB to 3.5 dB in the 2 GHz bandwidth, where it is below 3 dB (from 330 MHz to 2 GHz). As the gain drops above 2 GHz, the NF gets deteriorated. By carefully designing the PCB and choosing high Q-factor off-chip passive components, the NF could be further improved.

A two-tone RF signal at 100 MHz, 500 MHz, 1 GHz, 2 GHz, 3 GHz and 4 GHz (i.e. at the beginning, middle and end of

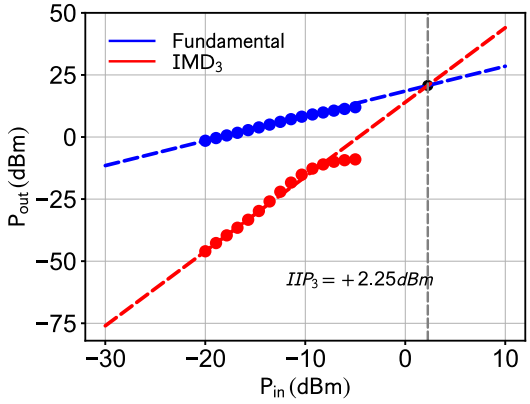


Fig. 13. Measured IIP3 at maximum gain.

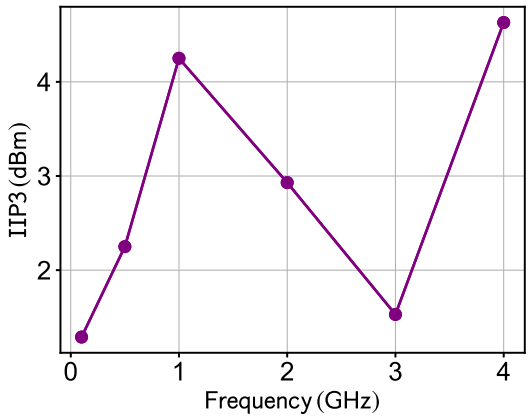


Fig. 14. Measured IIP3 versus frequency.

the band) is used to measure the wideband linearity performance. As shown in Fig. 13, the measured IIP3 at 500 MHz with 10 MHz spacing, where the maximum gain is reached, is +2.25 dBm. Figure 14 shows the measured IIP3 versus frequency, where +4.25 dBm is the maximum IIP3 in the entire bandwidth occurring at 1 GHz.

To compare the proposed LNA with recent state-of-the-art stand-alone wideband RF LNAs, and to emphasize the capability of reaching the lower frequencies in this wideband design, the following figures-of-merit (FoM) introduced in [5] and [4] and the overall results are summarized in Table II.

$$\text{FoM}_1 = \frac{\text{Gain}_{\text{av}}[\text{abs}] \times (f_H - f_L)[\text{GHz}]}{(F_{\text{av}} - 1) \times P_{\text{dc}}[\text{mW}]} \tag{15}$$

$$\text{FoM}_2 = \frac{\text{Gain}_{\text{av}}[\text{abs}] \times (f_H - f_L)[\text{GHz}] \times \text{IIP3}[\text{mW}]}{(F_{\text{av}} - 1) \times P_{\text{dc}}[\text{mW}]} \tag{16}$$

$$\text{FoM}_3 = \frac{\text{Gain}_{\text{av}}[\text{abs}] \times (f_H - f_L)[\text{GHz}] \times \text{IIP3}[\text{mW}]}{(F_{\text{av}} - 1) \times f_L[\text{GHz}] \times P_{\text{dc}}[\text{mW}]} \tag{17}$$

where Gain_{av} is the average power gain, F_{av} is the average noise factor over the 3 dB frequency range f_L to f_H, and P_{dc} is the power consumption. This LNA achieves the best FoM (i.e FoM_3), features high power gain and high linearity and low noise figure, while drawing only 4.1 mA current from the 1 V supply. The proposed LNA reaches the record-low 3 dB bandwidth cutoff frequency f_L of 20 MHz which makes it suitable for certain applications, such as software defined radio (e.g. Aaronia SPECTRAN V6 or AD-FMCOMMS4-EBZ). It maintains high performance and low power consumption,

TABLE II
SUMMARY AND COMPARISON WITH STATE-OF-THE-ART WIDEBAND LNAS

	This work	[4] JSSC'21	[13] TCASI'20	[14] TCASI'19	[15] TCASII'19	[16] TMTT'19	[17] TCASI'18	[18] TCASII'18	[19] MWCL'21	[20] MWCL'14
Noise cancel. used?	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	No
Core drive ext. 50Ω?	Yes	Yes	No**	No**	Yes	No**	No**	No**	No**	No***
CMOS tech. [nm]	28	28	65	65	65	65	65	180	130	180
BW_{3-dB} [GHz]	0.02∼2	0.02∼4.5	0.05∼1.3	0.05∼1	0.4∼2.2	0.3∼4.4	0.2∼2.7	2∼5	0.1∼1	0.025∼1.4(#)
S_{11} [dB]	≤-15	≤-10	–	≤-10	–	–	–	–	<-10	-15
S_{21} [dB]	18.5	15.2	27.5	30	16.4	26.7	21.2	13	14	10
IIP3 [dBm]	+1.29∼+4.25	-4.6∼-3.53	-4∼-1	-4∼-1	-5	-14.2	-2	-9.5	+2	-1
IIP2 [dBm]	+19.6∼+27.6	+3.49∼+7.25	+10∼+19.6	+10.7∼+20.6	–	–	–	–	–	–
P-1dB [dBm]	-6.5	–	–	–	–	–	-22.2	-15	–	–
NF [dB]	2.5∼3.5	2.09∼3.2	2.3∼3	2.3∼3.3	2∼2.5	3∼4.4	3∼3.5	6∼8	4	5
VDD [V]	1	1	1	2.2	1.2	1	1.2	1.8	1.2	1.5
Power [mW]	4.1	4.5	5.7	19.8	29	13.7	0.96	1.8	2.7	7.5
Active area [mm^2]	0.022	0.03	0.046	0.0448	0.16	0.009	0.05	0.72	0.099	0.033
FoM_1	5.22	7.76	6.18	2.17	0.7	6.5	30.04	2.49	1.1	0.27
FoM_2	13.89	3.452	3.48	1.7	0.22	0.24	18.95	0.28	1.75	0.21
FoM_3	694	172.6	69.56	34.52	0.55	0.82	94.77	0.14	17.5	8.22

* Single-ened load is 100 Ω. ** Uses addt'l on-chip measurement buffer. *** Needs addt'l external measurement buffer.
# Estimated from plots.

especially compared with [20]. It can also directly drive the external 50 Ω load, while most other reports require additional buffers which do not count towards their final power consumption numbers. Although [17] achieves comparable gain with better power consumption, the acceptable wideband input matching cannot be provided in the whole reported bandwidth based on its $|S_{11}|$ performance. Moreover, its noise and linearity performance are worse than in our structure. It also requires a higher supply of 1.2 V. Although [21] reaches quite high FoM due to its low power consumption, its gain, NF and IIP3 performance get compromised. Even though [13] provides high gain and slightly better NF, its linearity is worse, while consuming more power and occupying 2× the area. Moreover, [19] consumes lower dc power; however its NF, gain and bandwidth performance are worse, and it needs a higher 1.2 V supply, while requiring an additional buffer to drive the external 50 Ω load. Finally, [22] consumes less dc power and provides a bit higher gain; however its NF and linearity performance are worse even at a higher 1.2 V supply, and it requires an extra buffer to drive the external 50 Ω load. Moreover, it requires a couple of external high-quality current sources to directly bias its input stage.

IV. CONCLUSION

In this paper, a 20 MHz–2 GHz wideband LNA was proposed and verified in 28-nm CMOS. The LNA comprises three stages to achieve a low NF and to extend the high edge of bandwidth. The main idea is to cancel the channel thermal noise of the first noise-cancellation stage by using another cancellation stage, i.e. third LNA stage. To improve both the linearity and power consumption, a pMOS/nMOS structure is exploited in the second stage where the resistive feedback is applied to prevent high impedance nodes from dc variations. The measurement results show that throughout the entire bandwidth a high gain is achieved and the input and output matching are well met, with good noise and linearity performance. The upper frequency band of 2 GHz is limited by the output pad parasitics and bondwire; per simulation, it increases to 4 GHz when the pad gets eliminated (e.g., when integrating with a mixer).

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