Design of Low Power 5-bit Hybrid Flash ADC

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***Abstract*—In this paper, a low power 5-bit hybrid flash architecture is proposed. The proposed analog-to-digital converter (ADC) uses appropriate combination of both conventional double-tail comparators and standard cell comparators. Standard cell comparators are used to reduce power consumption. Thus, the proposed hybrid architecture results in extended dynamic range when compared to standard cell and threshold inverter quantization (TIQ) based flash ADC. The proposed hybrid architecture is implemented in CMOS 180 nm N-well technology with 1.8 V supply. Simulation results show the power reduction upto 48.47% when compared to conventional architecture. The simulated spurious-free dynamic range (SFDR) is 38.54 dB and effective number of bits (ENOB) is 4.7 bits with a 1.22 MHz input at a sampling rate of 250 MS/s. The hybrid ADC consumes about 7.11 mW of power with figures of merit (FOM) of 1094.18 fJ/conversion-step.**

***Index Terms*—Analog to digital converters, multiplication factor, threshold inverter quantization, standard cell, automated synthesis.**

I. Introduction

Flash architecture is the most efficient analog-to-digital converter (ADC) in terms of speed. A conventional N-bit flash ADC consists of 2^{N-1} comparators, resistive ladder and digital encoder as shown in Fig. 1. This architecture is limited by high power dissipation with the increase in resolution. A 4-bit flash ADC has power dissipation of 633 mW, when operated at sampling rate of 3 GS/s for input frequency of 100 MHz [1]. Several architectures such as folding and averaging converters [2], two stage flash ADC [3], [4] are proposed to improve the power performance. However, these architectures use analog components, which are difficult to integrate and also performance of system degrades as the technology scales down [5]. In literature the flash ADC built using only standard cell comparators showed less power consumption and less sensitive to noise [6]. Hence, there is a need to migrate the design more into digital like domain. In TIQ based flash ADC [7]-[9] comparators are designed by varying the feature size manually, which results in tuning problem. In standard cell design methodology [10], logic gates such as NAND, NOR, INVERTER and their combination is used to design the comparator with required built in reference voltage. But the TIQ and standard cell based flash ADC have the disadvantage of limited input range.

Comparator forms an essential component in ADC which converts an analog signal to digital. There are different types of comparators such as continuous time comparator [11], clock based dynamic and double-tail comparators [12], threshold inverter quantization (TIQ) based comparator [13] and standard cell based comparator [14]. Clock based dynamic comparators are widely used in many high-speed ADCs [15] due to strong positive feedback in the regenerative latch. These dynamic comparators [16] have the advantage of high input impedance, no static power consumption and rail-to-rail output swing. But they have the disadvantage of more delay due to several stacked transistors, which cannot operate at lower supply voltages. In addition to the advantages of dynamic comparator, the conventional double-tail comparator [12] has less delay and can operate at lower supply voltages. The standard cell comparators consume [10] less power compared to conventional double-tail comparators. As the standard cell comparators are designed with constant NMOS and PMOS aspect ratio, it can be used in automated synthesis. In this paper, a 5-bit hybrid flash ADC is proposed which incorporates the advantages of both conventional double-tail comparators and standard cell comparators. Thus, the proposed design uses optimized combination of these comparators, which results in reduction in power.

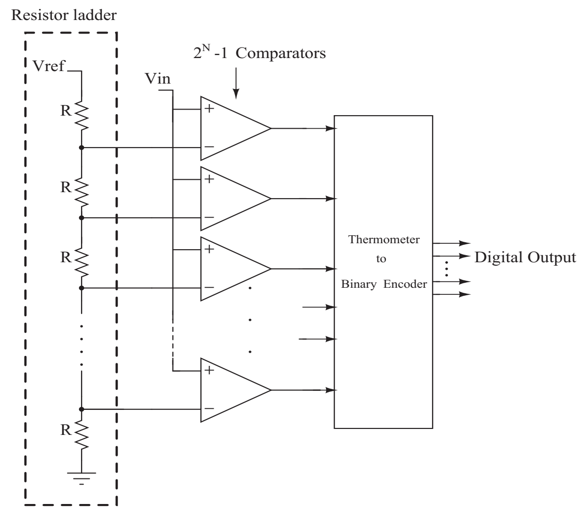

Fig. 1. Conventional N-bit flash ADC.

The rest of the paper is organised as follows: In Section II, conventional double-tail comparator and standard cell based comparator are discussed, followed by implementation of proposed 5-bit hybrid flash ADC architecture. Section III shows the simulation results. Finally, conclusions are drawn in Section IV.

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II. 5-BIT HYBRID FLASH ADC

The proposed hybrid ADC uses 2 types of comparators: 1) Conventional double tail comparator. 2) Standard cell comparator.

A. Conventional double tail comparator

A conventional double-tail comparator [12] is shown in Fig. 2. The comparator operates in two modes.

1) Reset mode: During this mode, CLK = 0, hence transistors M_{tail1} and M_{tail2} are OFF. Transistors M_3 and M_4 pre-charges f_n and f_p to V_{DD}, which causes transistors M_{R1} and M_{R2} to discharge the output nodes to ground.

2) Decision-making mode: In this phase, CLK is set to V_{DD}. Hence, transistors M_{tail1} and M_{tail2} are ON. Transistors M_3 and M_4 turn OFF and thus the voltage at node $f_{np(pn)}$ discharges with respect to the rate $I_{M_{tail1}}/C_{Lfn(p)}$. Thus, the differential voltage $\Delta V_{f_{np(pn)}}$ develops which is dependent on the input differential voltage. This difference voltage at node f_n and f_p is then passed by the M_{R1} and M_{R2} transistors to the cross-coupled inverter and hence provide a good shielding between input and the output, thus reducing kickback effect [17].

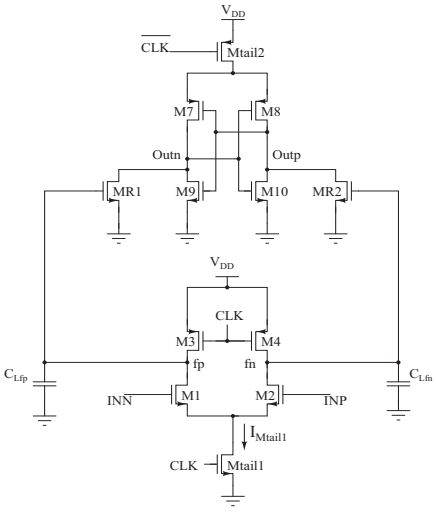

Fig. 2. Conventional double tail comparator.

This architecture can operate at lower supply voltage compared to conventional dynamic comparators [18], [19] because of less stacking. The double tail enables small current in the input stage for low offset voltages [20] and large current in the latching stage which is independent of common mode voltage V_{cm}.

B. Standard cell based comparator

Standard cell comparators consume less power compared to double-tail comparators because of following reasons: a) The reference voltage is internal to these comparators which avoids the use of resistor ladder. b) the need of power hungry analog components and additional biasing voltages are avoided. Using logic gates such as INVERTER, NAND and NOR, comparators can be designed with desired built-in reference voltage. The reference voltage of a comparator refers to threshold voltage of gate. The threshold voltage of gate V_{GTH} [10] is the input voltage for which the output is $V_{DD}/2$. The output of this comparator is '1' for the input voltage $V_{in} < V_{GTH}$ and '0' if $V_{in} > V_{GTH}$. Mathematically, the equation (1) gives the threshold voltage of a gate with all the inputs connected to V_{in}.

$$V_{GTH} = (V_{DD} - V_{TH} + MV_{TH})/(M+1) \qquad (1)$$

In the above equation V_{DD} is the supply voltage, V_{THn} = $|V_{THp}|$= V_{TH}, where V_{THp}, $|V_{THn}|$ are the threshold voltage of PMOS and NMOS transistors respectively and M is the multiplication factor of the gate.

M = 1 for INVERTER,
M = 1/b for b-input NAND gate,
M = a for a-input NOR gate.

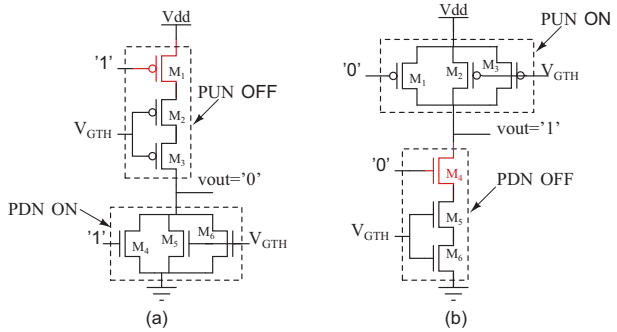

Fig. 3. (a). Three input NOR, (b). Three input NAND gate in standby mode.

The switching threshold voltage of a gate can be tuned by connecting another gate in parallel to it or by applying suitable control signal. The control signal for which the gate acts a comparator is called active signal and the gate is said to be in active mode. In active mode threshold voltage of NAND gate can be decreased by applying active signal '1'. Applying '0' as active signal, threshold voltage of NOR gate can be increased. Standby signal is the control input for which the output of gate is independent of input V_{in} and the gate is said to be in standby mode. In this case, the NAND and NOR gates output is '1' and '0' respectively for any given input. Precision in switching threshold is further enhanced by connecting more than one gate in parallel to an initial gate. Comparators with the reference voltage greater than $V_{DD}/2$ can be designed with gates having M<1 and the comparators whose reference voltage lesser than $V_{DD}/2$ can be designed with the gates having M>1. Comparators whose reference voltage is equal to $V_{DD}/2$ are designed using INVERTER with M=1.

In the active mode, standard cell based comparator consumes nominal power when input $V_{in} = V_{GTH}$. But at V_{in}= V_{GTH}, comparator in the standby mode consumes less power compared to that in the active mode. The low power consumption is achieved using the standby signal which switches either the pull up network (PUN) or pull down network (PDN) to

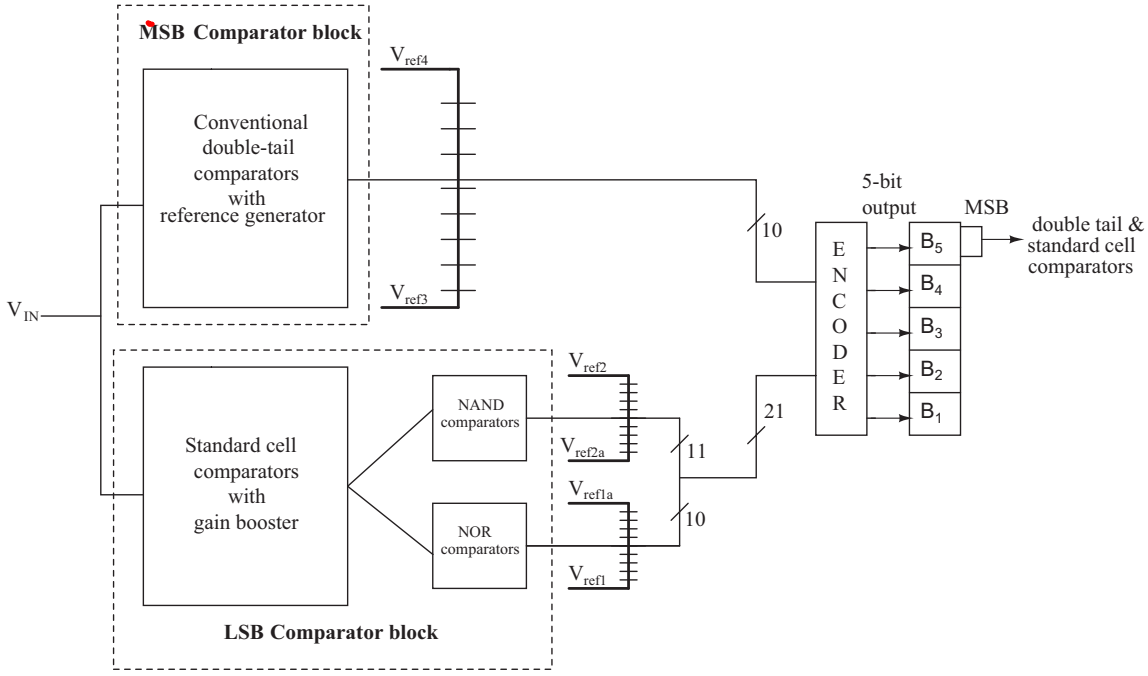

Fig. 4. Proposed 5-bit hybrid flash ADC I consisting of double-tail and standard cell comparators.

OFF state. Consider 3-input NOR gate in standby mode with the two inputs connected to $V_{in} = V_{GTH}$ and the remaining input is connected to standby signal '1' as shown in Fig. 3.(a) The standby signal '1' turns OFF the transistor M_1 thereby switching PUN to OFF state and turns ON transistor M_4 and hence, connecting V_{OUT} to '0' . Similarly, the behaviour of NAND gate in standby mode can be analysed from Fig. 3.(b). Thus, even at the gate threshold V_{GTH}, comparators in standby mode have zero static power consumption.

C. Proposed 5-bit hybrid flash ADC architecture

A conventional 5-bit flash ADC requires 31 comparators. Each comparator compares the input voltage with its reference voltage and gives output as '1' or '0'. The output of comparators are in thermometer code which is then converted to equivalent binary code using encoder [21]. As the conventional flash ADC consume more power, which is discussed in Section I, a low power hybrid flash ADC is proposed in this paper.

Fig. 4 shows the block diagram of proposed 5-bit hybrid flash ADC design I. The proposed design I consists of 2 comparator blocks namely MSB comparator and LSB comparator. The LSB comparator block consists of 21 standard cell comparators with minimum and maximum reference voltages V_{ref1} and V_{ref2} respectively. The MSB comparator block consists of 10 double tail comparators with minimum and maximum reference voltages V_{ref3} and V_{ref4} respectively. Since, the conventional double-tail comparators are less sensitive to process variations compared to standard cell comparators, they are used in MSB comparator block. Maximum number of standard cell comparators in LSB block are used to achieve low power consumption. Gain booster consisting of an inverter is used in the LSB comparator block and the reference generator consisting of resistive ladder is used in the MSB comparator block. Standard cell comparator produces output which is opposite to that of the conventional comparator. So, the output of the comparator is given to gain booster to get the required thermometer code and proper rail to rail voltage. Reference generator provides the required reference voltages for the MSB comparators.

Comparators C_1 - C_{21} in the LSB comparator block are the standard cell comparators, where the comparators C_1 - C_{10} have minimum and maximum reference voltages of V_{ref1} and V_{ref1a} respectively and the comparators C_{11} - C_{21} have minimum and maximum reference voltages of V_{ref2a} and V_{ref2} respectively. Fig. 5 shows that the comparators C_1 - C_{10} are designed using NOR and INVERTER as the maximum reference voltage, V_{ref1a} is less than $V_{DD}/2$. Fig. 6 shows that the comparators C_{11} - C_{21} are designed using NAND gates as the minimum reference voltage, V_{ref2a} is greater than $V_{DD}/2$. Power consumption in the LSB comparator block can be further decreased by effectively switching half of the standard comparators from active mode to standby mode using internally generated control signal C.

The signal C is generated by the comparator (COMP) with the help of input signal V_{IN}. The comparator generating control signal is designed with the gate threshold V_C = $(V_{DD}/2)$. For the input $V_{IN} < V_C$, the control signal is '0' as shown in Fig. 7(a). So, the comparators C_1 - C_{10} are in active mode and the comparators C_{11} - C_{21} are in standby mode. For the input $V_{IN} > V_C$, the control signal is '1'

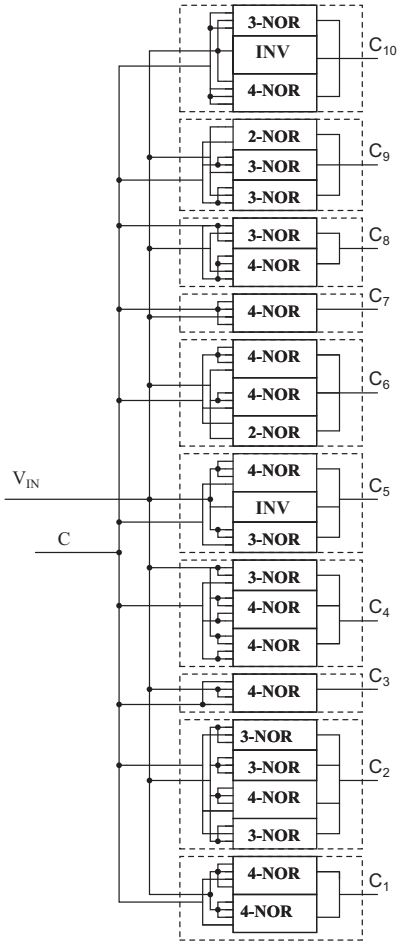

Fig. 5. Implementation of standard cell comparators C_1 - C_{10} using NOR, INVERTER gates.

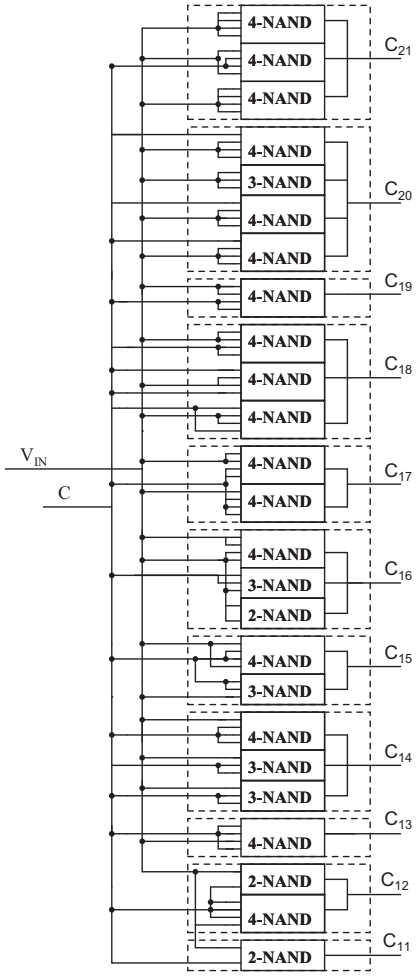

Fig. 6. Implementation of standard cell comparators C_{11} - C_{21} using NAND gates.

as shown in Fig. 7(b). So, the comparators C_1 - C_{10} are in standby mode and the comparators C_{11} - C_{21} are in active mode. Comparators C_{22} - C_{31} are designed using conventional double - tail comparator as shown in Fig. 8.

The output thermometer code T_1 - T_{21} corresponds to output of LSB comparator block and T_{22} - T_{31} corresponds to output of MSB comparator block. The thermometer code T_{31} - T_1 is passed through encoder, whose output is a binary code B_5 - B_1. The MSB bit B_5 is generated from T_{31} - T_{16}. Hence, bit B_5 is dependent on the output of both double-tail and standard cell comparators.

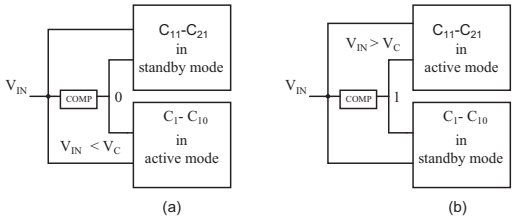

Fig. 7. Control signal generation for power saving mode (a) $V_{in} < V_C$, (b) $V_{in} > V_C$.

III. Simulation Results

The proposed 5-bit hybrid flash ADC and the flash ADC using double-tail comparators are simulated in 180 nm CMOS, N-well technology with the supply voltage of 1.8 V. The proposed hybrid ADC is designed to work at the sampling frequency (fs) of 250 MS/s with step size of 25 mV, V_{ref+}=1.425 V and V_{ref-}=0.625 V.

The differential non-linearity (DNL) and integral non-linearity (INL) measurements for the proposed hybrid ADC is shown in Fig. 9. Results show that the peak DNL and INL for the proposed design is 0.347 LSB and 0.52 LSB respectively. Fig. 10 shows the spectrum for 1.22 MHz sinusoidal input at a sampling rate of 250 MS/s for proposed design. Sine-wave SNDR is 29.96 dB with a 38.54 dB spurious-free dynamic range. The effective number of bits (ENOB) comes out to be

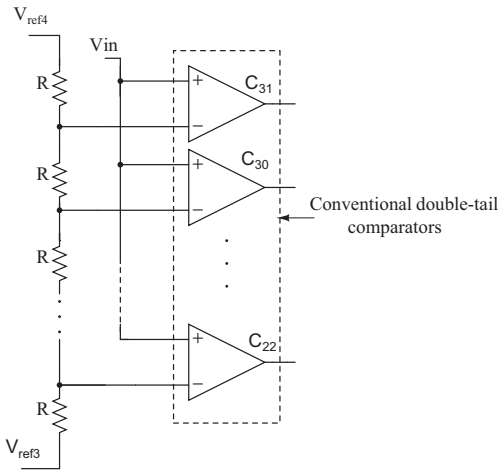

Fig. 8. MSB block containing conventional double-tail comparators with reference generator.

TABLE I
COMPARISION OF PROPOSED HYBRID FLASH ADC WITH EXISTING FLASH ADCS

Parameters	This Work	Flash ADC using double-tail comparator	[14]	[1]
Technology (nm)	180	180	180	180
Resolution (bits)	5	5	4	4
Sampling rate (MS/s)	250	250	400	3000
Input range (mV)	±400	±400	±257	±460
Supply	1.8	1.8	1.8	1.8
Input frequency (MHz)	1.22	1.22	1	800
SNDR (dB)	29.96	28.73	-	22.65
SFDR (dB)	38.54	34.45	25.16	-
DNL (LSB)	0.34	0.224	0.0016	0.15
INL (LSB)	0.52	1.61	0.024	0.24
Power consumption (mW)	7.11	13.8	6.9	633
FOM (pJ/step)	1.09	2.475	1.07	16.08

4.7. The performance metric of proposed design are compared with existing architectures and is tabulated in Table I. Table I shows that the proposed ADC consumes about 7.11 mW of power which reduces upto 48.47% as compared to flash ADC using double-tail comparators. The input dynamic range of the proposed flash architecture is also increased compared to [14]. The figure of merit (FoM) is given in equation (2),

$$FoM = \frac{Power}{2^{ENOB} * fs} \quad (2)$$

The proposed ADC shows better FOM value as compared to [1].

IV. CONCLUSION

In this paper, a 5-bit hybrid flash ADC design is proposed, which uses both conventional double-tail comparators and standard cell comparators. The proposed flash architecture has low power consumption as compared to conventional architecture. Low power consumption is achieved by using more number of standard cell comparators than double-tail comparators. In addition to low power consumption, the input dynamic range of the proposed flash architecture is also increased compared to standard cell and TIQ based flash ADC.

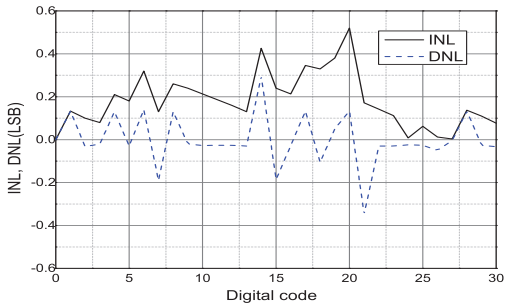

Fig. 9. DNL, INL plot for the proposed ADC I.

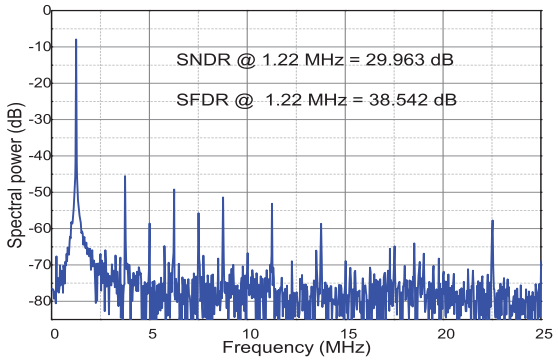

Fig. 10. Spectral plot for 1.22 MHz input sine wave at 250 MS/s.

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