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A novel process variation immune dopingless zero sub-threshold slope and zero impact ionization FET (DL-Z^{2}FET) based on transition metals

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Abstract Transition metal (TM) electrodes based dopingless zero sub-threshold slope and zero impact ionization FET (DL-Z^{2}FET) is reported in this paper. The work-function engineering of TM electrodes is used for charge plasma based electrostatic pseudo doping. Work-function difference between TM electrodes and the undoped silicon film induces p^+ and n^+ regions in the film. TMs exhibit easy tunability of work-function and their CMOS fabrication compatibility pledges for their potential applications as these electrodes. A technology computer-aided design simulation study is performed to provide physical insight into its working mechanism and performance. It exhibits all the inherent characteristics of conventional Z^{2}FET, viz. zero slope switching, high I_{ON}/I_{OFF} ratio, lower operating voltages, immunity towards hot electron degradation and gate controlled hysteresis. The detrimental doping control issues, mobility degradation due to heavy doping and statistical random dopant fluctuations can no more obviate the device performance, it results in more process variations immune design. Hence it can be a potential fast switching transistor.

Keywords Zero sub-threshold slope · Statistical random dopant fluctuations (RDFs) · Hot electron degradation · Gate controlled hysteresis

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1 Introduction

Sharp switching devices have been found to be fascinating with the advent of need to reduce the stand-by-leakage power in scaled CMOS technology. They are no more limited by the fundamental "Boltzmann Tyranny" or thermodynamic switching limitations (kT/q limit) of standard MOSFETs. A number of devices are reported in literature that are based on alternative current gating mechanisms such as impact ionization process [1] or quantum mechanical tunneling or [2–6]. By the same token of faster switching devices, there are also devices that employ positive-feedback to achieve steep switching behavior [7,8]. Thyristors use twin parasitic bipolar transistors initiated by impact ionization, exhibiting sharp switching with high drive current. One of its structural variants is the thin capacitive coupled thyristor (TCCT) [9,10] realized on fully depleted SOI (FD-SOI), it is reported to perform well as SRAM and DRAM memories. It requires precise doping control for reliable behavior [11]. Further dual gate structures for field effect diode (FED), is explored for high speed switch and gate controlled hysteresis. Recently, a novel device zero sub-threshold slope and zero impact ionization FET (Z^{2}FET) [12–14] working on positive feedback mechanism same as FED or FB-FET. But it has single gate and no trapped charges are involved. It demonstrates ultra steep switching (zero sub-threshold slope i.e., SS ($<$1 mV/dec)), I_{ON}/I_{OFF} ratio of the order of 10^8 and a larger gate controlled hysteresis in the drain current [15]. It is a forward biased p–i–n structure with gate semi-overlapped over the intrinsic region. Z^{2}FET is reported to be used for electrostatic discharge (ESD) protection, for capacitorless memory (1T-DRAM and 1T-SRAM) and high speed switching applications [16,17].

Despite of these advantages, it suffers from one major shortcoming of challenging fabrication process as steep dop-

ing profile is required for p–i–n scaled structure realization. Further, conventionally gate, source and drains are patterned using separate masks, thus the length of intrinsic region is prone to alignment errors [18]. These alignment errors induce various process variation related detrimental effects on device characteristics and hinders its scalability as well. Moreover, at such aggressively scaled device dimensions dopant fluctuations [19,20] and dopant activation [21] of highly doped source and drain regions of Z^2FET lead to higher thermal budget. It results in a critical bottleneck in its probable integration of CMOS process on SOI having polycrystalline silicon thin film transistors (TFTs). Additional photolithography and masking steps are required as compared to the conventional FET. This increases its fabrication cost immensely. Meanwhile, a number of recent publications demonstrate the great advancements in charge plasma based dopingless structures [22–27]. Further, the charge plasma based p–n diode (CP-diode) is already reported experimentally [28], it validates the concept of induced charge-plasma.

In order to address the aforementioned problems of conventional Z^2FET we conceptualize a TM electrodes based dopingless-Z^2FET (DL-Z^2FET) for process variation immune design for the first time. Here, the work-function difference between TM electrodes and undoped silicon film induces charge plasmas as pseudo doping. This realizes source and drain regions in intrinsic silicon. TMs exhibit significant capability to tune their work-functions via various techniques (silicidation and nitridation etc.) and their CMOS process compatibility makes them most desirable for this purpose. To elucidate the potentials of the proposed DL-Z^2FET, we have analyzed and compared it with conventional Z^2FET having identical dimensions and biasing conditions using TCAD. The most advantageous aspect of the proposed structure is its simplified fabrication process as ion-implantation and thermal annealing are no more required. It reduces the thermal budget of the device fabrication process, hence it facilitates its fabrication even on single crystal silicon-on-glass substrate [29,30] by wafer scale epitaxy transfer. It expedites the device's potential bio and opto compatibility [31]. Here, we have also proposed its various alternative modes of operation to explore its scalability.

This paper is organized as follows: Sect. 2 incorporates the device structure of DL-Z^2FET along with the simulation framework used for investigation. Simulation results and discussions about the characteristics of DL-Z^2FET are elaborated in Sect. 3. Section 4 covers its alternative operating modes to explore its scalability. Finally, Sect. 5 draws important conclusions from present investigation.

2 Device structure and simulation set-up

The schematic cross-sectional view of p-type conventional-Z^2FET, p-type DL-Z^2FET and n-type DL-Z^2FET are illustrated in Fig. 1a–c, respectively. It is a forward bias asymmetric p–i–n structure with gate semi-overlapped over intrinsic region (L_G) and the rest intrinsic region is left uncovered (L_{in}). Position of the gate with respect to channel decides the polarity of the device. For p-type device the gate is closer to n^+ region whereas, it is closer to p^+ region for n-type device. Accordingly source and drain swap their respective positions, region closer to the gate acts as drain. DL-Z^2FET consists of two TM electrodes having different work-functions grown on an intrinsic silicon film. In order to induce hole plasma, which will effectively act as p-region, metal M_1 must have work-function (ϕ_{M1}) greater than $\phi_{M1} > [\chi_{Si} + \frac{E_G}{2}]$ where, χ_{Si} is silicon electron affinity (χ_{Si} =4.17 eV) and E_G is band gap of bulk silicon. Similarly, to induce electron plasma to act as n-region, metal M_2 must have work-function (ϕ_{M2}) smaller than $\phi_{M2} < [\chi_{Si} + \frac{E_G}{2}]$. For better realization of electrostatic doping, difference between the work-functions of the two transition metals considered must be greater than 0.5 eV [22]. In the present work, we have considered Pt as metal M_1 with work-function as 5.93 eV and Hf as metal

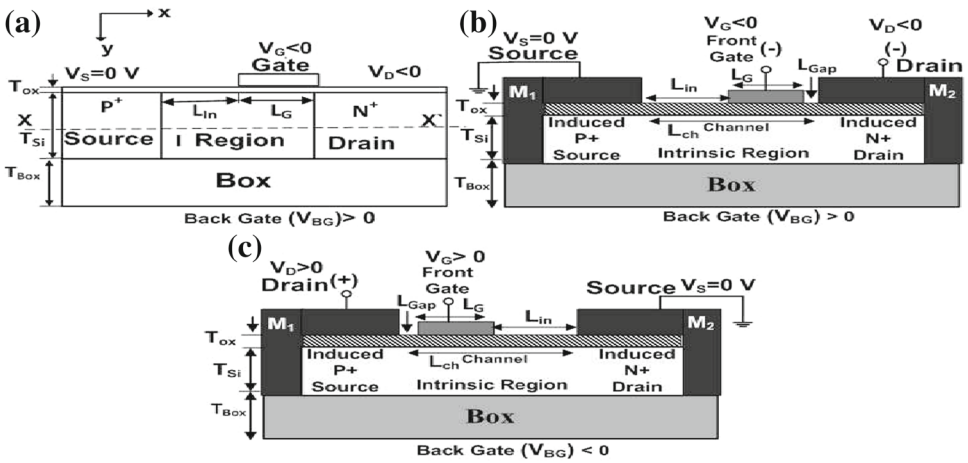

Fig. 1 Schematic cross-sectional view of **a** p-type conventional Z^2FET, **b** p-type DL-Z^2FET and **c** n-type DL-Z^2FET

M_2 having work-function 3.90 eV [23]. Another essential condition for charge plasma concept to substitute physical doping is the thickness of intrinsic silicon layer must be less than the Debye length [22], $L_D = \sqrt{\frac{\epsilon_{Si}}{q\beta N_C}}$ where, q is the elementary charge, N_C represents the charge concentration in silicon and ϵ_{Si} stands for the dielectric constant and β is the inverse of thermal voltage.

To analyze the device behavior we have used Silvaco ATLAS device simulator [32]. The simulation framework incorporates electric field and doping concentration dependent mobility models. Carrier life times are taken to be doping dependent. Band gap narrowing model (BGN), Shockley–Read–Hall (SRH) and Auger recombination at 300 K are also included. The validity of the simulator has been verified by calibrating its results against the previous literature data [16]. TMs are specifically used as they have low resistivity, high melting point and thermally stable. A number of transition metal layers such as tungsten, cobalt , erbium, palladium, molybdenum are already incorporated by bonding technology with low thermal budget [33–36]. Moreover, they have tremendous capability to tailor their work-functions via alloying, metal inter diffusion, silicidation and nitridation [37]. Some potential TMs with work-function data [38] are enlisted in Table 1, that can be employed to induce charge plasma (p/n-type) surrogate doping in silicon film. The detailed simulation parameters taken are enlisted in Table 2. Detailed conduction mechanism for DL-Z^{2}FET that employs positive feedback between gate controlled carriers injection barrier and carriers flow is shown in Fig. 7 and explained well in appendix section.

Table 1 Transition metals that can be used to induce hole/electron plasma (p/n-type) doping in silicon film [38]

Metals (M_1) to induce p-region	Ni	Pd	Au	Co	Ir
ϕ_{M1} (eV)	5.15	5.12	5.1	4.92	5.27
Metals (M_2) to induce n-region	Er	Y	Sc	Tl	Ti
ϕ_{M2} (eV)	3.09	3.1	3.5	3.84	3.96

3 Results and discussion

In order to investigate the proposed device, it is prerequisite to comprehend its operating mechanism in depth and it is revealed by its energy-band profiles. Figure 2a illustrates electron and hole concentration along the device length with horizontal cut-line at the center of the silicon film for p-type DL-Z^{2}FET and conventional Z^{2}FET, under thermal equilibrium state. Interestingly it is noticed that p^+–i–n^+ structure is realized even without any physical doping. The use of two TM electrodes having larger work-function difference with the intrinsic silicon film induces p^+ and n^+ regions. Hence the charge plasma formation concept is verified with TCAD simulation. The carrier concentration profiles of both devices are comparable. Figure 2b shows the carrier concentration in OFF state along the device length. The front gate bias $V_G = -2$ V and $V_{BG} = 2$ V bias accumulate holes and electrons under the gated region and ungated regions of intrinsic channel respectively. It realizes bias induced p–n–p–n thyristor like structure for both the devices considered with no channel doping. Figure 2c shows the carrier concentration in ON state along the device length. A redistribution of charge carriers takes place in both the devices after drain bias ($-V_D$) is applied. It is verified that the induced charges due to electrostatic doping is retained in thermal equilibrium and in biased states as well. Figure 2d depicts energy band

Table 2 Simulation parameters for conventional Z^{2}FET and DL-Z^{2}FET

Parameters	Z^{2}FET	DL-Z^{2}FET
Silicon thickness (T_{Si})	20 nm	20 nm
Gate length (L_G)	400 nm	400 nm
Intrinsic length (L_{in})	500 nm	500 nm
Source length (L_S)	100 nm	100 nm
Drain length (L_D)	100 nm	100 nm
Drain doping (N_D)	10^{20} cm^{-3}	–
Source doping (N_A)	10^{20} cm^{-3}	–
Background doping (N_{in})	1×10^{16} cm^{-3}	1×10^{16} cm^{-3}
Gate-oxide thickness (T_{ox})	2 nm	2 nm
M_1 work-function (ϕ_{M1}) (Pt)	–	5.93 eV
M_2 work-function (ϕ_{M2}) (Hf)	–	3.9 eV
Buried oxide thick (T_{Box})	140 nm	140 nm
Distance between gate and drain (L_{Gap})	–	5 nm

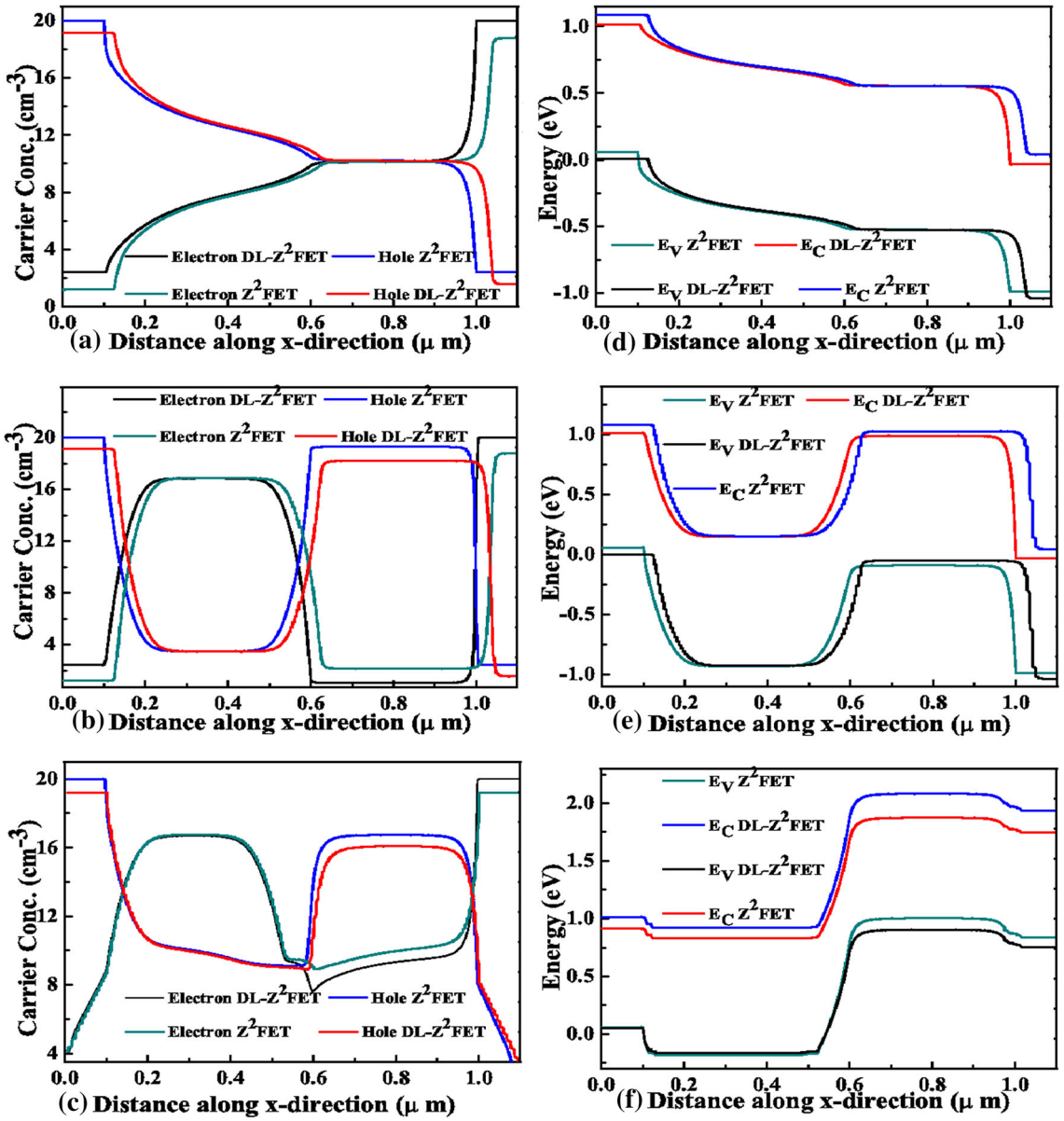

Fig. 2 Electron and hole concentration of p-type DL-Z^2FET and conventional Z^2FET along the device length under **a** thermal equilibrium, **b** OFF state, **c** ON state, and energy band diagram for **d** thermal equilibrium, **e** OFF state, **f** ON state

diagram along the device length for both devices under thermal equilibrium state. Under thermal equilibrium the energy band diagram of DL-Z^2FET also corresponds to the p^+–i–n^+ structure similar to the conventional Z^2FET. Figure 2e shows the OFF state energy band diagram along the device length at the center of the silicon film for both devices. In OFF state, as the two gate biases are applied they create injection barriers for the electrons and holes, thereby blocking their flow in OFF state. As a negative drain bias is applied it forward biases the channel drain junction and turns the device ON by initiating the positive feedback between gates biases induced injection barrier and carriers flow. ON state energy band diagram along the device length at the center of the silicon film for these devices is illustrated in Fig. 2f.

There are two probable biasing schemes for p-type Z^2FET as either drain is biased with a negative bias or source is biased with a positive bias to extract the transfer characteristics of the device. For conventional Z^2FET it is experimentally reported to have eight orders of change in the current level for 1 mV change in gate bias, i.e., SS < 1 mV/dec (effectively zero SS). Whereas to analyze transfer characteristics of DL-Z^2FET we have employed the process simulation along with the device simulation synergistically. The steps followed for the process simulation are based on the process followed to fabricate charge plasma diode [28] and proposed steps by Loan et al.

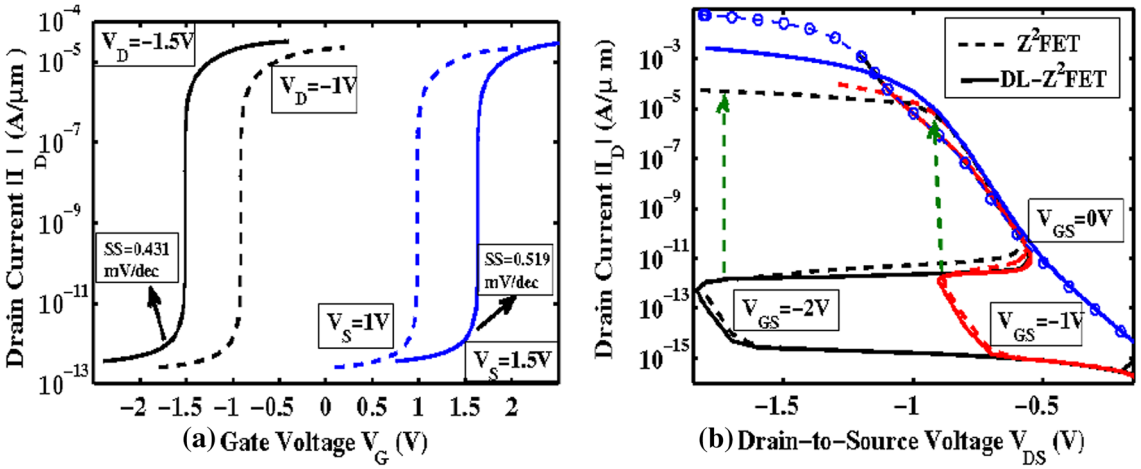

Fig. 3 **a** Transfer characteristics of DL-Z^{2}FET for two modes of operation ($V_D < 0$ V (*left side*) and $V_S > 0$ V (*right side*)) at $V_{BG} = 2$ V and **b** simulated $I_D - V_{DS}$ curve of conventional p-type Z^{2}FET and DL-Z^{2}FET

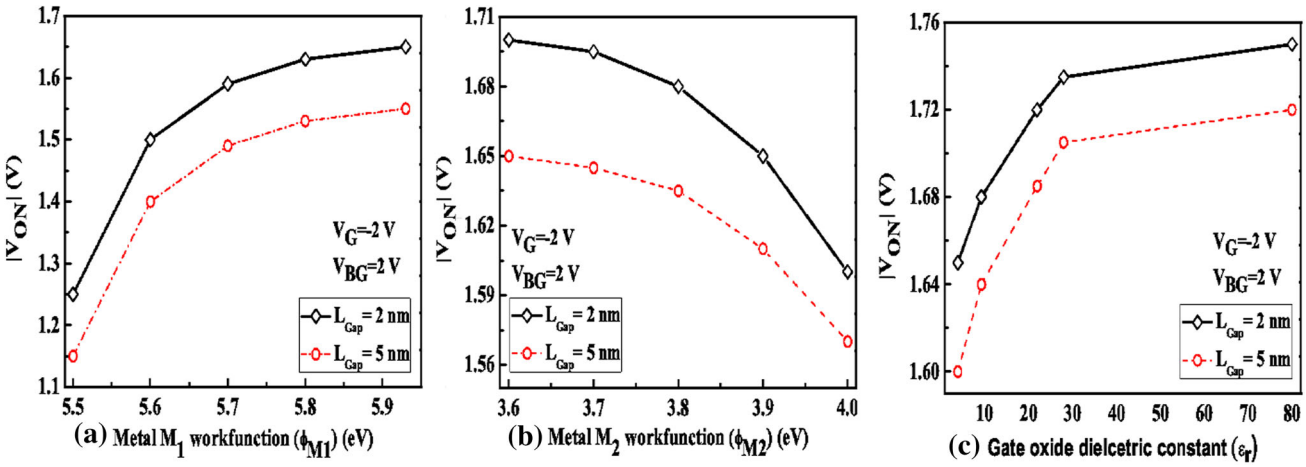

Fig. 4 **a** Impact of M_1 work-function on $|V_{ON}|$ with ϕ_{M2} is kept as constant as 3.9 eV, **b** effect of M_2 work-function on $|V_{ON}|$ with ϕ_{M1} is taken as 5.93 eV and **c** variation of $|V_{ON}|$ with gate oxide dielectric constant ϵ_r at $\phi_{M1} = 5.93$ eV and $\phi_{M2} = 3.9$ eV

[39] as they are similar charge plasma based devices. Figure 3a shows transfer characteristics of the device under two biasing modes (i) $V_D < 0$ V (left side, solid line for $V_D = -1.5$ V and dashed line for $V_D = -1$ V) and (ii) $V_S > 0$ V (right side, solid line for $V_S = 1.5$ V and dashed line for $V_S = 1$ V) at $V_{BG} = 2$ V for both the modes. The reported SS for both the cases is less than 1 mV/dec. Simulation results validate that DL-Z^{2}FET retains the zero-SS behavior. The switching behavior of DL-Z^{2}FET can be further improved by using different metals/alloys in place of the proposed metals. Further, switching point of the devices considered is bias dependent, this gives immense design flexibility during circuit designing. $I_D - V_{DS}$ characteristics of Z^{2}FET is unique, as it exhibits snap-back characteristics along with the gate controlled hysteretic behavior. This snap-back characteristics can not be observed even with quasi-static $I_D - V_{DS}$ measurements. Figure 3b depicts $I_D - V_{DS}$ curve of the conventional p-type Z^{2}FET (dashed line) and DL-Z^{2}FET (solid line). DL-Z^{2}FET and Z^{2}FET both show similar $I_D - V_{DS}$ characteristics. It demonstrates that the gate controlled hysteresis with turn-ON voltage ($|V_{ON}|$) is linearly dependent on the gate voltage. It is evident that there is a steep vertical transition in the current level for same V_D, which is indicated by the vertical green arrows.

In order to analyze the impact of work-functions of two metal electrodes on device parameters, we have carried out simulations of a V_{BG} operated device by keeping device dimensions and biasing identical. The effect of varying metal M_1 and M_2 work-functions, gate-oxide dielectric constant ϵ_r and the gap between gate electrode and drain (L_{Gap}) are demonstrated in Fig. 4a–c. Figure 4a explains the $|V_{ON}|$ with the variation of ϕ_{M1} from 5.5 to 5.93 eV and ϕ_{M2} is kept constant as 3.9 eV. The general trend is that $|V_{ON}|$ is governed by front and back-gate biases. Higher the gate biases controlla-

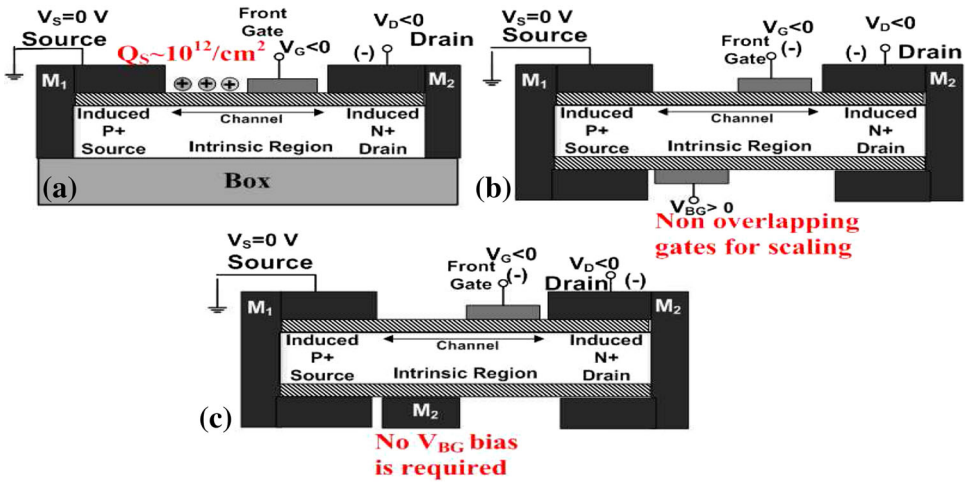

Fig. 5 Schematic cross-sectional view of **a** surface charge Q_s operated p-type DL-Z^{2}FET, **b** non-overlapping gate p-type DL-Z^{2}FET for enhancing scalability and **c** single gate operated p-type DL-Z^{2}FET

bility over the channel closer is value of $|V_{ON}|$ to the applied gate biases. It is noticed that higher gate bias controllability is observed for higher value of ϕ_{M1}, which results in $|V_{ON}|$ to be closer to the gate biases. It is due to the fact that at higher ϕ_{M1}, there is higher concentration of enhanced hole plasma in the source side. As a result the pseudo doping concentration for p^+ region increases, leading to lowered V_{sj} drop and it increases the impact of applied V_D in channel region. It enhances the gate controllability over channel region. Figure 4b illustrates the effect of ϕ_{M2} on $|V_{ON}|$, as it is varied from 3.6 to 3.9 eV with a fixed value of ϕ_{M1} as 5.93 eV. As the work-function of M_2 decreases the effective work-function between the Si layer and drain electrode increases. This in turn leads to significant enhancement in the induced electron plasma at drain side. This increases the induced charge concentration leading to lowered V_{dj} drop and increased impact of applied $-V_D$ in channel region. Hence lower value of ϕ_{M2} leads to enhanced gate controllability and improved the value of $|V_{ON}|$. Further, the dielectric constant of gate oxide ϵ_r decides the effective gate coupling of the gate bias over channel. Higher the value of ϵ_r higher is gate coupling. Hence, $|V_{ON}|$ gets closer to gate biases as shown in Fig. 4c. Another crucial device parameter is L_{Gap}, its variation is depicted in Fig. 4. It can be inferred that lower value of L_{Gap} results in stable and higher value of $|V_{ON}|$, but L_{Gap} is limited by the process technology used. The general conclusion can be drawn that ϕ_{M1}, ϕ_{M2} and L_{Gap} are recognized as potential parameters to tailor its electrical performance.

4 Alternative operating mode and scalability of device

There are two alternative operating modes for Z^{2}FET, (i) back-gate operated and (ii) surface charge Q_S operated, as reported in literature [16]. In the later mode hole barrier is induced by the surface charge and electron barrier is still under the control of front gate. It ensures significant controllability of gate voltage on $|V_{ON}|$. DL-Z^{2}FET can also be operated in the surface charge Q_S mode as shown in Fig. 5a. To model these charges, we have considered point charges near silicon–SiO_2 interface with Q_s=10^{12} C/cm^2. The simulation parameters for Q_s operated DL-Z^{2}FET are: thickness of silicon film (T_{Si}) is 20 nm, gate oxide thickness (T_{ox}) is 2 nm, gate length (L_G), intrinsic channel length (L_{ch}), and box thickness (T_{Box}) are 200, 200, and 140 nm respectively.

Further to enhance the scalability of Z^{2}FET its structural variant with non-overlapping gates is already reported [16], further a local grounded plane (GP) in the LIN region only is also reported that can be realized by envisaging either a planar double-gate process [40]. To validate this scalability for DL-Z^{2}FET its non-overlapping gate architecture is also investigated here as demonstrated in Fig. 5b. One crucial advantage of DL-Z^{2}FET based structure is that it can mitigate the need of two independent gate biases. Apart from the two TM electrodes of Pt and Hf as source and drain electrodes respectively, another electrode of Hf can be used as back-gate electrode. It avoids the need of back-gate biasing, as the electrostatic doping due to work-function difference between Hf electrode (instead of back-gate) and silicon film induces virtual n-region just adjacent to the p^+ type source. It actuates the hole barrier exactly similar to the back-gate bias or Q_S induced hole barrier. Thereby leading to three terminal device operation for single gate operated DL-Z^{2}FET instead of the four terminal device as Z^{2}FET. Further, it also avoids the complicated chemical vapor deposition (CVD) method to realize the Q_S mode of operation. The schematics of the proposed novel three-terminal device structure for single gate operated p-type DL-Z^{2}FET is delineated in Fig. 5c. The simulation parameters for scaled un-overlapped gate DL-Z^{2}FET and single gate operated DL-Z^{2}FET are: thickness of silicon film (T_{Si}) is 5 nm, gate oxide thickness (T_{ox}) is 1 nm, gate

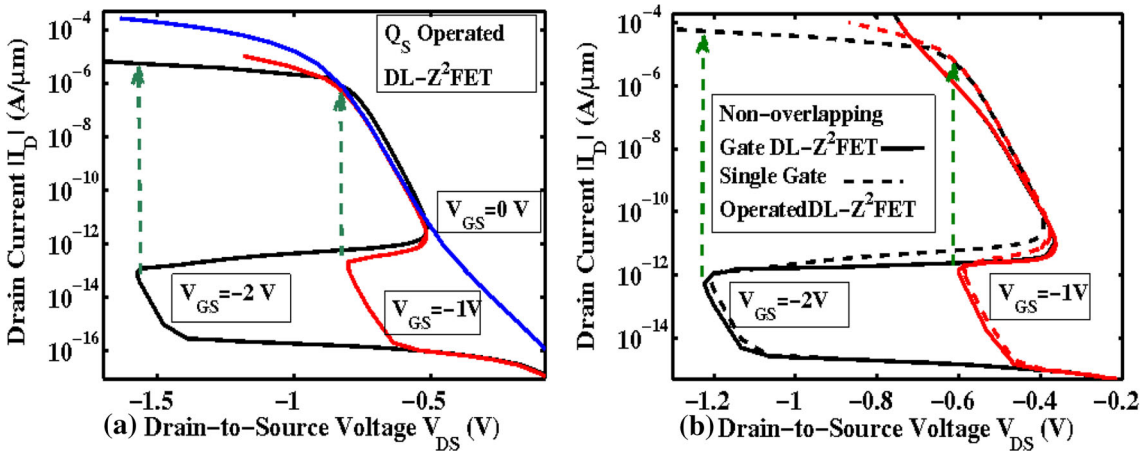

Fig. 6 **a** I_D-V_D characteristics of Q_S operated DL-Z^2FET and **b** $I_D - V_D$ curve of non-overlapped gate DL-Z^2FET and single gate operated DL-Z^2FET. For non-overlapped gate DL-Z^2FET V_{BG} = 2 V whereas there is no need to bias back gate for single gate operated DL-Z^2FET configuration

length (L_G), intrinsic channel length (L_{ch}), and box thickness (T_{Box}) are 50, 50, and 3 nm respectively. It is to be noticed that for Hf electrode to induce n-region efficiently (in place of back-gate), the thickness of box must be scaled.

Figure 6a plots the $I_D - V_{DS}$ curve of surface charge (Q_S) operated DL-Z^2FET. It depicts the similar gate controlled hysteretic behavior as it was for the case of V_{BG} operated DL-Z^2FET. TCAD simulation results indicate less gate bias control over $|V_{ON}|$, as for charge operated DL-Z^2FET $|V_{ON}|$ is less than the DL-Z^2FET for the same gate biases and comparable device dimensions. This less gate controllability for Q_s operated DL-Z^2FET results in detrimental effects at scaled down dimensions. Hence, Q_s operated DL-Z^2FET are not preferable for scaled DL-Z^2FET operations but this configuration can be used for charge sensing applications. In order to resolve this limitation and explore the device scalability, non-overlapping gate DL-Z^2FET is also investigated. Further, using the induced charge plasma for back gate as well, single gate operated DL-Z^2FET is realized. It avoids the need for back gate bias without hindering the device scalability. Figure 6b depicts $I_D - V_{DS}$ curve of non-overlapping gate DL-Z^2FET (solid line) and DL-Z^2FET (dashed line). Both the devices considered show approximately analogous $I_D - V_{DS}$ behavior. It is to be noticed that although gate controllability decreases at scaled dimensions but drive current seems immune to scaling effects. These structural variants point towards the probable scalability of DL-Z^2FET.

5 Conclusion

In this paper, we have demonstrated a novel approach to envisage the transition metal (TM) electrodes to realize DL-Z^2FET. It deploys the work-function difference between the TM electrodes and undoped silicon film to induce p^+ and n^+ regions in the film. The significant contribution of the proposed structure is its simplified fabrication process as ion-implantation and thermal annealing are no more required. It offers high immunity against process variations and there is no mobility degradation issues related to high doping. This also reduces the thermal budget, it facilitates its fabrication even on single crystal silicon-on-glass substrate by wafer scale epitaxy transfer. This results in its potential bio and opto compatible applications as well. Sensitivity analysis of the device reveals that work-function of M_1/M_2 and L_{Gap} are potential parameters to further tailor the device performance. Moreover, surface charge Q_s operated, non-overlapping and single gate operated DL-Z^2FET are also analyzed to explore the scalability of the device. DL-Z^2FET can be a potential candidate to macadamize the way to next generation steep switching transistors that can be employed for capacitorless 1T-DRAM/SRAM memory and electrostatic discharge protections as well.

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Appendix

Conduction mechanism of DL-Z^2FET

The conduction mechanism for DL-Z^2FET involves positive feedback between gate controlled carrier injection barrier and carrier flow is shown in Fig. 7. Under OFF state, front gate is negatively biased and back gate is positively biased ($V_G = -2$ V and $V_{BG} = 2$ V). These biases emulate p–n–p–n structure without any channel doping. Front gate bias generates electron barrier (V_n) and the back gate bias creates

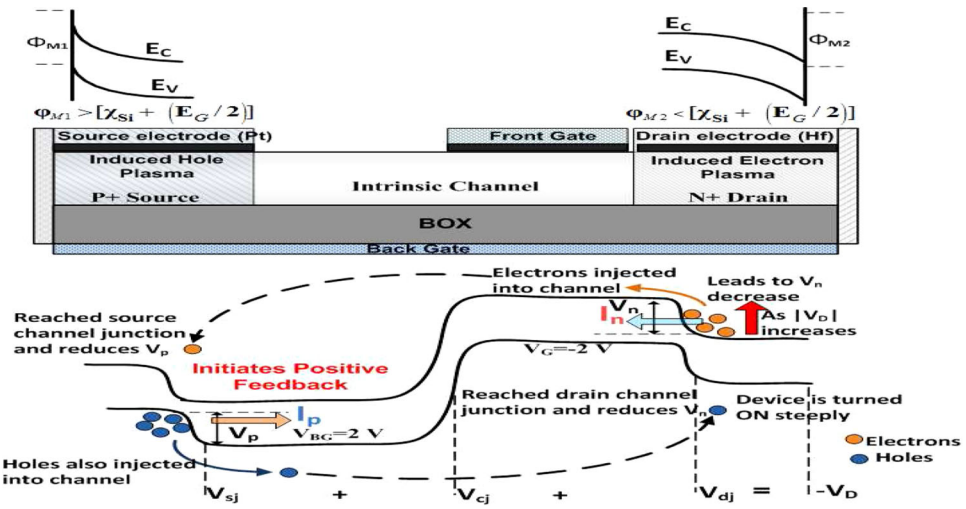

Fig. 7 Demonstration of positive feedback between injection barrier and carriers flow in DL-Z^{2}FET

hole barrier (V_p), thereby blocking the carrier flow in OFF state. When a negative bias is applied at drain, it forward biases the channel drain interface. This reduces the electron injection barrier at the drain channel side and initiates electron injection from drain to channel. As injected electrons reach source side, it reduces potential at the source channel interface. As a result, hole injection barrier reduces resulting in hole injection from source into the channel. This triggers the positive feedback between charge carriers flow and gate controlled injection barriers. It leads to high drive current as the device gets ON. To quantify this positive feedback it can be modeled as three virtual junctions realized by physical doping/electrostatic doping and applied biases at the gate electrodes. Hence, the applied forward bias at drain ($-V_D$) drops at these junctions, namely potential drop across drain channel junction (V_{dj}), source channel junction (V_{sj}) and virtual junction in the channel itself (V_{cj}). The electron diffusion current (I_n) is governed by V_{dj}. As this current reaches source side, it tailors V_{sj} and in turn V_{sj} induces hole diffusion current (I_p). I_n and I_p per unit gate width can be written by using MOS subthreshold model as [16]:

$$I_n = \frac{qn_i D_n T_{Si}}{L_G} \exp\left(\frac{V_{biG}}{V_T}\right)\left[\exp\left(\frac{V_{dj}}{V_T}\right) - \exp\left(\frac{-V_{cj}}{V_T}\right)\right] \quad (1)$$

$$I_p = \frac{qn_i D_p T_{Si}}{L_{in}} \exp\left(\frac{V_{biBG}}{V_T}\right)\left[\exp\left(\frac{V_{sj}}{V_T}\right) - \exp\left(\frac{-V_{cj}}{V_T}\right)\right] \quad (2)$$

where, V_T is the thermal voltage, n_i represents intrinsic carrier and $D_{n/p}$ are the electron/hole diffusion coefficients. Further V_{biG} and V_{biBG} models the built-in potentials offered during front gate and back gate bias respectively. If the currents in Eqs. (1) and (2) are given, junction drops V_{dj} and V_{sj} can be modeled using basic diode equations as

$$V_{dj} = V_T \ln\left(\frac{I_p - I_{Rd}}{I_{Sd}} + 1\right) \quad \text{and}$$

$$V_{sj} = V_T \ln\left(\frac{I_n - I_{Rs}}{I_{Ss}} + 1\right) \quad (3)$$

Recombination currents I_{Rd} and I_{Rs} and saturation currents I_{Sd} and I_{Ss} can be approximated as [16]. The perusal of Eqs. (1), (2) and (3) reveals the positive feedback mechanism. I_n is governed by V_{dj} and V_{dj} is I_p dependent. Similarly V_{sj} decides I_p and it is I_n dependent. Further, it is worth mentioning that although the current gating mechanism is still governed by the diffusion but positive feedback effect predominates and steep transition is achieved. For DL-Z^{2}FET the basic modeling equation would be same as there is dominant effect of virtual doping realized in the channel region due to applied gate biases. Whereas, the impact of source and drain doping is not very evident in the analytical framework. Moreover, within Debye length the variation of concentration of charge carriers due to charge plasma along the vertical direction can be approximated as constant profile [23].

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