سلام برای کد ISE پیوست به دنبال این هستم که دو شکل زیر استخراج شود. در شکل اول عملگرهای جمع و ضرب و جمع و منها و shiftو... مورد استفاده در کد نمایش داده میشوند. در شکل دوم submodule ها نمایش داده میشوند. برای رسم این دو شکل چنان چه روی کاغذ هم کشیده شود مسئله این نیست.

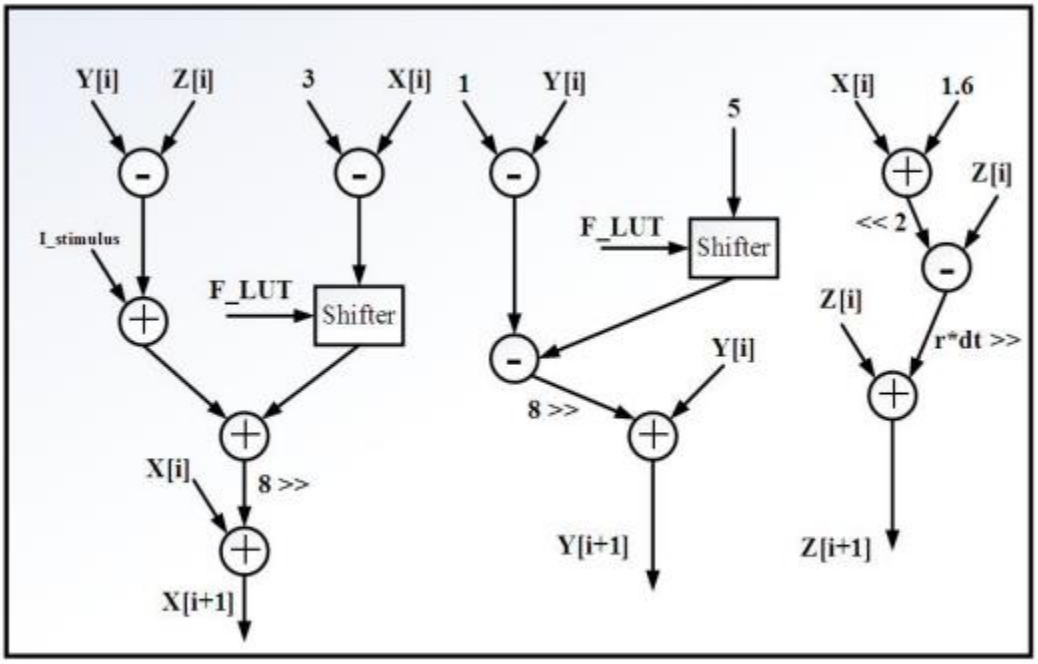

Fig. 7. Scheduling diagrams for the proposed model variables.

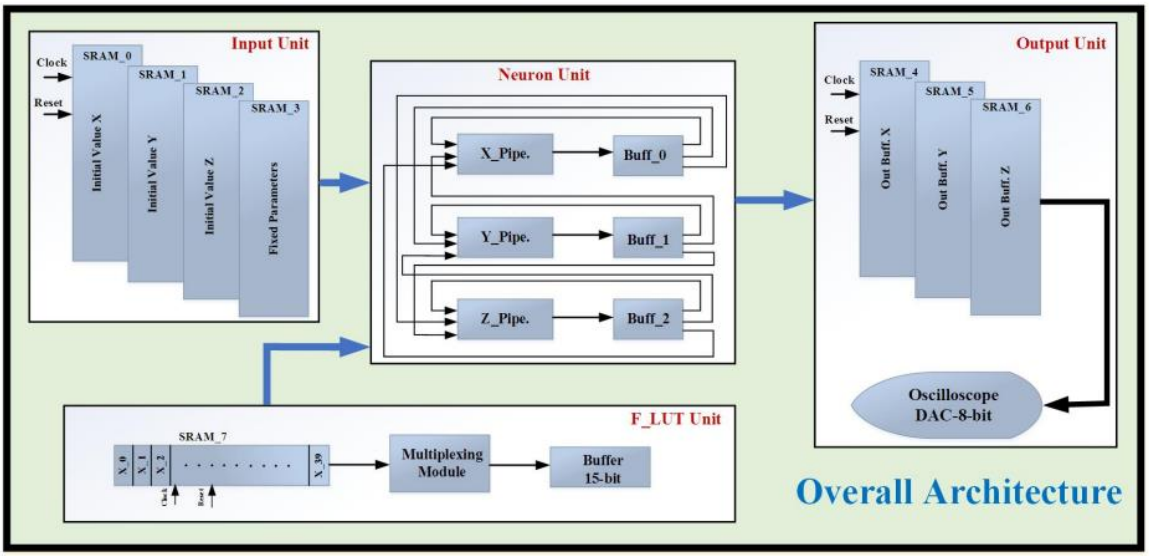

Fig. 8. The overall architecture for the proposed N-LUT-HR neuronal model.

E. Architecture View

Based on the proposed N-LUT-HR equations, the overall architecture can be presented. As can be seen in previous sections, the proposed neuron model is a multiplierless model with low-error levels with the original one. On the other hand, in this model, only adders, subtractors, and shifters have been used to realize the final system. The overall structure is depicted in Fig. 8. As can be illustrated, this overall module is made of some submodule that can generate the final signals. At first, the Input Unit is applied to create the required initial values and fixed parameters. For implementing this submodule, some SRAMs have been considered. If the Clock pulse is rised, the pointer is increased and the final value of the proposed function is extracted from this unit and transferred to the pipelining unit. Also, to implement the Neuron Unit, we have used the pipelining approach to accelerate the output signal production. in this way, for all variables, one buffer has been considered to store the objective output values, X, Y, and Z. On the other hand, the basic values of the nonlinear term that is modified by LUT approach, can be applied to the pipelining unit. In this state, F_{LUT} unit considered to create the required values and then, transfers these values to the pipelining submodule. Finally, objective signals extracted from pipelining unit and applied to the Output Unit for representing signals on oscilloscope device (with 8-bit DAC).