Z-Source Circuit breaker design and protection schemes for DC micro grid systems

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by
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Abstract

The work presented in this thesis includes recent developments and designs for the novel Z-source dc breaker as well as its application in dc micro grids since it was first proposed for use in dc circuits. The novelty of this work is that the initial Z-source breaker design has been modified and tested extensively in simulation and hardware to provide a more practical solution for dc protection. The first part of this work addresses the design of the breakers and the unique advantages offered by the variations in designs. The second part is focused on protection schemes for multi-breaker systems and using sensor and communication tools to ensure system-wide protection using Z-source breakers. Most of this work has been developed with funding from office of Naval research and is tested primarily for systems replicating an all electric shipboard power system. The results from simulation of large systems and protection schemes are presented in great detail. Laboratory testing for several Z-source breaker designs and multi-breaker systems with a central control is also presented and discussed.

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Chapter 1

Introduction

1.1 Dc protection: problem and solutions

Design innovations have furthered the use of dc power in ship systems, in particular medium-voltage dc systems [1]-[3]. Protection devices for dc systems are limited, since dc fault current does not produce a natural zero crossing as it does with ac systems [4]-[6]. Normally, in dc systems, the interruption of current by mechanical contacts produces an arc which is sustained by the system inductance, preventing the system from turning OFF under a fault condition [7]-[9].

Future Naval ship power systems will be based on an MVDC architecture [10]-[12]. Benefits of the MVDC system include fewer power conversion steps (i.e., improved power density) and overall higher efficiency [13]-[14]. However, circuit breakers for MVDC systems are in the experimental stage [15]-[20]. Many dc microgrid systems require rapid reconfiguration for survivability. This has led to research into advanced dc circuit breakers. One popular choice is the hybrid dc breaker, which uses a mechanical switch in parallel with a path containing semiconductor devices. When the mechanical switch is opened, the current is diverted to the semiconductor, which is then opened. The current is ultimately diverted to a metaloxide varistor, which clamps the voltage and allows system inductance to reduce the current. A main advantage of this type of breaker is its low on-state power losses.

Some other breaker-based protection strategies include using high blocking voltage solid-state switches, such as insulated-gate bipolar transistors or gate turn-off thyristors, controlled by a fault detecting algorithm [21]-[26]. A surgeless solid-state dc breaker discussed in [24] employs a semiconductor device to conduct during normal operation. During a short-circuit fault, the current increase is detected and the semiconductor is immediately switched OFF. The circuit design provides a path for fault current to commutate through a free-wheeling diode. The self-powered dc solid-state breaker discussed in [25] uses SiC junction field-effect transistors (JFETs) as the main static switch. The unique fault detection and gate control mechanism presented in [25] does not require any auxiliary power source and monitors voltage across the JFET device to detect a fault. An optimized version of bidirectional solid state dc breaker has been recently developed by ABB and is presented in [26]. This breaker employs reverse blocking IGCTs as switches and has surge arrestors in parallel to the conducting path to allow commutation of current once the semiconductors are switched OFF. It has also been suggested to use breakers in a breakerless control as a secondary protection.

It is safe to say that the MVDC system architecture and protection in electric ships is an emerging topic of research and considerable work is being carried out in this area [27]-[31]. The majority of the protection schemes can be classified as using either the breaker or breakerless approach [32]. All examples discussed above are of breaker based protection schemes. The breakerless approach has fault detection methods embedded in the power converter feeding the load [33]-[35]. The most basic fault detection is the overcurrent limit set on the converter. Impedance measurement is also used to define trip conditions. The advantage offered by breakerless distribution is higher power density. In the case of a fault in a breakerless system, the converters will detect the fault and stop feeding the load, allowing mechanical contacts to open and isolate the affected zones. For higher survivability, breaker-based architectures are preferred.

1.2 Z-source breaker: Principle of operation

The z-source inverter, as introduced by *F.Z. Peng*, could interface to a voltage or current source and utilize the short-circuit state to achieve a voltage boost. This new topology has led to a considerable amount of research demonstrating variations and improvements to the circuit. Later, the z-source circuit found application in dc circuit breakers. A form of solid-state breaker, the z-source dc breaker rapidly and automatically responds to faults.

Z-source breakers can be installed in the breaker-based architecture. The additional advantage offered by these breakers compared with other dc breaker solutions is autonomous instantaneous isolation of the load from the fault. Several designs for Z-source breakers have been introduced and will be discussed in the second section of this thesis. The most recent design and the one used in the laboratory setup at the Clemson Micro Grid and Power Electronics Lab is shown in Figure 1.1. To close the Z-source breaker, a gate signal is applied to the SCR until the capacitors are charged up to the source voltage and a steady dc current is flowing through the inductors. Once steady-state operation is achieved, the gate signal from the SCR must be removed. Now the breaker is armed and ready to operate in the case of a fault. A short-circuit fault at the output of the breaker will cause the capacitors in the breaker to discharge instantly while the inductor current remains constant. The path of this discharge current is shown in red in Figure 1.2. This will force the SCR current to go to zero.

1.3 MVDC system architecture and protection schemes

The work in this thesis explores the use of a solid-state Z-source breaker in a notional ship power system. The system is defined in Figure 1.3 and the breaker design is discussed in later sections. The focus of this work is on finding practical control algorithms which can be handily implemented without requiring many design changes in the z-source breaker itself.

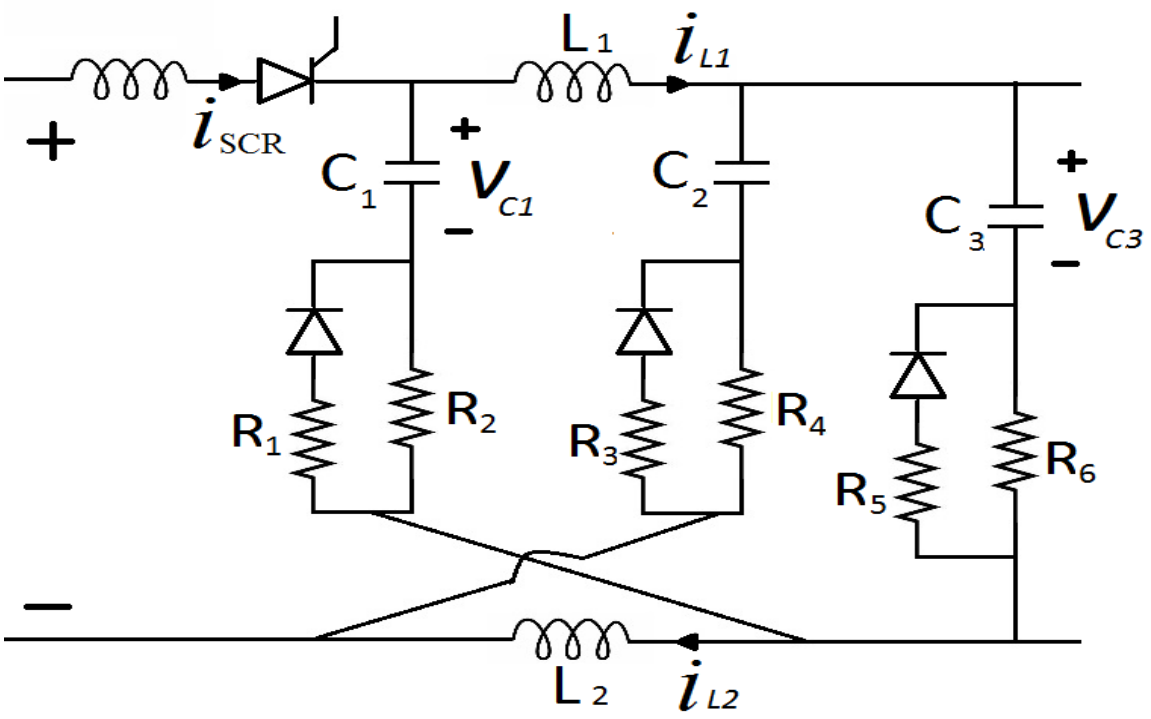

Figure 1.1: Most recent Z-source dc breaker design

The ring architecture provides more flexibility to a MVDC system compared to a star connected architecture. Its value lies in providing continuous power to the load even if there is a fault in one of the lines, or if one section has to be tagged out and isolated for maintenance purposes.

For the system shown in Figure 1.3 two sources supply three loads through a ring type network which is chosen for redundancy and survivability. In this system the Z-source breakers are installed at locations A through K and communicate to a higher-level control unit which makes decisions on which breakers receive gate commands at which time. The locations 1 through 11 depict where faults will be applied. Using this multi-breaker ring distribution system, a protection scheme is simulated and presented in this work. The goal of the scheme is to identify and consequently isolate the faulty zone through communication among multiple breakers.

The simulations for the protection scheme is carried out on the system of Figure 1.3 however for laboratory set up a simplified version of a zonal ship power system is

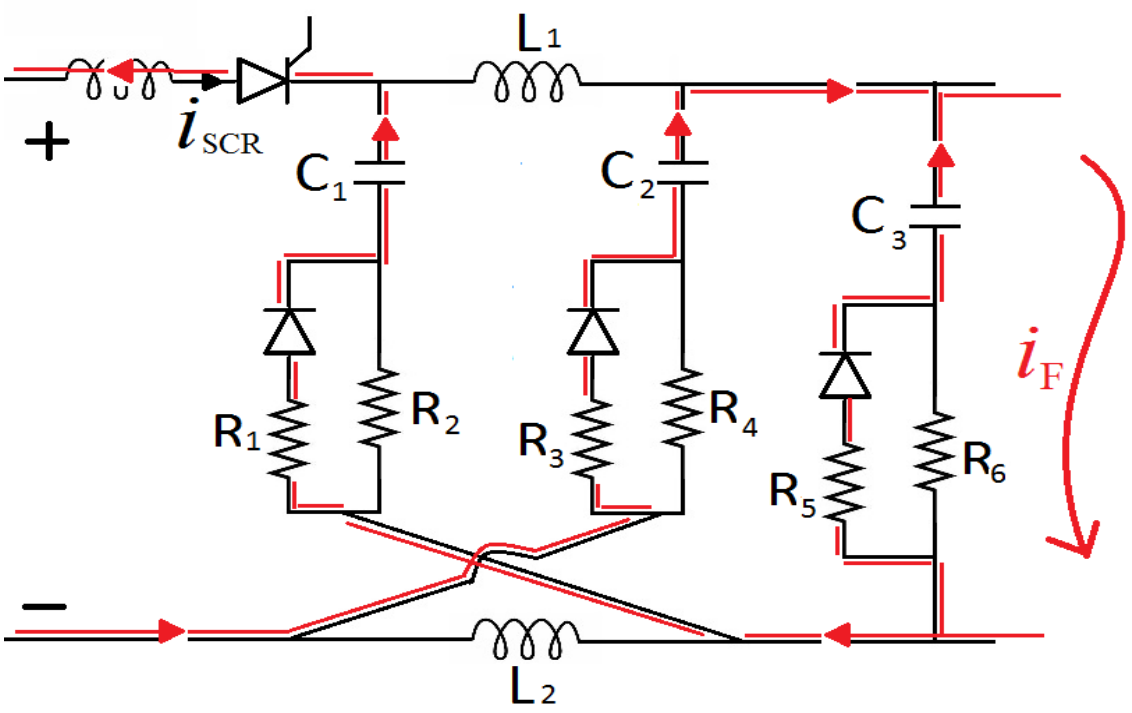

Figure 1.2: Capacitor discharge path during a fault

considered as shown in Figure 1.4. The load centers contain inverters supplying low-voltage ac loads. Each load center is supplied from medium-voltage dc (MVDC) buses on the port and starboard side through nonisolated dc/dc converters. Port and starboard are the nautical terms for left and right sides of the ship, respectively. The most important feature of this architecture is redundancy. Each load center or zone has access to two paths for obtaining power. This leads to higher reliability in the case of a fault or maintenance procedure where the load can still obtain power with some part of the system being offline. This work considers the problem of introducing a Z-source breaker in such a system while retaining this feature of redundancy.

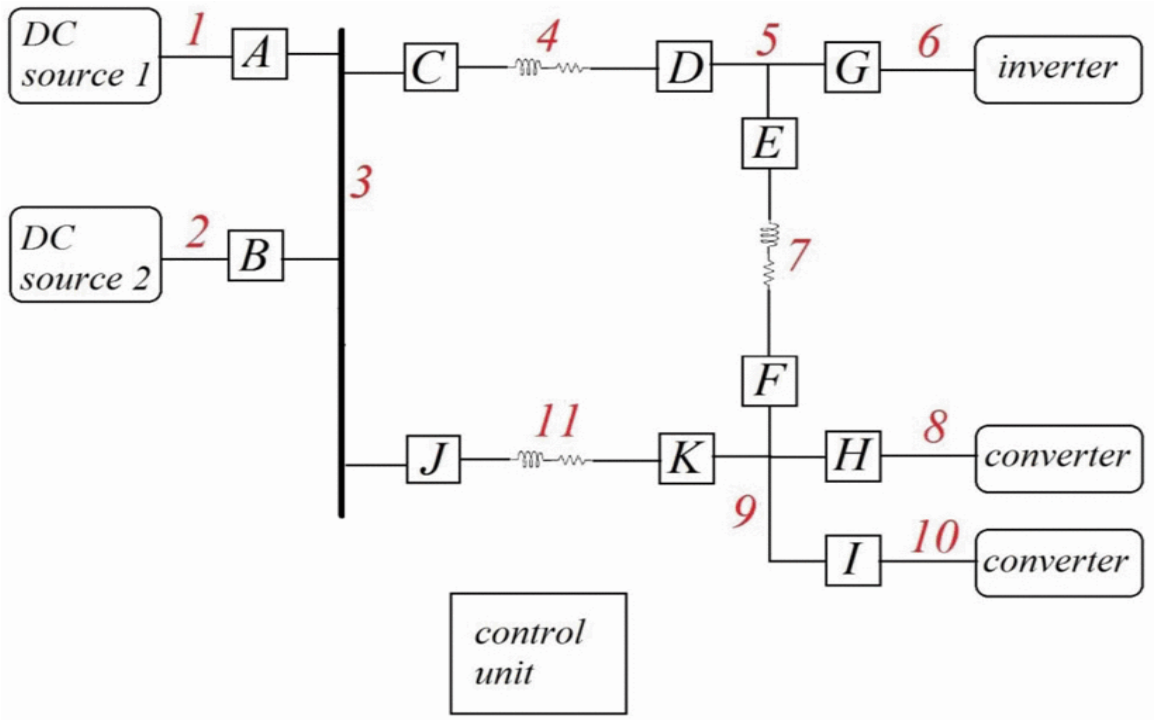

Figure 1.3: Ring-connected MVDC power system

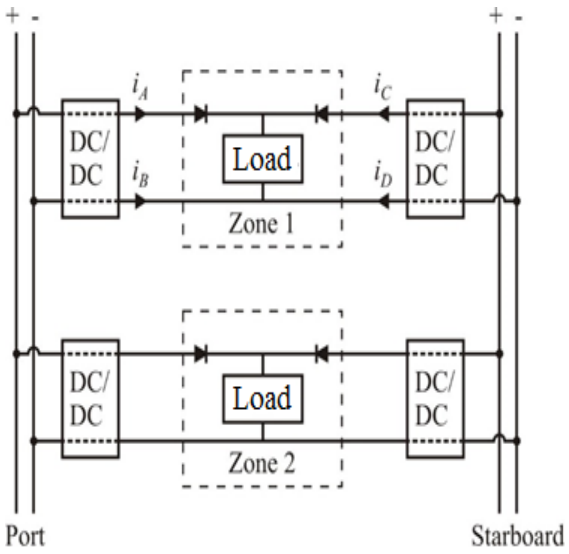

Figure 1.4: Example of a Zonal ship power system

Chapter 2

Z-source breaker designs

2.1 Original designs

Previous Z-source breaker designs include the classical Z-source breaker design and the series connected Zsource breaker design; shown in Figures 2.1 and 2.2, respectively. These breakers are quite different in design. The classical design provides isolation from the fault to the source through the SCR; however, the frequency response of the classical Z-source breaker is undesirable as it resembles that of a band-pass filter which would allow harmonics from the dc supply to transfer to the load. Also, the classical design does not include a common path to ground through the breaker. This problem is mitigated in the series connected design. The series connected design differs from the classical Z-source design, in that it has a common path to ground but it carries the disadvantage of not providing isolation between input and output when the SCR is turned OFF. The transfer function of the series connected Z-source breaker is improved as it resembles a low-pass filter, giving it the ability to preserve a pure dc signal.

The breaker needs to have a gate signal for the SCR at the start of the operation. If the load is discontinuous then the gate signal must be provided every time the breaker current needs to increase from zero. This makes the gate control considerably more complex and increases the risk of a fault going undetected, so for this work only continuous resistive

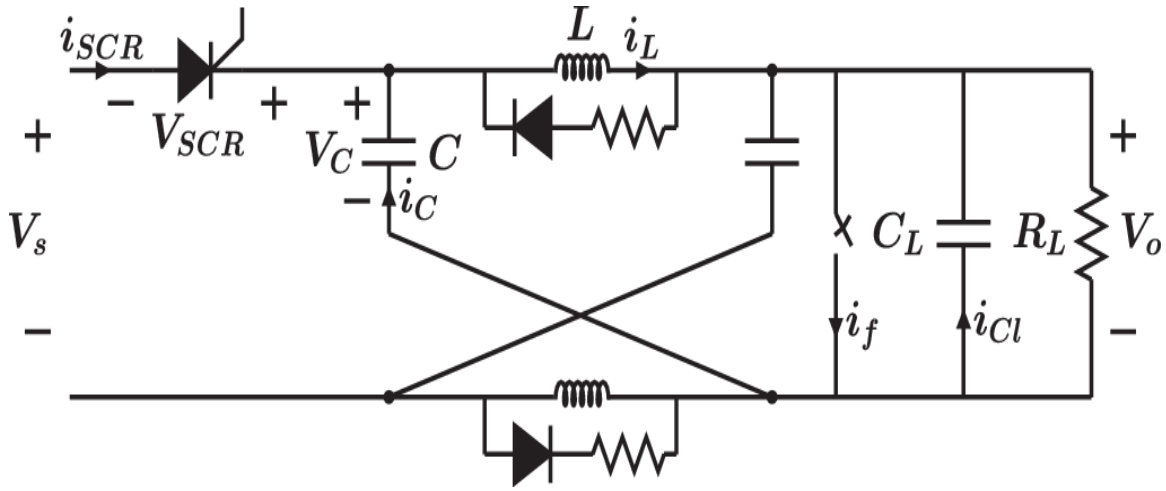

Figure 2.1: Classical Z-source breaker

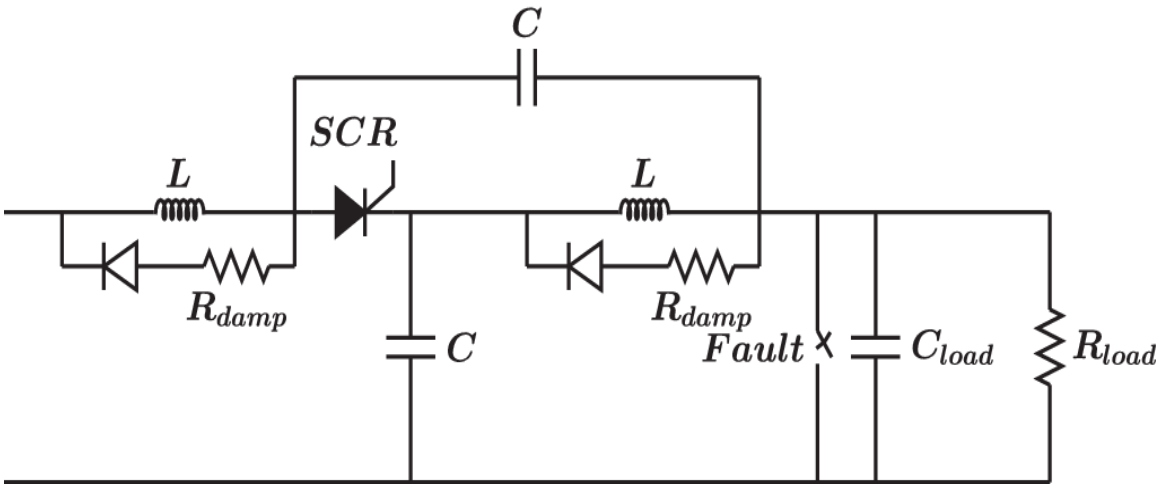

Figure 2.2: Series connected Z-source breaker

load will be discussed.

For a purely resistive load, neither of these designs will allow instantaneous increases in the load current greater than their steady-state current. Consider the circuit in Figure 2.1 without the output capacitor, i.e., i_{Cl} equal to zero in case of a step change. Any step increase in current must come through the breaker capacitors because inductor current cannot change instantaneously. Current balancing at the cathode of an SCR shows that if the capacitor current becomes greater or equal to the steady-state load current, it will push the SCR current to zero hence opening the breaker. If either of these breakers were to

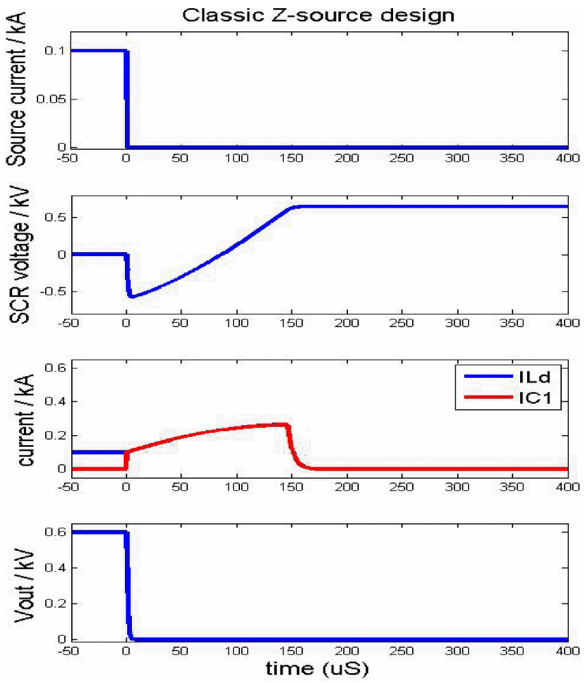

Figure 2.3: Fault response of a classic Z-source breaker

experience a step change in load greater than their steady-state current in the absence of the output dc capacitor, the breaker would turn OFF; effectively mistaking a change in load for a fault. If load capacitor is present then breaker capacitors can be designed to control exactly how much step change is to be allowed. This relationship between downstream capacitance and minimum fault resistance is analyzed extensively in previous works.

The operation of the breaker in response to a fault could best be understood through the simulation results shown in figures 2.3 and 2.4. In this simulation a dc source of 600V is used to supply 100A to a RC load through a z-source breaker. Both the original designs are used to provide a comparison of their characteristics. The parameters listed in table 2.1 are used for the breaker. At time t=0 a line to line fault is introduced across the load forcing a large transient current to flow and both breakers are successfully able to isolate the source from the fault by forcing SCR current to zero in a few micro seconds.

The only difference in the breaker operation visible from figures 2.3 and 2.4 is the source current. The classic design isolates the fault instantly whereas with the series

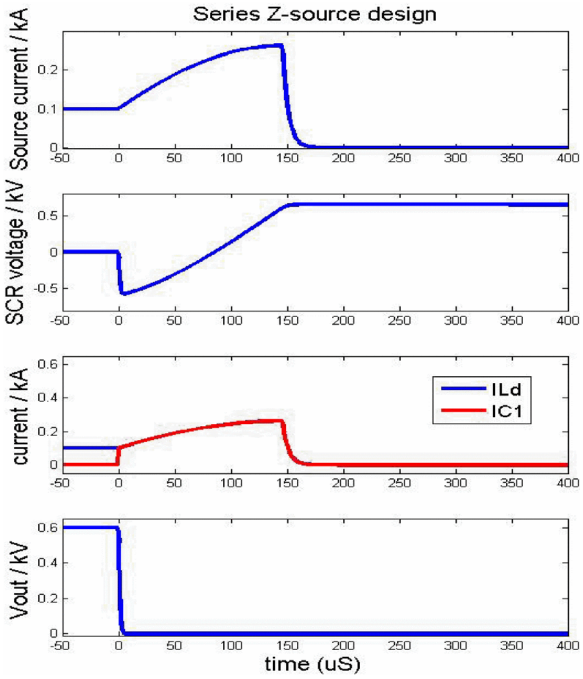

Figure 2.4: Fault response of a series Z-source breaker

Nominal Voltage	Nominal current	C	L	R_L
600V	100A	$50\mu F$	$300\mu H$	$6m\Omega$

Table 2.1: Z-Source breaker parameters

breaker there is resonance current coming through the source after the fault.

2.2 Novel DC Circuit Breakers

The basis for the new Z-source breaker designs is the addition of a capacitive current divider, which would allow two paths for current to flow during fault or load change conditions. The addition of the current divider within the breaker design allows for a change in current that is greater than the steady state current even without output capacitance. This change is dependent on the capacitor values. Analysis suggests that the capacitors would naturally be subject to a high amount of current during fault conditions, and therefore, methods were chosen to limit the amount fault current that is seen by the capacitors. The

first method, designated as design 1, utilizes resistors to limit the capacitor current. The second method, designated as design 2, utilizes inductors for current limiting. The next extension of this research also considers variations of the zsource dc breaker which utilize coupled inductors. Bidirectional breaker designs are also presented.

2.2.1 Design 1-Capacitor Current Divider With Resistive Current Limiting

The first modified design is shown in Figure 2.5. During steady state operation, the current will flow to the load through the inductors L_1 and L_2 . The first design consists of a capacitive current divider created by C_1 and C_2 which creates two current paths. One path consisting of C_2 and R_2 will allow current to flow through the SCR in the opposing conventional direction allowing the breaker to turn OFF in the event of a fault. The second path consisting of R_1 and C_1 allows current to flow through the capacitor C and to the load allowing a partial amount of transient current to flow into the load. The capacitance values for C_1 and C_2 will determine how high the transient current will be allowed to reach before the breaker considers the transient current as a fault. The resistors in series will limit the amount of transient current in the capacitors. The reliability of these components will need to be high, as the transient current will flow through them to remove the fault. The integration of these resistors allows for fault detection since the resistor voltage indicates the fault current. This property may be utilized for multiple breaker interoperability.

When the breaker is operating in steady state, the circuit can be simplified as shown in Figure 2.6 by considering the SCR as closed and ideal. The combination of R_1 and C_1 in series and in parallel with the series combination of R_2 and C_2 will be designated as the impedance Z_1. Further combining L_2 and C makes the impedance designated Z_2. The transfer function of the breaker is

$$H = \left(1 + \frac{sL_1(Z_1 + Z_2 + Z_{load})}{Z_1(Z_2 + Z_{load}}\right)^{-1} \left(\frac{Z_{load}}{Z_2 + Z_{load}}\right) \tag{2.1}$$

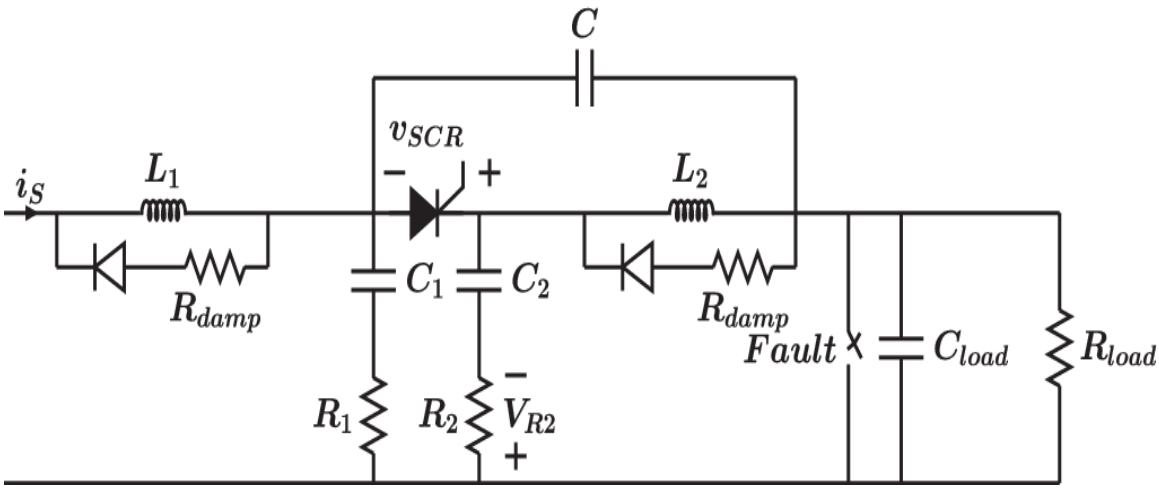

Figure 2.5: Modified Z-source breaker, design 1

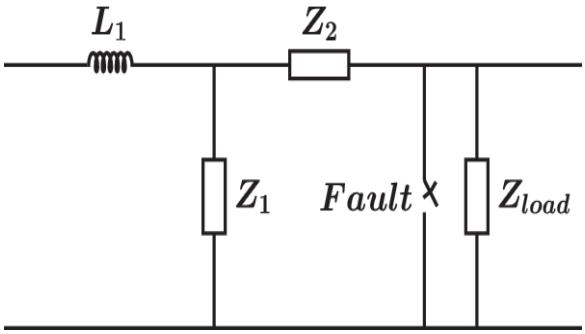

Figure 2.6: Design 1 simplified circuit

$$Z_1 = [[(sC_1)^{-1} + R_1]^{-1} + [(sC_2)^{-1} + R_2]^{-1}]^{-1} \tag{2.2}$$

$$Z_2 = [sC + (sL_2)^{-1}]^{-1} \tag{2.3}$$

$$Z_{load} = (sC_{load} + (R_{load})^{-1})^{-1} \tag{2.4}$$

The Bode plot of 2.1 is shown in Figure 2.7 for typical values of R, L, and C components. The values of components used are listed in Table 2.2.

The frequency response of the system appears to approximately match a low-pass

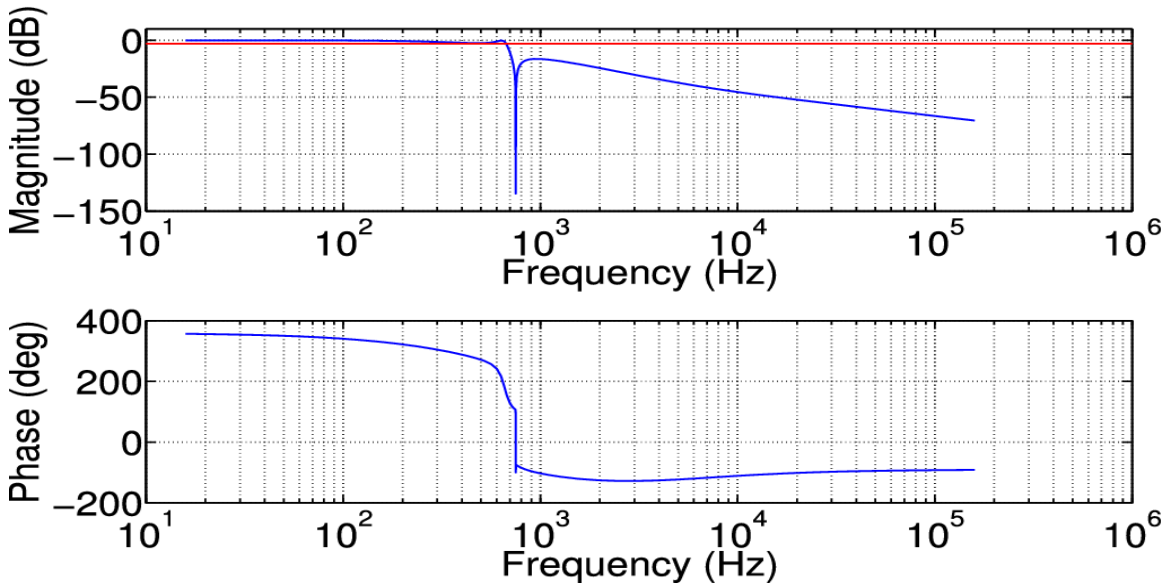

Figure 2.7: Bode plot for voltage transfer of design 1

$R_1(\Omega)$	$R_2(\Omega)$	$C_1(\mu F)$	$C_2(\mu F)$	$C(\mu F)$	$L_1(mH)$	$L_2(mH)$
1	1.5	30	20	50	1.8	0.9

Table 2.2: Component values for design 1 bode plot

filter with 3 dB cutoff frequency near 660 Hz and a notch at 750 Hz.

2.2.2 Design 2-Capacitor Current Divider With Inductive Current Limiting

The second design, shown in Figure 2.8, is similar in operation to the first design. This design utilizes two inductors instead of the resistors. The inductors in this design serve the same purpose; to limit the amount of transient current that is allowed to flow through the capacitors. Current flows through the capacitor branch only for transients, so in the case of design 1 shown in Figure 2.5 there will be some additional losses during that period only. For small resistors and loads with infrequent transients, these losses will not be appreciable, nevertheless design 2 has a brief advantage in this regard.

When the breaker is operating in steady state, it can be simplified from that shown

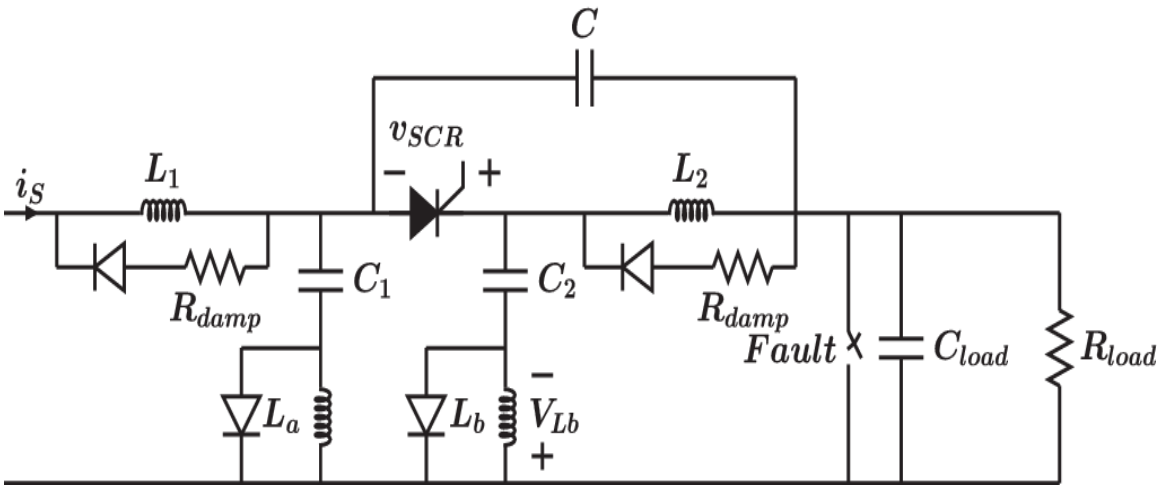

Figure 2.8: Modified Z-source Breaker, design 2

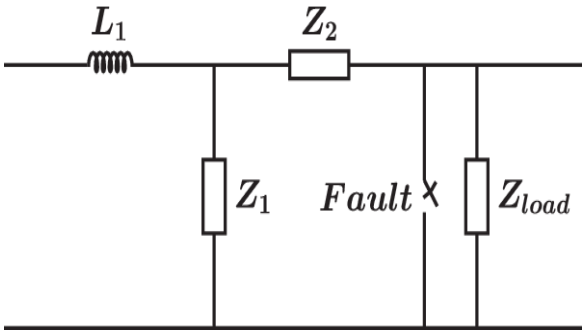

Figure 2.9: Design 2 simplified circuit

in Figure 2.8 to that shown in Figure 2.9.

The transfer function for design 2 can be expressed as

$$H = \left(1 + \frac{sL_1(Z_1 + Z_2 + Z_{load})}{Z_1(Z_2 + Z_{load}}\right)^{-1} \left(\frac{Z_{load}}{Z_2 + Z_{load}}\right) \tag{2.5}$$

$$Z_1 = [[(sC_1)^{-1} + sL_a]^{-1} + [(sC_2)^{-1} + sL_b]^{-1}]^{-1} \tag{2.6}$$

$$Z_2 = [sC + (sL_2)^{-1}]^{-1} \tag{2.7}$$

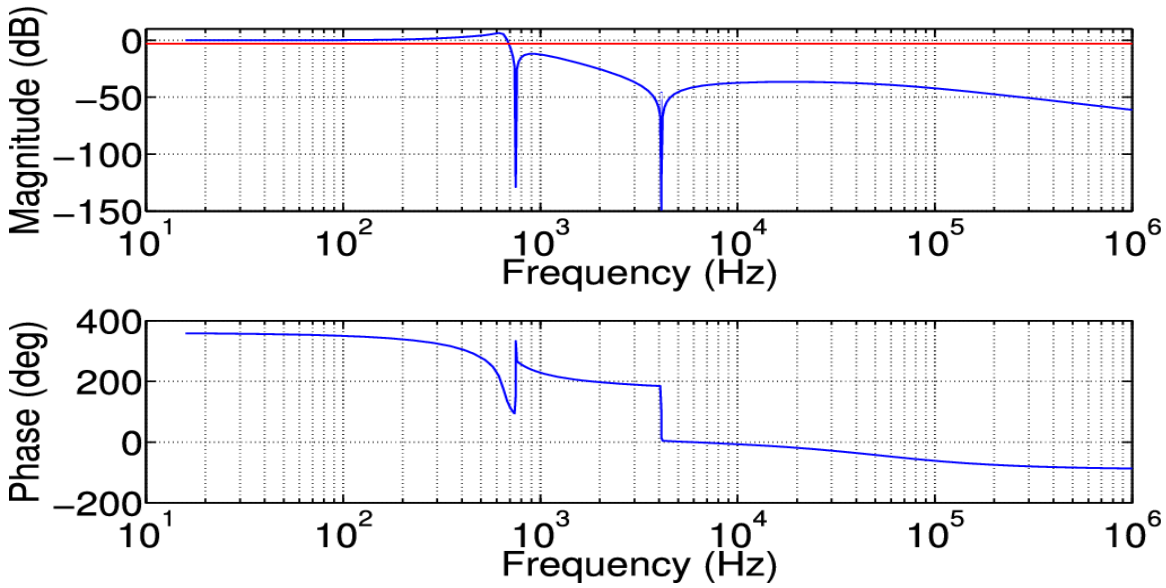

Figure 2.10: Bode plot for voltage transfer of design 2

$L_a(\mu H)$	$L_b(\mu H)$	$C_1(\mu F)$	$C_2(\mu F)$	$C(\mu F)$	$L_1(mH)$	$L_2(mH)$
50	75	30	20	50	1.8	0.9

Table 2.3: Component values for design 2 bode plot

$$Z_{load} = (sC_{load} + (R_{load})^{-1})^{-1} \tag{2.8}$$

The corresponding Bode plot of 2.5 is shown in Figure 2.10. Values of the components used are listed in Table 2.3. The transfer function of this design has a frequency response resembling a low-pass filter with 3 dB cutoff frequency of about 660 Hz. It also has notch at 750 Hz and 4.1 kHz.

The response of both the designs to a shunt fault is identical so either design can be used depending upon the availability of components. The transfer function differs slightly with the inductor design having an additional notch but both have the general properties of a low-pass filter.

Fault clearing ability of the breaker is defined as the maximum fault current that could be successfully interrupted. For ac breakers, it is the arc extinguishing technique that limits this ability. For the Z-source breaker, the limiting factor is the SCR specifications

such as maximum reverse blocking voltage and surge current tolerance. Comparing the original design in Figure 2.2 to new designs of Figures2.5 and 2.8, it can be seen that the maximum reverse blocking voltage in either case is equal to source voltage as there is only one SCR in conduction path. Also in neither of these designs will the SCR experience any surge current because the transients through the capacitors will always force to decrease SCR current as shown in the analysis in next section. Since, the fault is always large compared to step changes in load, it forces the SCR current to zero and the fault clearing ability for the new designs is the same as the original design.

Both designs 1 and 2 could allow the breaker to tolerate three or four times a step change in load by selecting appropriate impedance ratio for the shunt capacitor branches. The next section on design and analysis will focus on design 1 only; however, similar parameters can be used to select components for design 2 as well.

2.2.3 Coupled inductor Z-source breaker

Note from Figure 2.1 and 2.2 that during all modes of operation, steady state and transient, the currents in both inductors are identical. This key feature allows a factor of two improvement in effective inductance when comparing the two separate inductors to a coupled set of inductors that use the same number of turns. Another way to express this is that considering a design with a specific value of inductance, the number of turns can be reduced by nearly 30%. Considering that the coupled inductors can be wound on the same core, the inductor size can be reduced to 50% compared to the non-coupled case. This is significant for higher power designs; as the inductor has the largest volume and weight of all of the breaker components.

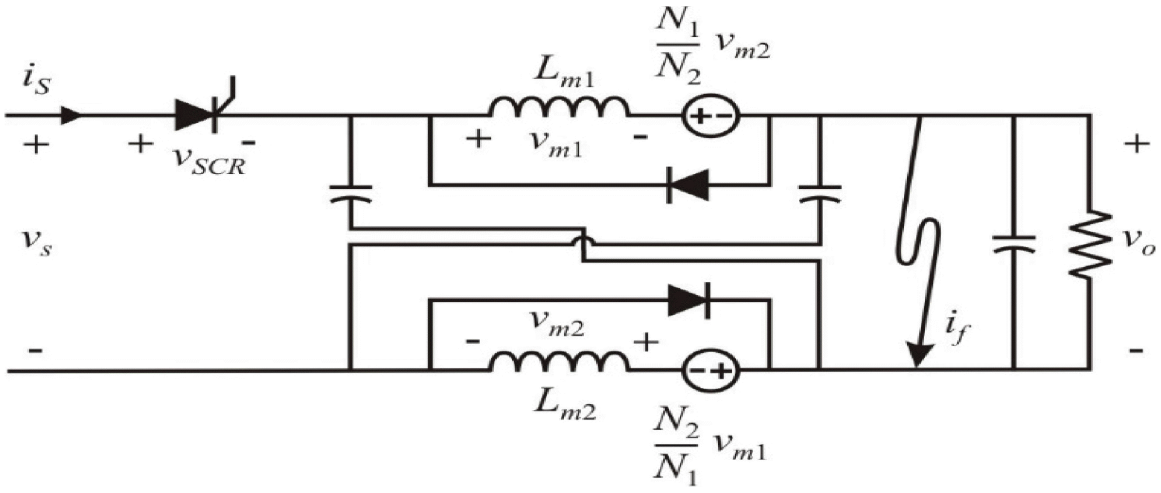

Figure 2.11: Equivalent circuit of the coupled-inductor classic z-source breaker

2.2.3.1 Equivalent circuits for Z-source breakers with coupled inductors

Figure 2.11 shows the equivalent circuit of the classic z-source breaker wherein coupled inductors have been used. In this special case, the turns ratio is set to unity. Furthermore, due to symmetry, the current in each inductor is the same. Therefore, $v_{m1} = v_{m2}$ and the coupled term is identical to the mutual inductance term. This means that the inductance value can be cut in half compared to the case where the inductors are not coupled. When constructing the breaker, only 70.7% of the number of turns are required to make the inductance half of the previous case. Figure 2.12 shows the equivalent circuit for the series breaker with coupled inductors.

2.2.3.2 Sizing of the new designs

With mobile applications of dc systems such as naval ships, hybrid vehicles and aircraft there is an increasing trend towards making the systems compact and more power dense. This is evident by the growing interest in Silicon Carbide devices to replace all current power electronic applications. With this in mind a significant reduction in breaker size could be considered very important towards making it a more practical solution for dc

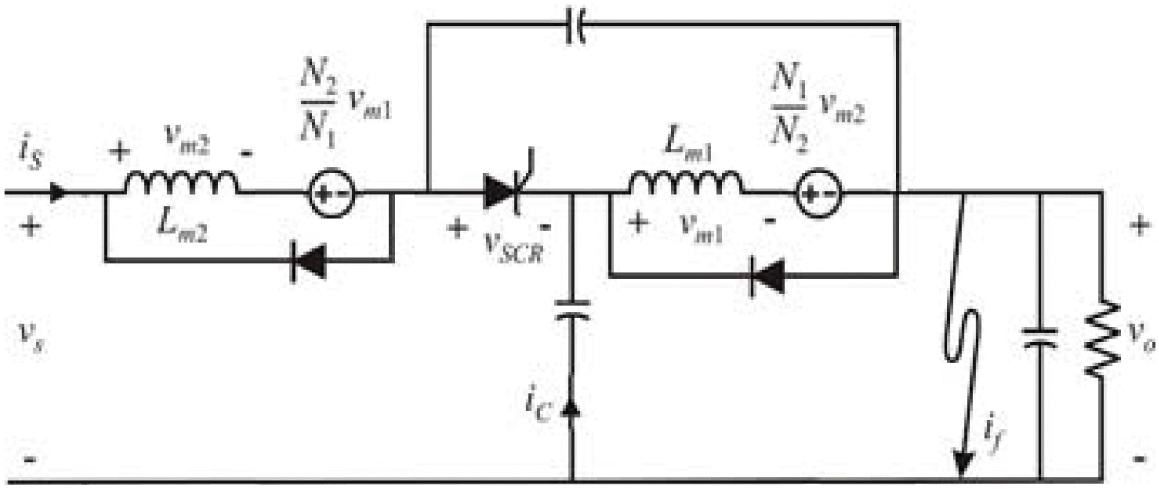

Figure 2.12: Equivalent circuit of the coupled-inductor series z-source breaker

Z-source breaker	Coupled Z-source breaker
$L = 300\mu H$	$L_m = 150\mu H$
$r_L = 6m\Omega$	$r_m = 4.5m\Omega$
$C = 50\mu F$	$C = 50\mu F$
$Mass = 16.6kg$	$Mass = 11.7kg$
$Volume = 43.3ltr$	$Volume = 32.1ltr$

Table 2.4: Z-source breaker sizing results

system protection.

To see the effect of coupled inductors on breaker size consider a case study for designing a 60KW, 600V z-source breaker. Since both the classic and series design use the same amount of material no distinction is made while calculating the size. The detailed steps of calculation are provided in appendix A and the results can be seen in Table 2.4.

In this case it can be seen that the weight of the coupled breaker will be reduced by 30%. Also, the volume is reduced by 26%. These are significant reductions in size and weight for mobile applications such as Naval ships, hybrid vehicles, aircraft, etc.

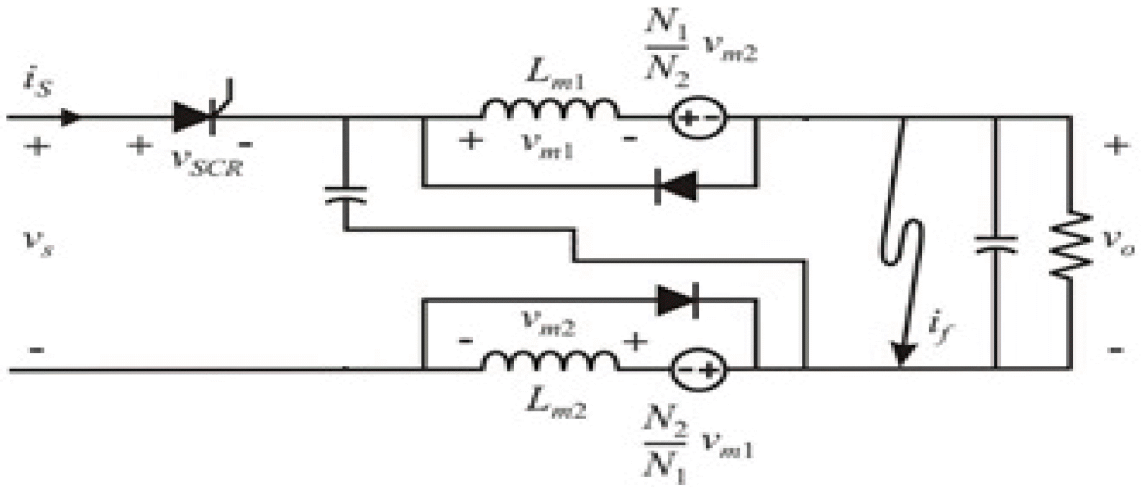

Figure 2.13: Coupled-inductor classic z-source breaker with reduced capacitance

2.2.3.3 Coupled inductor Z-source breakers with reduced capacitance

Another aspect of having coupled inductors is that the coupling can the used for the circuit breaker opening. Therefore, either one of the capacitors can be removed as shown in figures 2.13 and 2.14. Two capacitors are used in the original z-source breaker designs in order to complete the loop for transient currents through capacitors. While using the new design there is an instantaneous change of voltage across the inductors due to fault. That can be reflected in instantaneous change in current through both inductors due to their mutual inductance hence eliminating the need of a return path through additional capacitor. Furthermore removing one capacitor also decreases the mass and volume of the breaker.

2.2.3.4 Simulation results for coupled inductors

In order to validate the designs introduced in this paper a simulation is carried out with same parameters as the simulation for original designs using Table 2.1. Dc source voltage of 600V is supplying 100A to a RC load through a z-source breaker when the fault is introduced. Figure 2.15 show the result for design of figure 2.12.

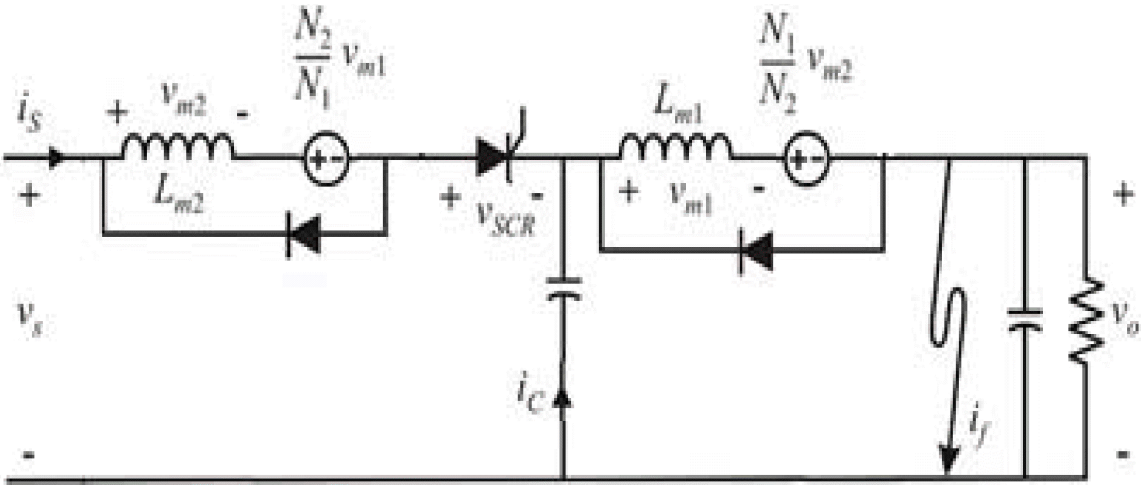

Figure 2.14: Coupled-inductor series z-source breaker with reduced capacitance

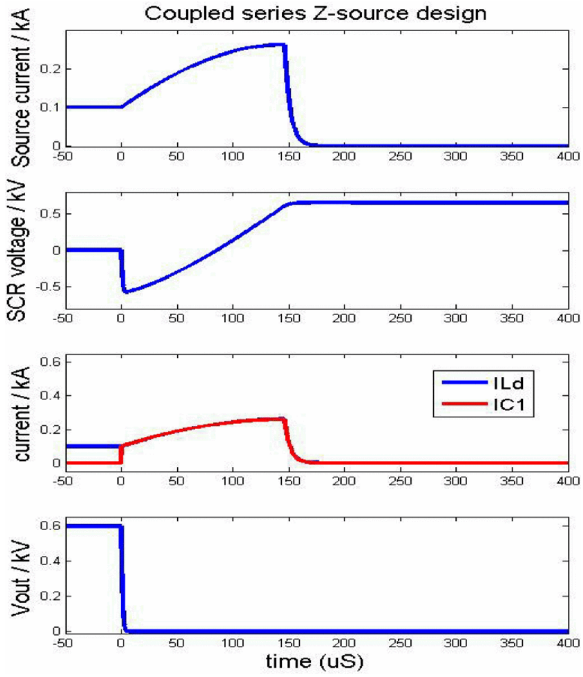

Figure 2.15: Fault response of a coupled series Z-source breaker

The fault response in figure 2.15 is identical to the response of the breakers without coupling inductors in figur 2.4 hence confirming the operation of the new design.

With the same system parameters, the new designs of figure 2.14 is tested and its response is shown in figure 2.16. Comparing figure 2.16 to figure 2.15 shows the only differ-

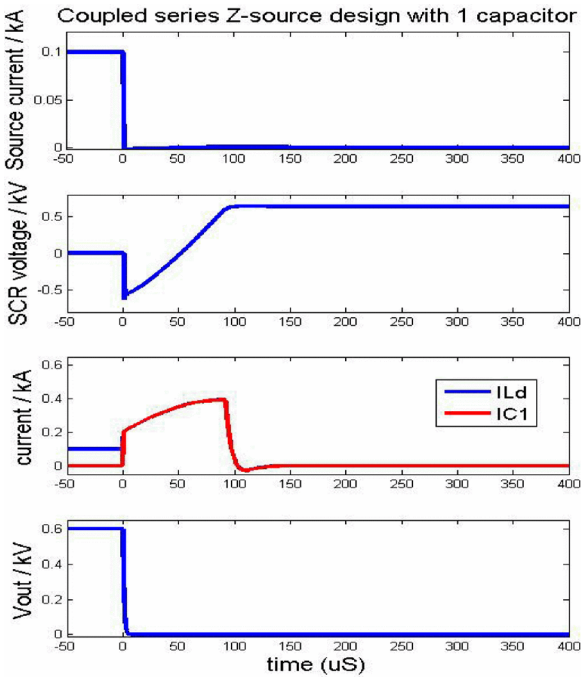

Figure 2.16: Fault response of a coupled series Z-source breaker with reduced capacitance

ence is that the load end inductor current is increasing instantaneously with the capacitor current which is only possible due to the coupling effect. This has the drawback of reducing the reverse bias resonance time for SCR voltage.

One major advantage of removing the additional capacitor in this case is that the source current goes to zero instantly instead of shooting up as the source current is in series with the SCR current. Importantly both the designs with reduced capacitance are also able to isolate the fault like the original designs.

2.2.4 Bidirectional breaker designs

In applications with a single source and load the direction of power flow may be fixed so the breaker, as shown in Figure 2.5, would be adequate. In complex power system architectures, the direction of power flow through the lines may vary depending on the load distribution. Also there may be elements within the system which may receive from as

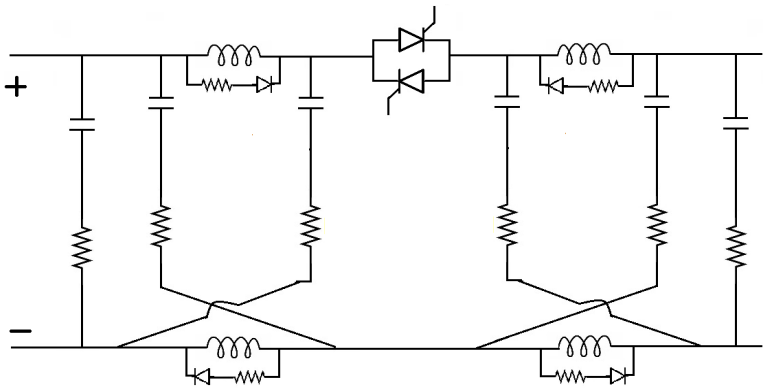

Figure 2.17: Bidirectional Z-source breaker, option 1

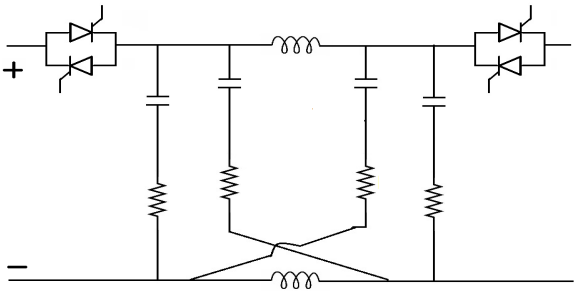

Figure 2.18: Bidirectional Z-source breaker, option 2

well as send power to the grid. In these applications it is important that the breaker be bi-directional.

Figures 2.17 and 2.18 show two possible ways to rearrange two Z-source breakers to achieve the flexibility of bi-directional current flow. In both designs, it is possible to define the direction of the current flow by controlling the SCR gate pulses. Breaker in figure 2.18 is preferred as the basic design in this work. It provides a much cleaner isolation of a fault as the input current would fall instantly to zero without any complications of transients.

2.3 Design and Analysis

Some important expressions for currents and voltages are derived in this section that allow researchers to select values for capacitors, inductors, and resistors to be used in

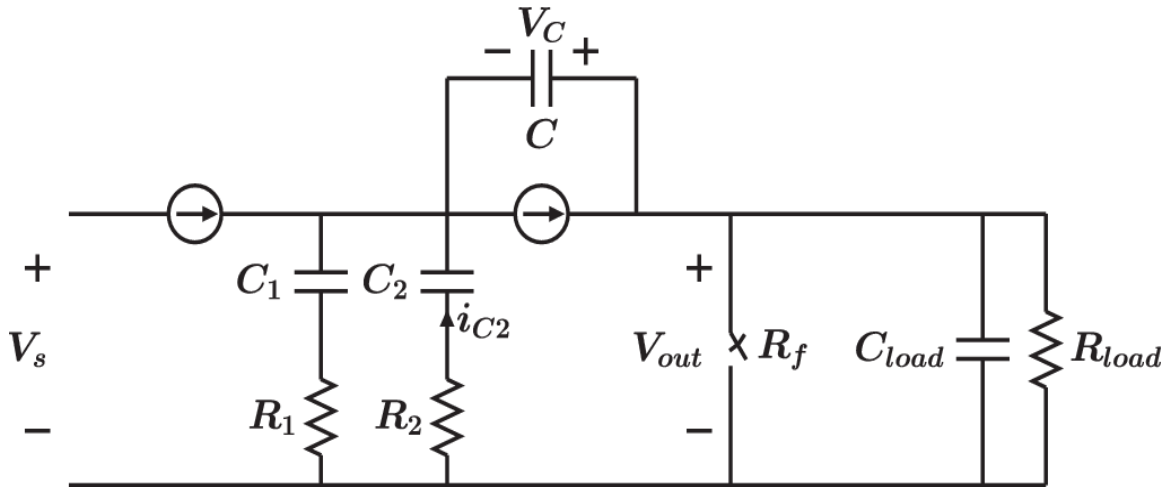

Figure 2.19: Breaker circuit just before the fault

a Z-source breaker design.

Some analysis is already done for Z-source breakers in other works, where expressions for minimum detectable fault current and ramp rate are used to design the components. This work presents how an additional capacitive branch would change those designs. Furthermore, the overshoot in source current and SCR recovery time are also taken into account as design parameters.

2.3.1 Maximum Allowed Step Change in Load Current

Assuming the SCR and inductors to have negligible voltage drop, Figure 2.5 can be simplified to Figure 2.19. The steady-state current path is only through the inductors and SCR. The steady-state current path is of no interest in this section. If C_1 and C_2 are similar in value compared to C_{load} then the RC network in the above Z-source breaker could be further simplified to that shown in Figure 2.20 which shows the transient current path. The transient fault current through this period must be supplied only by the capacitors in Figure 2.20.

The range of fault resistance that would allow breaker to trip has been derived in the Appendix B. Only the final result is presented here.

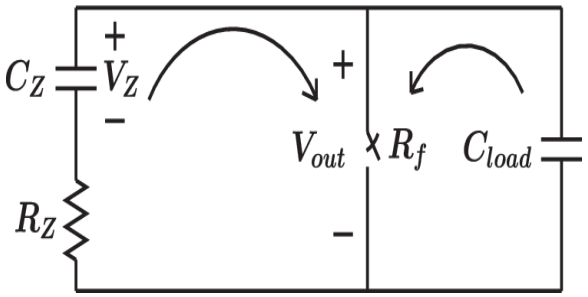

Figure 2.20: Equivalent circuit for Z-source breaker for transient current

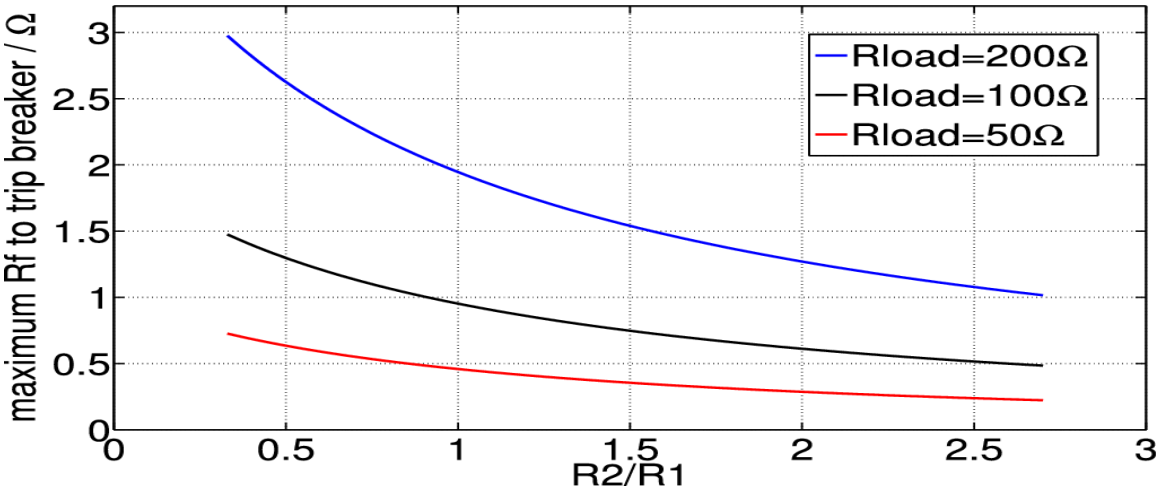

Figure 2.21: Relation between maximum R_f and ratio of series resistors

$$R_f < \frac{ln\left(\frac{R_2}{R_L}\right)}{C_L B\mathbf{W}\left(\frac{R_2}{R_L} ln\left(\frac{R_2}{R_L}\right)\right)} \tag{2.9}$$

Figure 2.21 is the graphical representation of the relation in 2.9. All breaker capacitors are assumed to be $30\mu F$ and load capacitor is taken to be $1mF$. As the ratio of R_2 to R_1 increases, higher percentage of the fault current starts coming through the SCR. This leads to the requirement of a much smaller fault resistance so that enough current comes through R_2 to force SCR current to zero. Also the required fault resistance varies almost proportional to the load resistance which shows that it is not the absolute value of fault current, but its relation to the load current that actually turns OFF the breaker.

To verify the relation shown in Figure 2.9, a simulation is performed in MATLAB

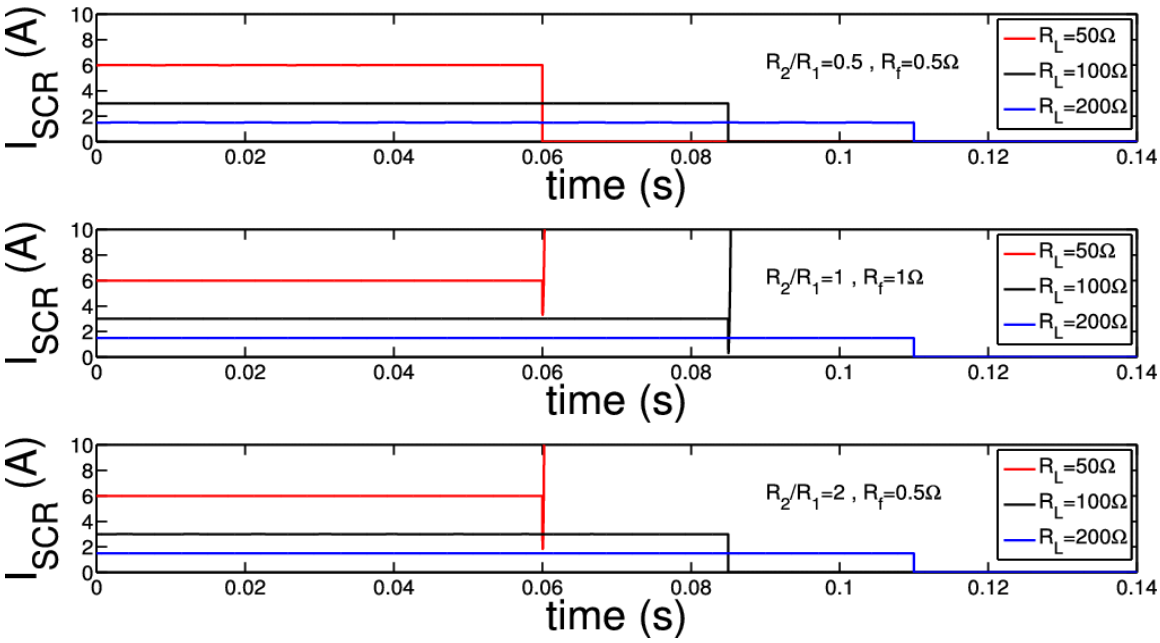

Figure 2.22: Simulation results to verify relation between maximum R_f and ratio of series resistors

Simulink where the effect of different fault resistances is observed on breakers with various load resistances and resistors R_2 to R_1 ratios. All breaker capacitors are assumed to be $30\mu F$ and load capacitor is taken to be $1mF$. Source voltage of $300V$ is used and inductor values are all $1mH$. The results are shown in Figure 2.22 and they conform to the prediction on Figure 2.9. The y-axis is scaled to emphasize the transient in current closer to zero. If the fault resistance is close to the minimum required resistance to trip, then SCR current will go to a very small value before recovering.

As shown in previous section, the breaker itself can act as a low-pass filter so for some small systems the load could be purely resistive, i.e., $C_L = 0$. For those cases, the calculations of this section do not hold true as the output voltage will not decrease exponentially. For those cases, it is even simpler to calculate the minimum step change in load that would cause the breaker to turn OFF.

For analysis, the same equivalent circuit from Figure 2.20 can be used. The transient current now would have to pass through a resistive combination of breaker resistance

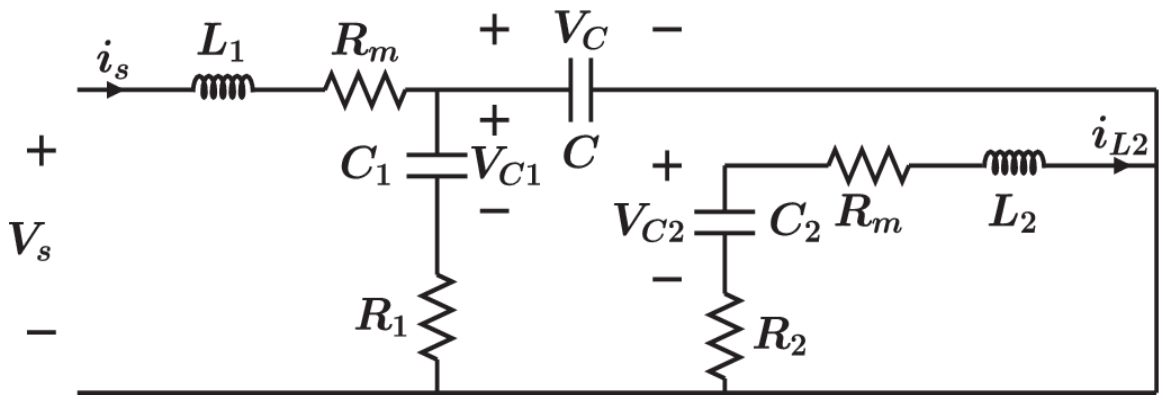

Figure 2.23: Z-source Breaker after the SCR opens

and fault resistance. The current would rise instantaneously and then decline exponentially, so the maximum current would occur as soon as the fault happens. The current labelled i_{C2} in Figure 2.19 is the key to turning breaker OFF because the SCR current falls to zero when that current reaches the inductor current of V_S/R_L :

$$i_{C2max} = \frac{V_S}{(R_1||R_2) + R_f}\left(\frac{R_1}{(R_1 + R_2)}\right. \tag{2.10}$$

Plugging in the condition for turn OFF gives the restriction on fault resistance

$$R_f \leq \frac{R_1(R_L - R_2}{(R_1 + R_2)} \tag{2.11}$$

2.3.2 Maximum Overshoot of Source Current

The analysis in this section deals with the response of Z-source breaker once the SCR is opened. An equivalent circuit after the SCR opens is presented in Figure 2.23 below with R_m as the series resistance of inductors. In this figure, the worst-case scenario for fault is assumed where V_{out} falls to zero instantaneously. Output capacitance is assumed to discharge completely before the SCR opens.

In Figure 2.23, two independent current paths can be seen. One is for the source current that consists of L_1 , C, C_1 , and R_1 resonant components. Other is resonance circuit for C_2 , L_2 , and R_2 . The steady-state current path consists of load resistance and inductor

series resistances. At steady state, the current is dc so there is no drop across inductors and also the drop across the SCR is assumed zero. Assuming that the SCR opens at time $t = 0$, the initial inductor current is the steady-state current

$$i_S(0) = i_{L1}(0) = i_{L2}(0) = \frac{V_S}{R_L + 2R_m} \tag{2.12}$$

At steady state, the drop across the SCR is 0 and there is no current flowing through R_1 and R_2 so the voltage across C_1 and C_2 will be equal. This voltage is calculated as

$$v_{C1}(0) = v_{C2}(0) = V_S - R_m i_S(0) = \frac{V_S(R_L + R_m)}{(R_L + 2R_m)} \tag{2.13}$$

At steady state, the voltage across capacitor C is just the voltage drop across the SCR and inductor L_2 . Taking into account the effect of series resistance R_m, this voltage can be calculated as

$$v_C(0) = V_{SCR} + R_m i_S(0) = \frac{V_S R_m}{(R_L + 2R_m)} \tag{2.14}$$

Applying Laplace transform at the source current path with these initial conditions gives

$$I_S(s) = \frac{a_0 + a_1 s + a_2 s^2}{b_0 + b_1 s + b_2 s^2 + b_3 s^3} \tag{2.15}$$

where

$$a_0 = V_S C(R_L + R_m) + V_S C_1 R_m \tag{2.16}$$

$$a_1 = V_S(L_1(C + C_1) + R_1 C_1 C(R_L + R_m)) \tag{2.17}$$

$$a_2 = V_S L_1 R_1 C_1 C \tag{2.18}$$

$$b_0 = (R_L + 2R_m) \tag{2.19}$$

$$b_1 = (R_L + 2R_m)(R_m(C + C_1) + R_1C_1) \tag{2.20}$$

$$b_2 = (R_L + 2R_m)(R_1R_mC_1C + L_1(C + C_1)) \tag{2.21}$$

$$b_3 = (R_L + 2R_m)L_1R_1C_1C \tag{2.22}$$

The inverse for this Laplace is hard to analyze so the next simplifying assumption is made here. The cubic term in denominator and square term in numerator can be ignored as their coefficient is much smaller than other terms for typical parameter values.

In time domain, the expression for inductor current is

$$i_S(t) = (\alpha_1 cosh(\omega_c t) - \alpha_2 sinh(\omega_c t))e^{-\gamma t} \tag{2.23}$$

where

$$\omega_c = \frac{1}{b_2}\sqrt{\frac{{b_1}^2}{4} - b_0b_2} \tag{2.24}$$

$$\alpha_1 = \frac{a_1}{b_2} \tag{2.25}$$

$$\alpha_2 = \frac{a_1}{\omega_c b_2}\left(\frac{a_0}{a_1} - \frac{b_1}{2b_2}\right) \tag{2.26}$$

$$\gamma = \frac{b_1}{2b_2} \tag{2.27}$$

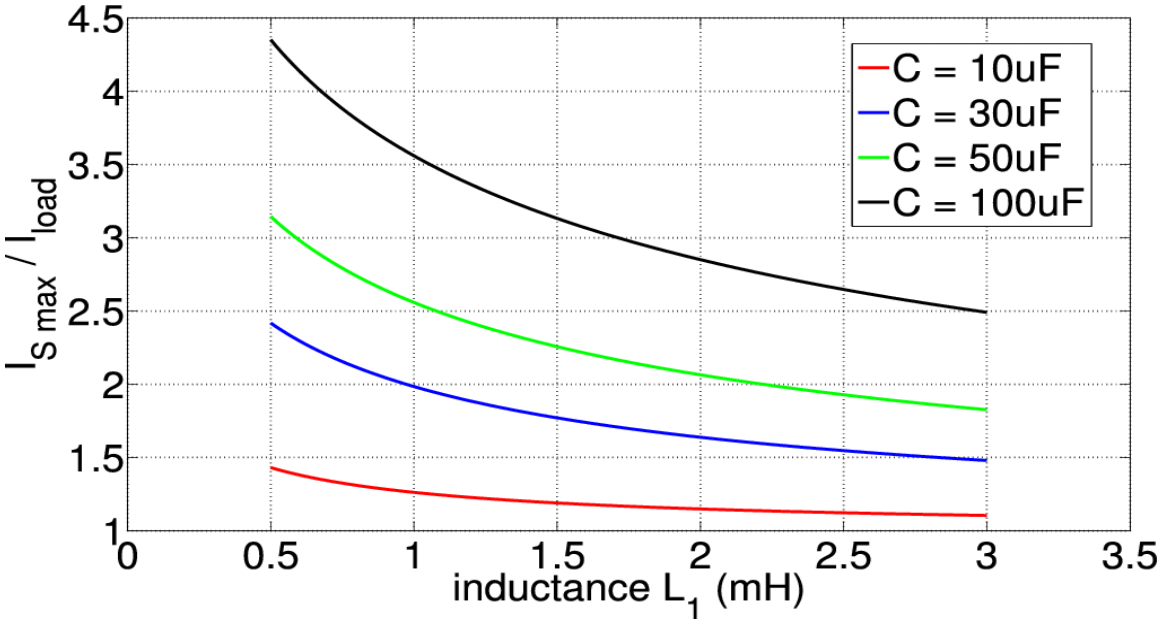

Figure 2.24: Relationship between L_1, C and source current

Figure 2.24 is a plot for ratio of maximum source current to load current during a bolted fault. This plot is independent of L_2 and load circuit. R_1 is selected to be 0.68Ω and R_m is taken to be 1.5Ω. C_1 and C_2 are selected as 30 and 20 μF, respectively. An important trend that can be observed from Figure 2.24 is that the source current spike is always less for larger values of inductor L_1 and smaller values of capacitor C_1.

A simulation is run in MATLAB Simulink to verify the results from Figure 2.24. Source voltage of $100V$ is used with load of 16.67Ω. Plots of source currents from the simulation are shown in Figure 2.25. In the first subplot, inductor L_1 value is kept constant at $1mH$, while different values of capacitor C are used. In the second subplot, C is held at $30\mu F$ while different values of L_1 are tried. Source current is normalized to steady-state value to make comparison with Figure 2.24 easy. It can be seen that the calculations in Figure 2.24 closely predict the simulation result. The simulated waveforms are shown by the solid line and dashed line shows the calculated result from 2.23. The prediction gets slightly less accurate with large values of L_1 and C because of the simplifying assumption made earlier. The dropped terms a_2 and b_3 in 2.15 are directly proportional to L_1 and C.

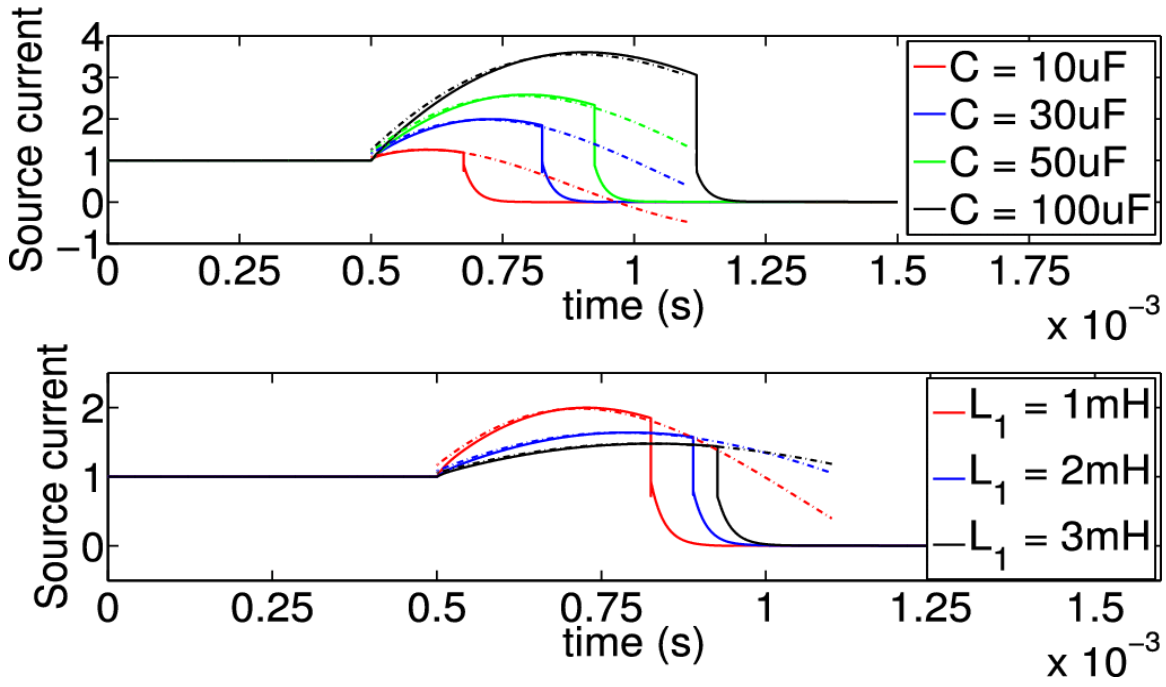

Figure 2.25: Simulation results to verify relationship between L_1, C and source current

2.3.3 Reverse Recovery Time for SCR

Once the current through the SCR reaches zero in absence of a gate signal it turns OFF, but in order to stay off an SCR must be reverse biased for a certain minimum amount of time which is specified in the datasheet. Usually it would be less than $40\mu s$ for a fast recovery inverter grade SCR. After the current through an SCR falls to zero, the voltage across it can be estimated by the expressions for i_S and i_{L_2}.

Elements L_2 , C_2 , R_2 , and R_m form a simple RLC network as shown in Figure 2.26 with initial conditions specified in 2.12 and 2.14. The expression for i_{L_2} is of the underdamped form for typical component values.

$$i_{L_2}(t) = (\beta_1 cos(\omega_d t) + \beta_2 sin(\omega_d t))e^{-\sigma t} \tag{2.28}$$

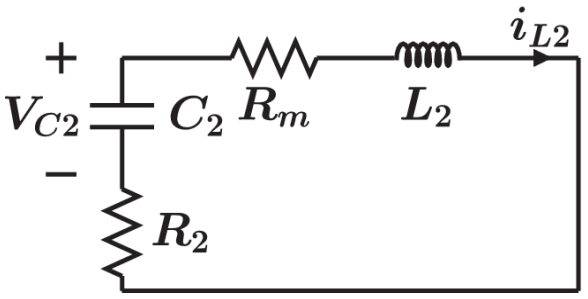

Figure 2.26: Equivalent circuit after SCR is open

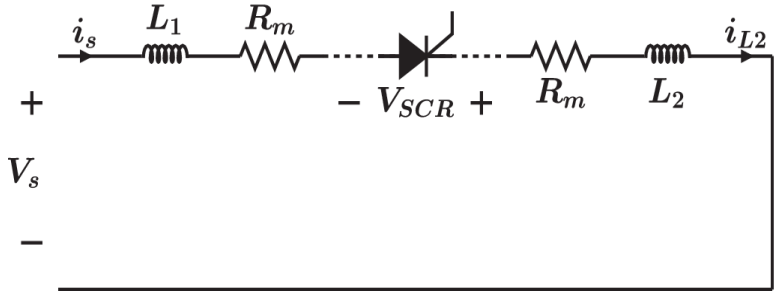

Figure 2.27: Voltage across SCR after current falls to zero

where

$$\sigma = \frac{(R_2 + R_m)}{2L_2} \tag{2.29}$$

$$\omega_d = \sqrt{\frac{1}{L_2 C_2} - \frac{(R_2 + R_m)^2}{4{L_2}^2}} \tag{2.30}$$

$$\beta_1 = \frac{V_S}{(R_L + 2R_m)} \tag{2.31}$$

$$\beta_2 = \frac{V_S(R_L - R_2)}{\omega_d L_2(R_L + 2R_m)} + \frac{\sigma\beta_1}{\omega_d} \tag{2.32}$$

Equations 2.23 and 2.28 lead to an expression for v_{SCR} that can also be seen from Figure 2.27.

$$v_{SCR} = L_1 \frac{di_S}{dt} - V_S + L_2 \frac{di_{L_2}}{dt} + R_m(i_S + i_{L_2}) \tag{2.33}$$

Equation 2.33 does not trace v_{SCR} accurately because of the many assumptions involved in formulating inductor currents however it gives a fairly close estimate of the resonance time, which is the only thing of interest in this section for the selection of SCR. It is important to realize that the resonance time varies drastically with fault resistance, but for design purposes, the worst-case scenario where resonance time will be at minimum should be known. The inductor currents in 2.23 and 2.28 have been formulated for a case with bolted faults, so the resonance time calculated from it will be an estimate of that worstcase scenario. Still it is advised to leave a further 20% margin when selecting an SCR based on resonance times.

Equation 2.33 can alternatively be expressed as

$$v_{SCR} = (\lambda_1 cosh(\omega_c t) + \lambda_2 sinh(\omega_c t))e^{-\gamma t} + (\zeta_1 cos(\omega_d t) + \zeta_2 sin(\omega_d t))e^{-\sigma t} - V_S \tag{2.34}$$

where

$$\lambda_1 = L_1(\alpha_2 \omega_c - \gamma \alpha_1) + R_m \alpha_1 \tag{2.35}$$

$$\lambda_2 = L_1(\alpha_1 \omega_c - \gamma \alpha_2) + R_m \alpha_2 \tag{2.36}$$

$$\zeta_1 = L_2(\beta_2 \omega_d - \sigma \beta_1) + R_m \beta_1 \tag{2.37}$$

$$\zeta_2 = L_2(-\beta_1 \omega_d - \sigma \beta_2) + R_m \beta_2 \tag{2.38}$$

Using 2.34 the resonance time is plotted in Figure 2.28 for various values of L_2 and C_2 . All the other parameters are held constant. Source voltage of $100V$ is used. All the

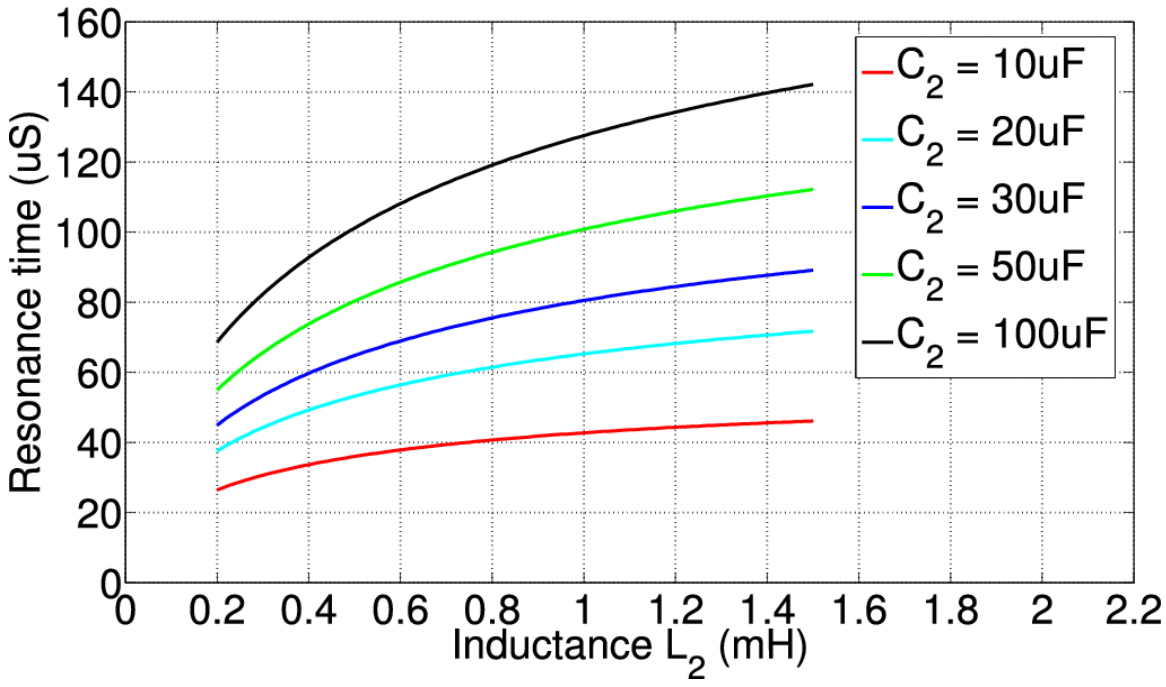

Figure 2.28: Relation of L_2 and C_2 to resonance time

capacitor values are set to $30\mu F$ and inductor L_1 is taken to be $1.8mH$. Resistor values for R_1 , R_2 , R_m, and R_L are selected as 0.68, 1, 1.5, and 16.67Ω, respectively. The trend shown in Figure 2.28 is that for higher values of inductor and capacitor, the SCR stays reverse biased for longer and that makes intuitive sense because the components will be storing energy for longer.

To verify these results, a simulation is run in MATLAB Simulink using the same parameters as the calculations. Figure 2.29 shows the SCR voltage from simulation in solid line and 2.34 is plotted with dashed line. Resonance time is the time taken for voltage to cross zero so the fault is created at $t = 0s$ to make it easier to read resonance time from the graph. In subplot 1, L_2 is set to $0.9mH$ while different values of capacitor C_2 are tried. In subplot 2, C_2 is set at $20\mu F$ and different values of inductors are tried. The simulation results are fairly close to the predicted time from calculation. Equation 2.34 does not predict the initial voltage accurately, but it eventually catches on with the simulated waveform and so the error in resonance time prediction is small.

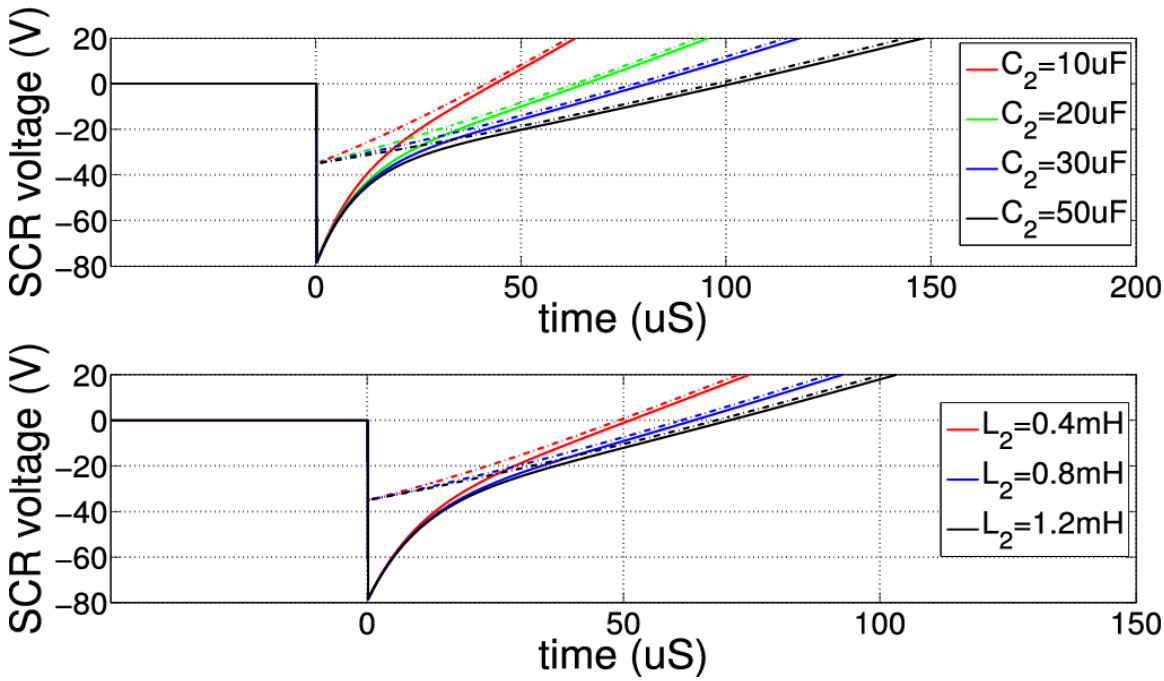

Figure 2.29: Simulation results to verify relation of L_2 and C_2 to resonance time

2.4 Laboratory validation of Modified Z-source breaker designs

Laboratory validations of the previously discussed modified designs 1 and 2 were performed on a low-voltage laboratory setup that would allow breaker testing in all three modes of operation. The schematic of laboratory setup is shown in Figure 2.30. Total load consists of three resistors each rated at 50Ω connected in parallel. The first resistor is connected to the Z-source breaker directly whereas the other two loads are connected through a switch. This allows for testing a step change in load, i.e., to change the steady-state current to three times its initial value. Note that there is no output capacitor in Figure 2.30, so the original Z-source designs would not have allowed such large step change. For design 1, R_2 and R_1 are selected as 1 and 0.68Ω, respectively, using 2.11. This makes sure

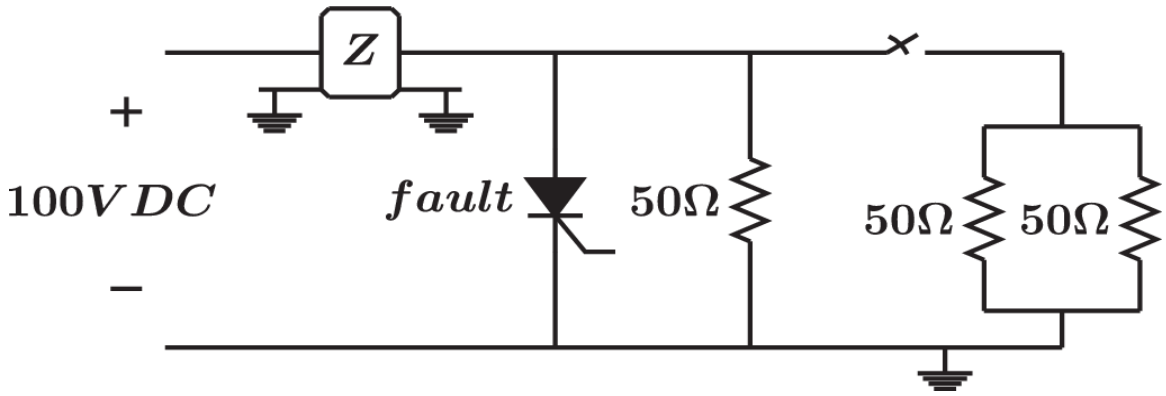

Figure 2.30: Lab test schematic

$R_1(\Omega)$	$R_2(\Omega)$	$C_1(\mu F)$	$C_2(\mu F)$	$C(\mu F)$	$L_1(mH)$	$L_2(mH)$
0.68	1	30	20	30	1.8	0.9

Table 2.5: Components values for Lab setup Design 1

$L_a(\mu H)$	$L_b(\mu H)$	$C_1(\mu F)$	$C_2(\mu F)$	$C(\mu F)$	$L_1(mH)$	$L_2(mH)$
50	75	30	20	30	1.8	0.9

Table 2.6: Components values for Lab setup Design 2

that the step load of 25Ω is not considered a fault. Using the same ratio, C_2 and C_1 are taken as 20 and $30\mu F$. To keep the surge in source current less than double the steady-state current, $C = 30\mu F$ and $L_1 = 1.8mH$ are selected from Figure 2.24. Finally, to keep the resonance time greater than $50\mu s$, $L_2 = 0.9mH$ is selected using Figure 2.28. The inductors used for the lab setup are not machine-coiled so their series resistance Rm is rather high at 1.5Ω. For design 2, L_2 and L_1 are selected with the same ratio as R_2 and R_1 in design 1. The component values are summarized in Table 2.5 and 2.6 for design 1 and 2 respectively.

The first design, shown in Figure 2.31, was tested at $100V$ during a step change in load and during a fault. The step change showed that the breaker remained ON and continued to supply the load. The results for this test are shown in Figure 2.32, including the source current and the SCR current. All the waveforms are imported from lab oscilloscope into an excel file and then plotted through MATLAB. The SCR current drops but does not quite reach zero which keeps the breaker ON. The fault test was conducted by shorting

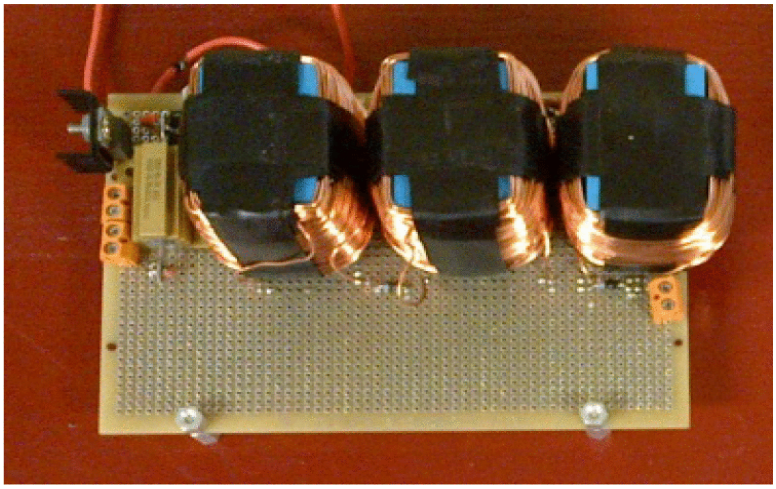

Figure 2.31: Design 1 Z-source breaker

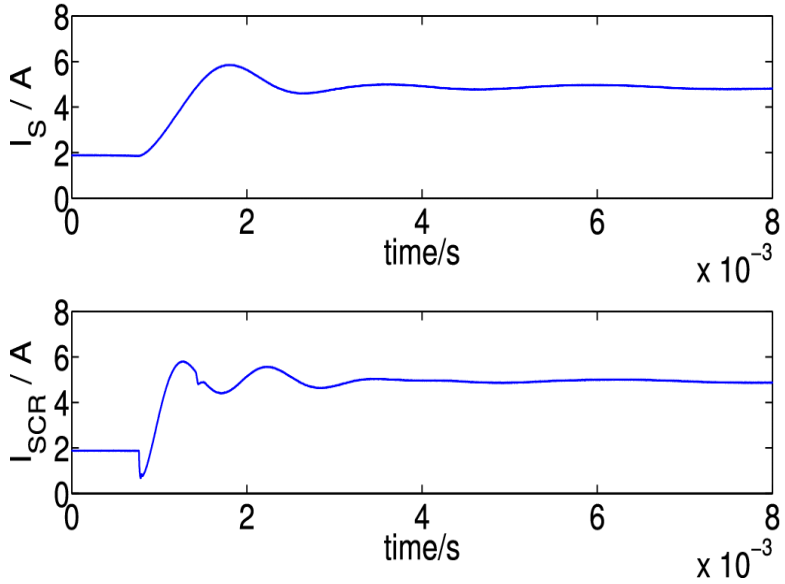

Figure 2.32: Demonstration of step change in load for design 1

the dc bus using an SCR, to ensure that the fault resistance is as constant as possible. Figure 2.33 shows the results from this test, including the source current, SCR current, SCR voltage, and R_2 resistor voltage. The breaker removed the fault allowing the source current to go to zero. The voltage spike across resistor can be used as an indication of fault which can be useful when devising a control algorithm.

The results shown in Figure 2.32 are as predicted by the ratio of components

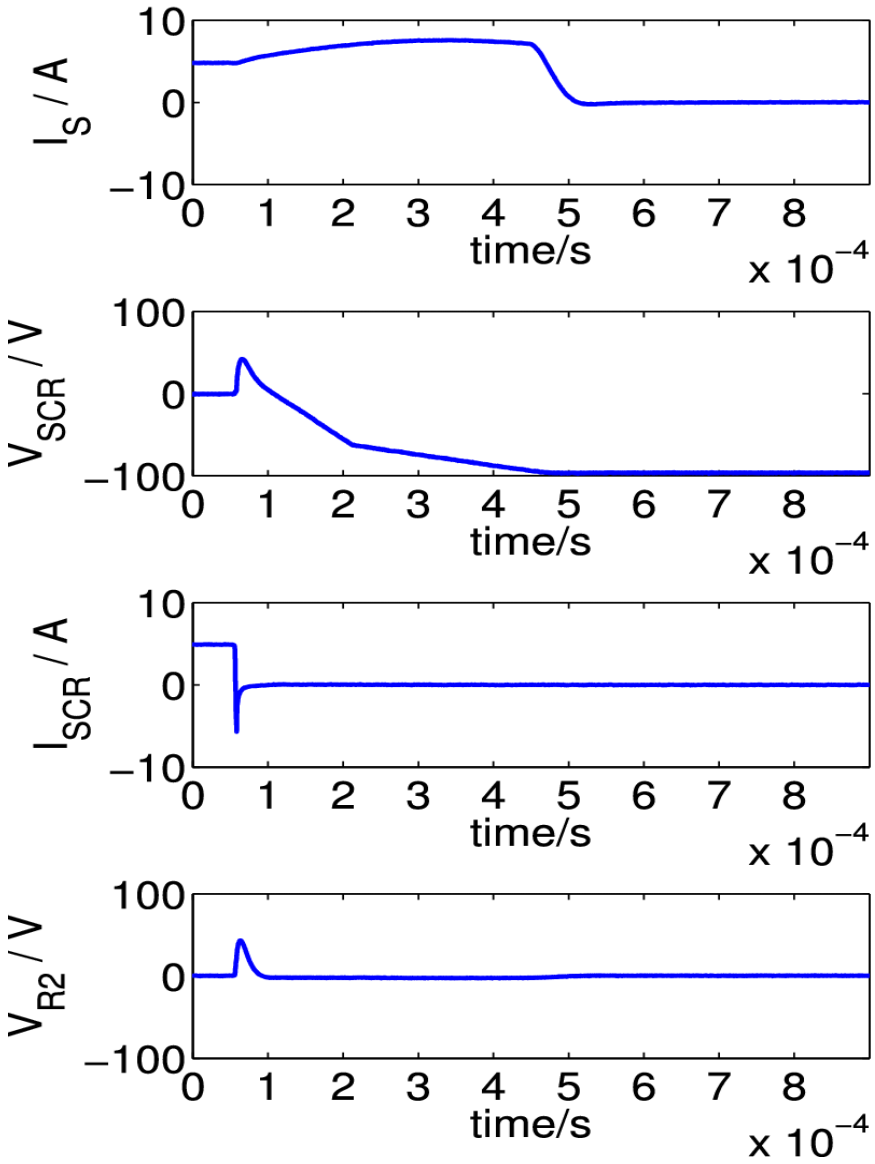

Figure 2.33: Demonstration of fault response for design 1

selected. Plugging in the values of R_2 and R_1 in 2.11 for a load of 50Ω shows that any resistance greater than 19.8Ω will not be considered as fault. Also the surge in source current reads as 1.75 times steady-state current from Figure 2.24 and this is approximately what can be seen in Figure 2.33. From the same figure, the SCR voltage can be seen to stay positive for approximately $50\mu s$ which was one of the design goals.

The second design shown in Figure 2.34 was tested at the same voltage as design 1.

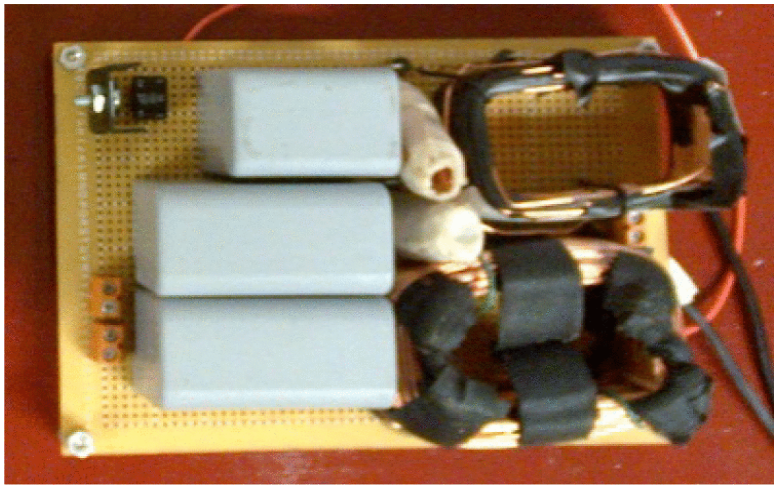

Figure 2.34: Design 2 Z-source breaker

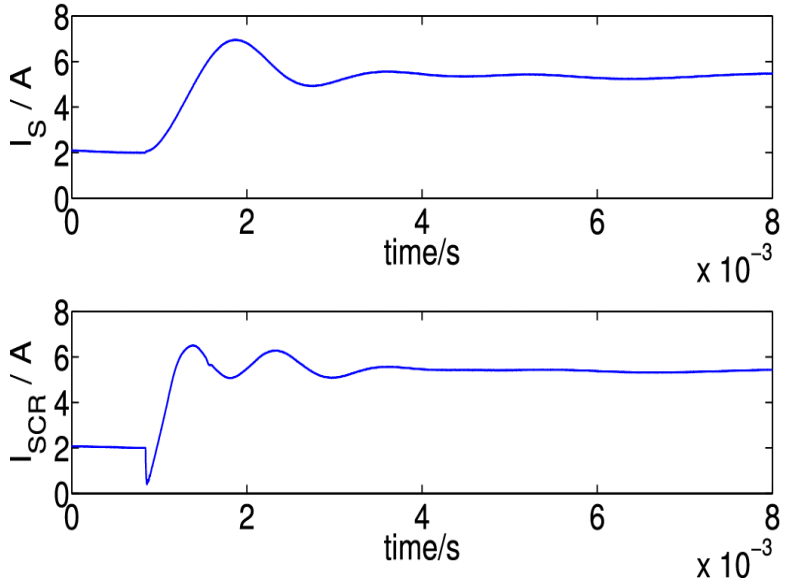

Figure 2.35: Demonstration of step change in load for design 2

The results from the step change in load are shown in Figure 2.35. The step change in load was successful in allowing the load to remain ON after the load resistance was decreased. The fault test results are shown in Figure 2.36. The breaker was able to remove the fault.

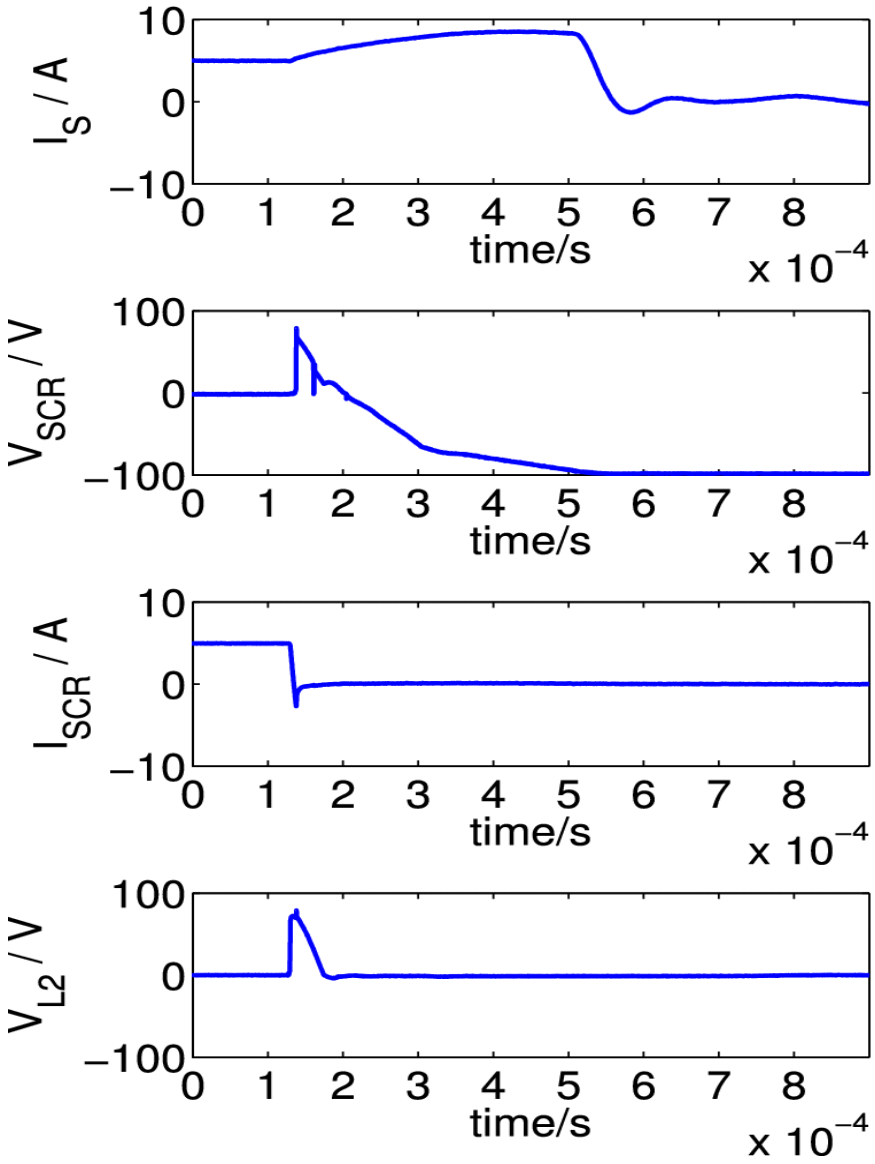

Figure 2.36: Demonstration of fault response for design 2

Chapter 3

The Z-source breaker for dc power system protection

3.1 Breaker Coordination

This chapter of the thesis deals with the higher level coordination of multiple Z-source breakers to achieve protection for a ring connected MVDC power system as shown in Figure 1.3. That Figure is repeated here as Figure 3.1 as it will be referred repeatedly in this chapter.

3.1.1 System Modules

- Source: Each dc source module is an average-value model of a boost converter that is being controlled for a constant output voltage. The output bus voltage selected is 600V boosted from 315V. This dc voltage was selected so that it could later be replicated on hardware in a laboratory environment.

- Bus and Line: The bus is represented by a thicker line at node 3. The single line diagram in Figure 3.1 is a two-line system with one return path or neutral. Transmission

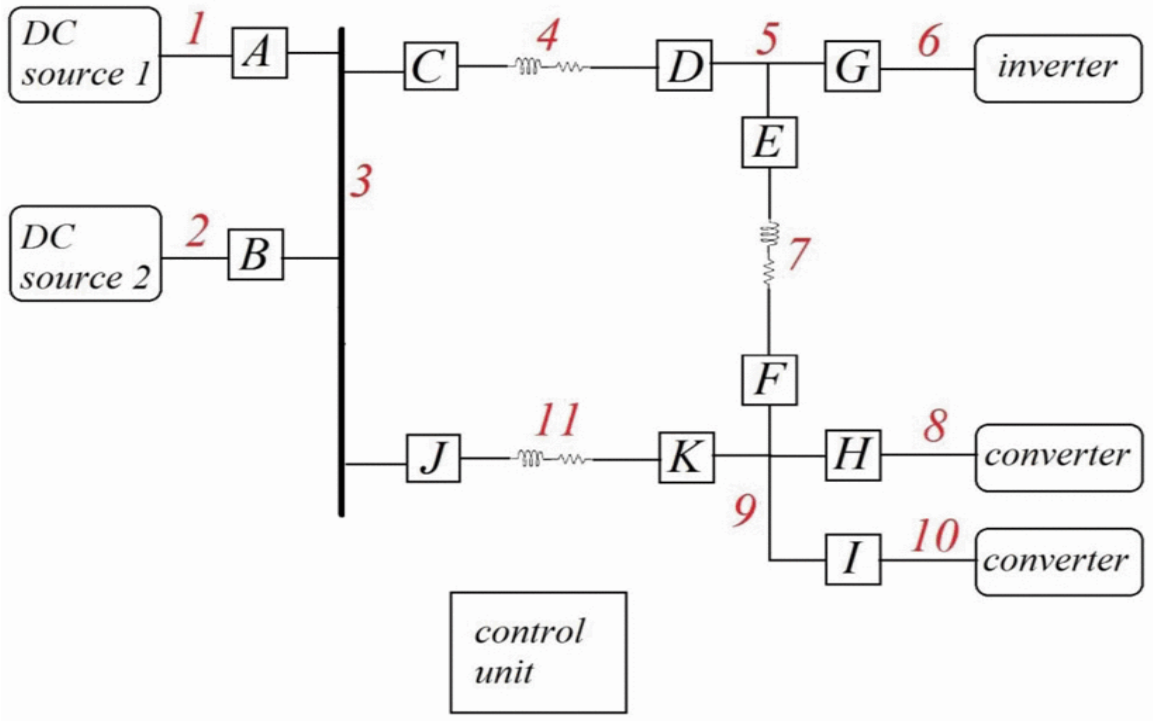

Figure 3.1: Ring-connected MVDC power system

lines have been modelled with inductors and resistors. Capacitance has been ignored for lines that are not expected to be very long.

- Inverter load: A three-phase voltage source inverter is connected to a constant power load with power factor 0.85 lagging. The modulation index of inverter is being controlled to ensure constant output power of 5kW. An average value-model is used for the simulation to speed up the process.

- Converter load: These loads mimic a pulsed load on a ship system. Each converter module is a boost converter with duty cycle control to ensure constant power of 1.25KW at the output. An average-value model is used for the simulation.

- Breakers and control unit: Since the inverter load is of higher power than the converter loads combined, the steady state direction of current through E and F is upwards. However, if the inverter load is turned off or reduced the direction through those breakers will have to be reversed. Therefore on locations E and F bidirectional break-

Fault Location	*Breakers that opened*	*Desired breakers to open*	*Reason for difference*	*Fault category*
1	A,E,F	A	Large transients through F,E	Terminal
2	B,E,F	B	Large transients through F,E	Terminal
3	All	All		Bus
4	C,D	C,D		Line
5	C,D,G,E,F	C,D,G,E,F		Junction
6	C,D,G,E,F	G	Change in direction for F,E	Terminal
7	F,E	F,E		Line
8	H	H		Terminal
9	E,F,H,I,J,K	E,F,H,I,J,K		Junction
10	I	I		Terminal
11	E,F,H,I,J,K	J,K	Change in direction for F,E	Line

Table 3.1: Fault Summary without a control unit

ers are required. On other locations simple unidirectional breakers would be sufficient. The control unit and breakers are described in the later sections.

3.1.2 Need for coordination

The bidirectional breaker design shown in Figure 2.18 does not automatically allow current to change direction. The correct SCR gates will need to be triggered. Some external control is therefore required to prevent extra breakers from opening in ring architecture MVDC systems. Table 3.1 summarizes the fault analysis for system in Figure 3.1. For this table, it is assumed that the initial steady-state direction of current through breaker F and E is upwards from junction 9 to 5.

Breakers E and F carry the smallest steady-state current so are most susceptible to opening at transients. Any fluctuation in load would cause a change in dc bus voltage if several sources are connected through droop control. That would result in capacitors at the input of the inverter load to discharge and cause system transients. Similarly the inductors at the input of an inductive load might also cause disturbances if current is interrupted by

a fault. The protection scheme has to be sensitive enough to detect large changes in current but also must ensure that breakers that open because of transients must be closed once the system has settled.

3.1.3 Central control scheme

The faults have been categorized in four ways.

- Terminal Fault: Can be isolated from the breaker by opening exactly one breaker. These faults can be at the source or load end.
- Line Fault: Can be isolated from the system by opening exactly two breakers.
- Junction Fault: Needs more than two breakers to isolate this fault.
- Breaker Bus Fault: Cannot be isolated from the system. All breakers must open.

The crux of the control scheme is that all breakers would be continuously sending their state signals to the central control unit. After the fault, once the breakers are open, the control unit determines the location of the fault. The control would be programmed specific to one load scheme with all the information on which generators and what loads are online. It would then send start signals to only those breakers that could stay closed without feeding any current to the fault location. So the breaker opening in response to a fault is automatic, but in some cases the breakers would be signaled to close by the control. This will cause interruption but by making some design changes to the breakers and keeping the entire process fast, those interruption effects could be minimized.

In this embodiment, each breaker would continuously send a two bit status signal to the control unit. A simple current sensor can be used to generate the most significant bit, MSB, of state signal for each breaker. The sensor circuit does not need to sense the actual magnitude of current it just needs to sense when the current through the SCR goes to zero.

All these single bit state signals (1 or 0) are sent continuously to the central breaker control unit which is returning SCR gate signals to the breakers. An analog comparator would be enough and SCR current would be compared to a small value close to zero.

The Least significant bit, LSB, is generated when the output current is compared to a predetermined value, generally in excess of 3 or 4 times the full load steady-state current but less than the minimum fault current. Therefore, the system has to be designed and analyzed for faults and load flow before placing the protection scheme in place. The LSB is used to localize the fault. The output current shoots up when the fault on the output of the breaker and goes to zero when the fault is on the input.

The dc sources are also required to send the status bit to the central unit so that it can locate the faults that happen at their output nodes. A single bit like the LSB of the breakers would be sufficient.

With this data the control unit can localize the fault and close any breakers that do not need to be open. A fault in each location would result in a unique indicator that is listed in Table 3.2. The MSB of status bit is 1 for open breaker and 0 for close breaker. The LSB is 1 for fault at the output of a breaker and 0 for fault at the input of a breaker. As an example consider a fault that occurs at location 5. The status bits for breaker D and E would be 11 while breaker G would be 10. However, if the inverter load was offline before this fault then status bit for D would be 11 and E would be 10.

Table 3.2 shows how a fault at each of the locations in Figure 3.1 can be uniquely identified based on the status bits received from breakers A to K and also the sources S1 and S2.

These unique indicators in Table 3.2 are specific to the system shown in Figure 3.1. However, each category of fault identified earlier could have its own indicator which would work for any general system design. For example, if any load end terminal breaker opens and the fault is at the output then irrespective of what other breakers open, the fault location can be identified as being at that terminal. For a source end terminal fault, the indicator is fault happening at the output of the source. For a bus fault it would be fault

Fault Location	Unique Indicator (Breaker name =status bits)	Required action (after waiting time T)
1	S1=1 AND A=10	Signal all breakers except A to close
2	S2=1 AND B=10	Signal all breakers except B to close
3	A=11 OR B=11	Nothing
4	C=11	Signal all breakers except C and D to close
5	Line 4 is Online AND D=11 OR Line 4 is Offline AND E=11	Signal all breakers except C,D,E,F and G to close
6	G=11	Signal all breakers except G to close
7	Inverter is Online AND F=11 OR Inverter is Offline AND E=11	Signal all breakers E and F to close
8	H=11	Signal all breakers except H to close
9	Line 11 is Online AND K=11 OR Line 11 is Offline AND F=11	Signal all breakers except J,K,E,F,H and I to close
10	I=11	Signal all breakers except I to close
11	J=11	Signal all breakers except J and K to close

Table 3.2: Fault action summary with a control unit

at the output of a source end terminal breaker. The indicator for any line fault is that for a pair of line breakers open such that one sees the fault at its output and other sees it at its input. This logic is very similar to differential protection schemes used in ac power systems.

3.1.4 Control and processing solutions

There are two different processing requirements in the proposed dc system with z-source breakers and there are different factors governing the selection for both. For individual z-source breakers, according to the central control scheme, it is not essential to process instantly because the settling time is in milliseconds which is significantly larger than processing time in any of the modern day microprocessors. Also the processing involved for the breaker is not very complicated. The processor needs to have ADC capabilities to

deal with current sensor inputs and needs to have UART feature for communication with central control. It also needs to have enough power to drive relay for SCR gate control. Most of the microprocessor and DSP have all these features so the real deciding factor is size because the controlling device needs to be enclosed in the breaker box. Arduino UNO is one such device which offers only the minimum required features and is compact in size.

The other processing requirement is the central control that unlike the z-source breaker controller, is dealing with information from multiple breakers. If the central control deals with all the information in series it will have buffering time because the fault localizing algorithm requires all the information to be present. This buffering might approach the settling time for large number of breakers. It is therefore a better approach to use an FPGA as a central control as it can process all the information in parallel and make fast decisions. Size is not a factor in this selection as central control can be placed isolated from rest of the system.

For communication between z-source breakers and central control the first decision involves the mode of communication being wired or wireless. Wired is the better option for small distances or where speed is a biggest concern; however wireless is more suited for a ship environment. A fault on shipboard is likely to be of a physical nature where communication lines are as susceptible to damage as the power lines so the more secure option is to go for wireless. After the initial phase of installation the wireless system is more flexible than wired and can easily be expanded.

Most establishments already have a wireless network on which data can be transferred. If an independent system is required, like it would be in the proposed lab dc system, then it can be programmed through Bluetooth or Xbee. Both support UART and offer similar range but Bluetooth offers better speed. Presently the modules available have a range of 100m at 2.0 Mbps. The range of 100m would work for a lab environment but for some applications it might not prove to be enough. The option in that case would be to install boosters at fixed distances to enhance the signals. This might cause significant delays so care must be taken in placement of breakers and control within the ship. Some

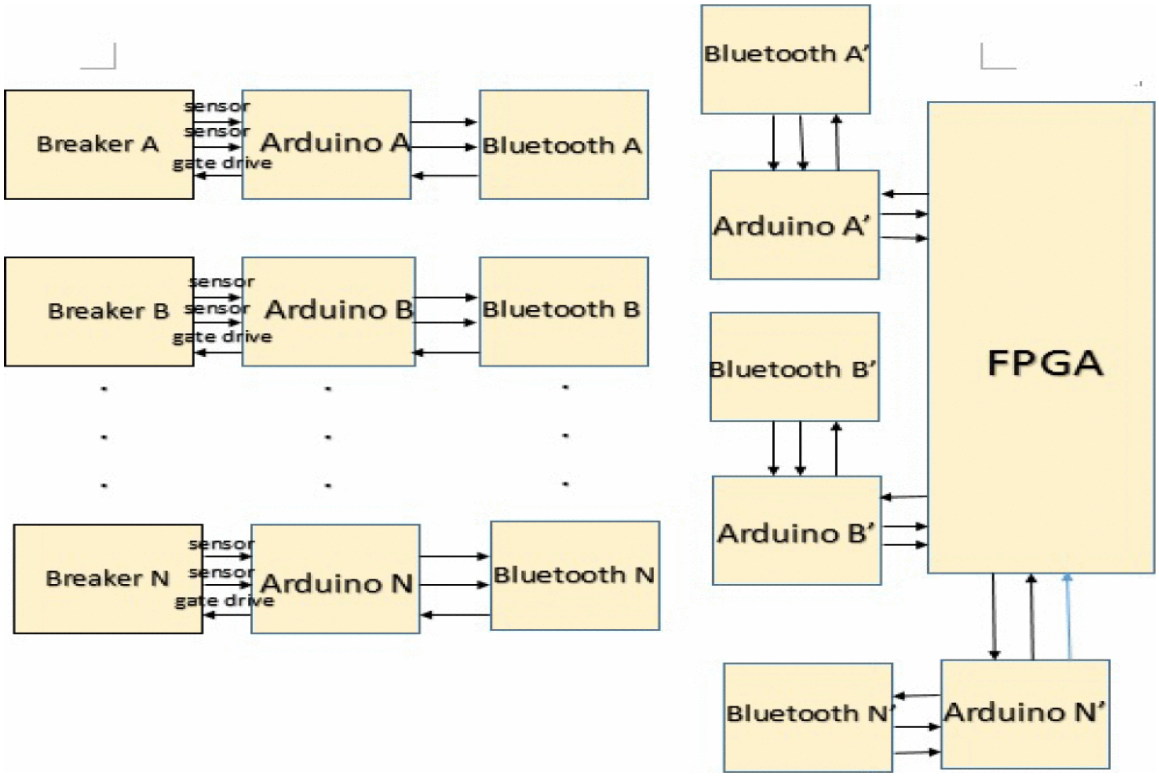

Figure 3.2: Proposed communication architecture

programming has already been carried out on Bluetooth to send data to and from a pair of Arduinos at small range which is to be used for a dc lab system.

The proposed communication architecture for the dc lab system is shown in Figure 3.2. Each breaker will need to have a current sensor at input and output for the differential protection scheme to work. The sensor must not saturate for up to 4 to 5 times nominal current to detect the overshoot. The Arduinos analog pin reads the value sent by the sensors connected to the breaker .Then the Arduino compares it with a small value and generates the most significant bit (MSB). This bit contains the information whether a breaker is ON or OFF. The Least significant bit, LSB, is generated when the output current is compared to a predetermined value, generally in excess of 3 or 4 times the full load steady-state current but less than the minimum fault current. This bit contains the information if the breaker has seen a fault at its output or not.

The arduino encodes this information in UART format and instructs the blue-

tooth to transfer this information to its complementary bluetooth where another adruino decodes the information and passes it to the central FPGA. In this mode of communication Bluetooth devices will be programmed as a pair, each with a unique address to avoid interference. Central FPGA gathers data from all the active breakers and sends gate signals for all the SCRs in each breaker based on the received information. The gate signals follow the same path but in the other direction till they reach the respective breaker. SCRs used in this lab design require 150mA gate current to operate and arduino cannot supply this current directly so a MOSFET based current amplifier will be operated by each arduino in breaker box.

3.1.5 Breaker design modifications

The central control scheme suggested in the previous section would require some breakers to close quickly after staying open for a few microseconds. For a cleaner isolation in a large system, cross connected breakers are preferred over series connected breakers. To stay consistent with earlier modification, an extra capacitive branch is added at the output of the breaker. A series resistor is added to the shunt capacitors similar to design 1 introduced in chapter 2. Other changes made are:

- A small inductance could be added in series with the SCR.
- A large resistance in parallel to a diode could be used in series with the shunt capacitors. This would provide different charging and discharging resistance. The discharging resistance should be small because the breaker would need to open immediately in case of a fault. Charging resistance would be large so that when the breaker closes it would not demand a large inrush current.
- Also with a large charging resistance, the diode in parallel to the inductors will not be needed, as it is in the path of inductor discharge circuit too.

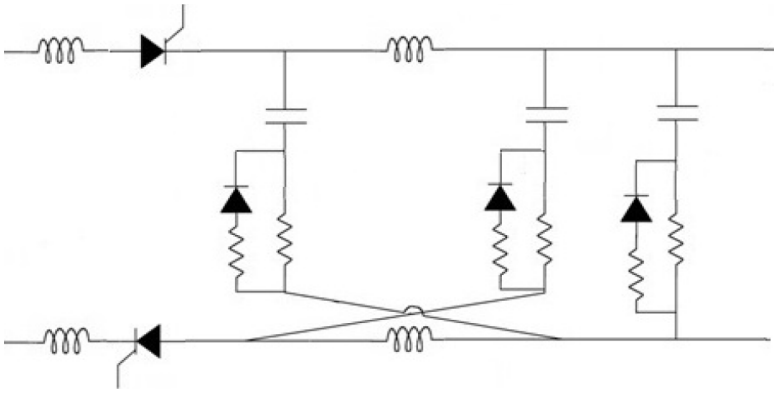

Figure 3.3: Cross connected modified Z-source breaker

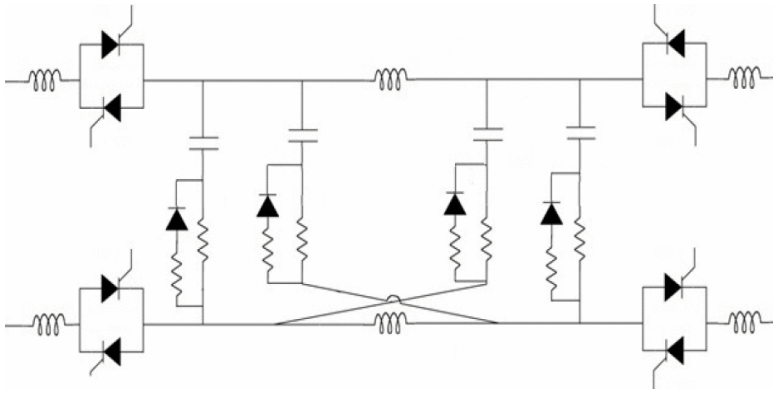

Figure 3.4: Bidirectional Cross connected modified Z-source breaker

The modified breaker is shown in Figure 3.3. The bidirectional breaker with the same changes is shown in Figure 3.4.

3.2 Simulation Results from Central control scheme

The simulation is run on PSCAD for the system described in figure 3.1 using the final breaker designs of Figures 3.3 and 3.4. Figure 3.5 shows the input current for four of the breakers when a shunt fault is created at location 2. The fault is created at 1 second and lasts indefinitely. Breaker B opens instantly, isolating the fault from rest of the system. Breaker A has to double its current now because source 1 must provide for all loads. The

transients force breaker E current to zero so that it opens. Those transients can be seen in breaker J current as well but they are not enough to force it to zero. After an arbitrary delay of 0.2 seconds, which is to model process delays, the control sends gate signals to all breakers except B. Breaker E closes, charging smoothly to a steady-state value to avoid any more transients in the system. Breaker J current also changes smoothly to accommodate the changes in the system.

Figure 3.6 shows the results of same fault at location 6. Breaker G operates instantly to make the inverter load go offline. This means the direction of current through breakers E and F needs to reverse. In the absence of a control signal breaker E current goes to zero and the breaker opens. This isolates line 4 from rest of the system and breaker D also opens as SCR current is forced to zero. Again, transients cause a disturbance in breaker K but not enough to open it. After 0.2 seconds the breakers receive a gate signal and smoothly integrate into the system. The current through breaker E has changed direction as required.

Figure 3.7 shows the results for fault at location 9. This one is easily isolated without the transients causing any unnecessary breaker opening.

Figure 3.8 is again a fault at location 9 but this time in the system line 11 is offline. This could be because of maintenance or because of a previous fault. Still the fault is located and required breakers open. This result is important as it shows the flexibility of the control.

3.3 Low Voltage dc test bed

3.3.1 Hardware design

Three distinct units of hardware in the system are the dc sources, z-source breaker enclosure and Loads. The source and load both need to be programmable so that faults can be simulated at either end of a breaker. The dc source has been designed as an IGBT

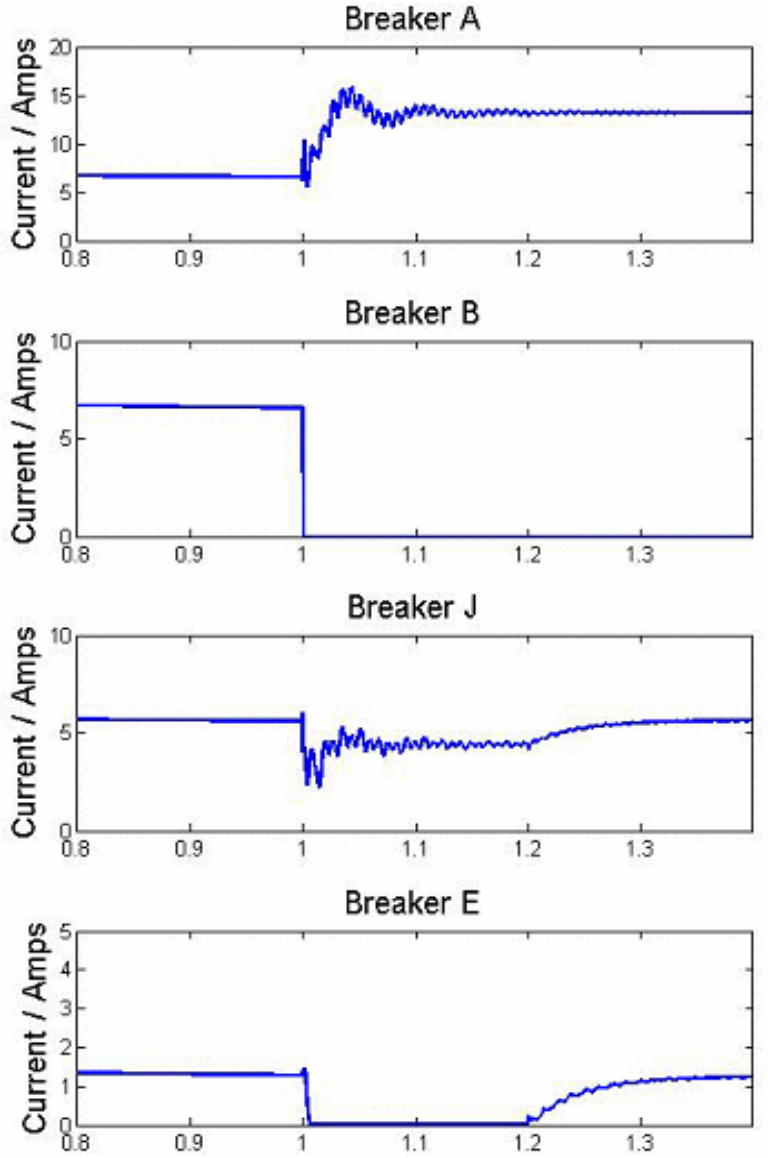

Figure 3.5: Response of the breakers for fault at location 2

Output Voltage Range	**Nominal Voltage**	**Rated Current**	**Line Inductor**	**DC Capacitor**
$280 - 440VDC$	$375VDC$	$30ADC$	$1.8mH$	$1.2mF$

Table 3.3: DC source parameters

based three phase active rectifier with power factor correction. The important parameters of the design are listed in Table 3.3.

For the z-source breakers the design shown in Figure 3.3 is preferred over other

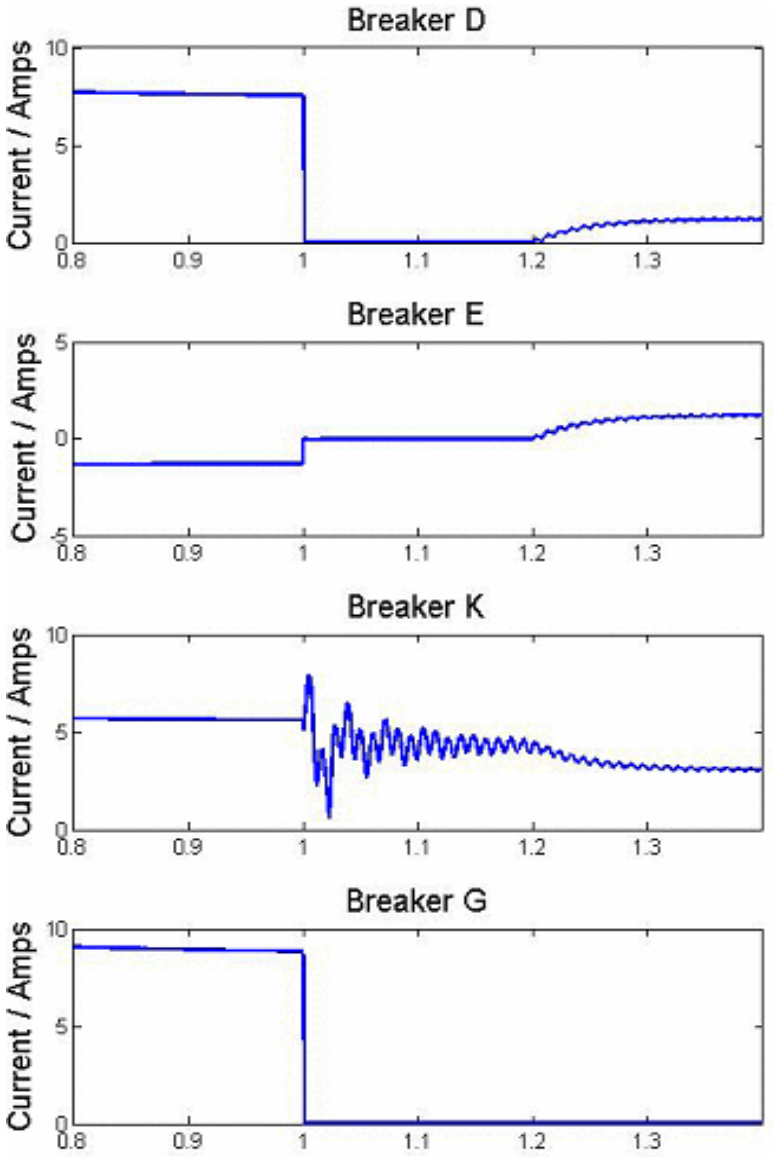

Figure 3.6: Response of the breakers for fault at location 6

options because it allows instant isolation between load and source. Other features like high charging resistance and additional capacitive branch are also present. The component values selected for the breaker are shown in table 3.4.

Breakers to be installed in this system need to be compact and portable. The ongoing work has been focused on designing such compact boxes for z-source breaker with maximum steady state ratings of 900V, 30A. For the initial work two such boxes have been

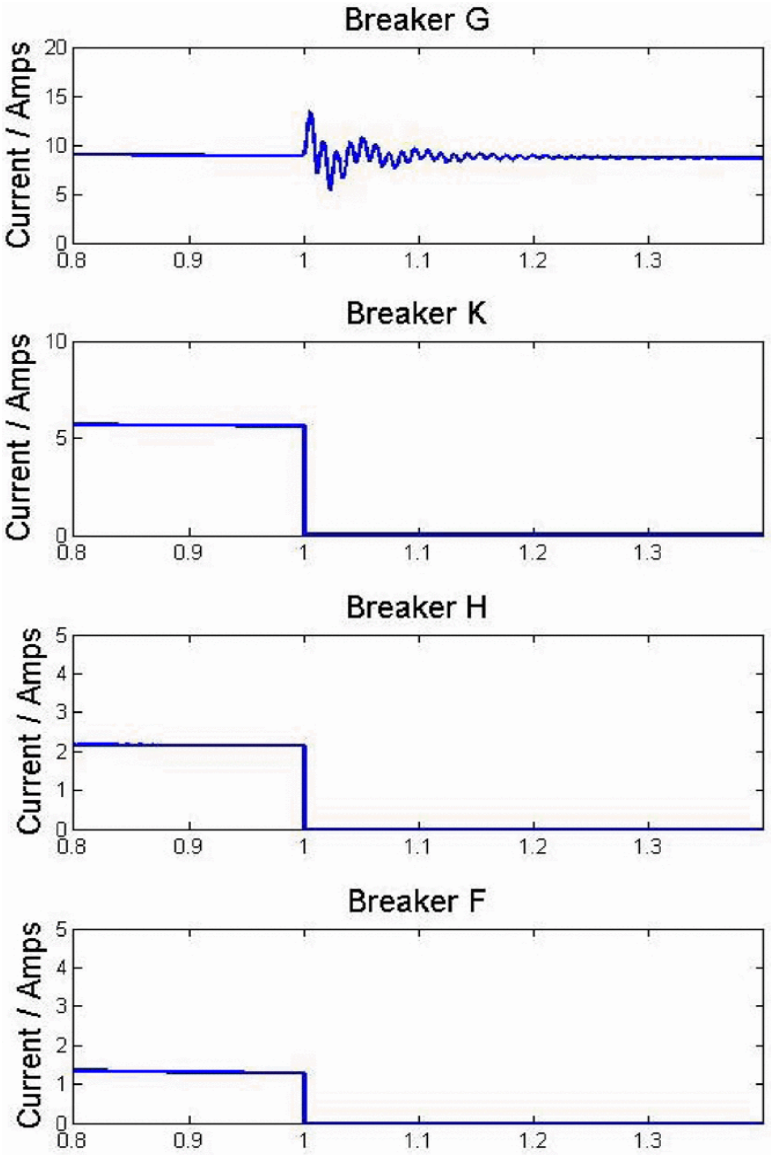

Figure 3.7: Response of the breakers for fault at location 9

Maximum Voltage	$900VDC$
Nominal current	$30ADC$
SCR turn off time	$30\mu s$
Inductor	$1mH$
Capacitor	$50\mu F$
Discharging resistor	2Ω
Charging resistor	100Ω

Table 3.4: Z-source breaker parameters

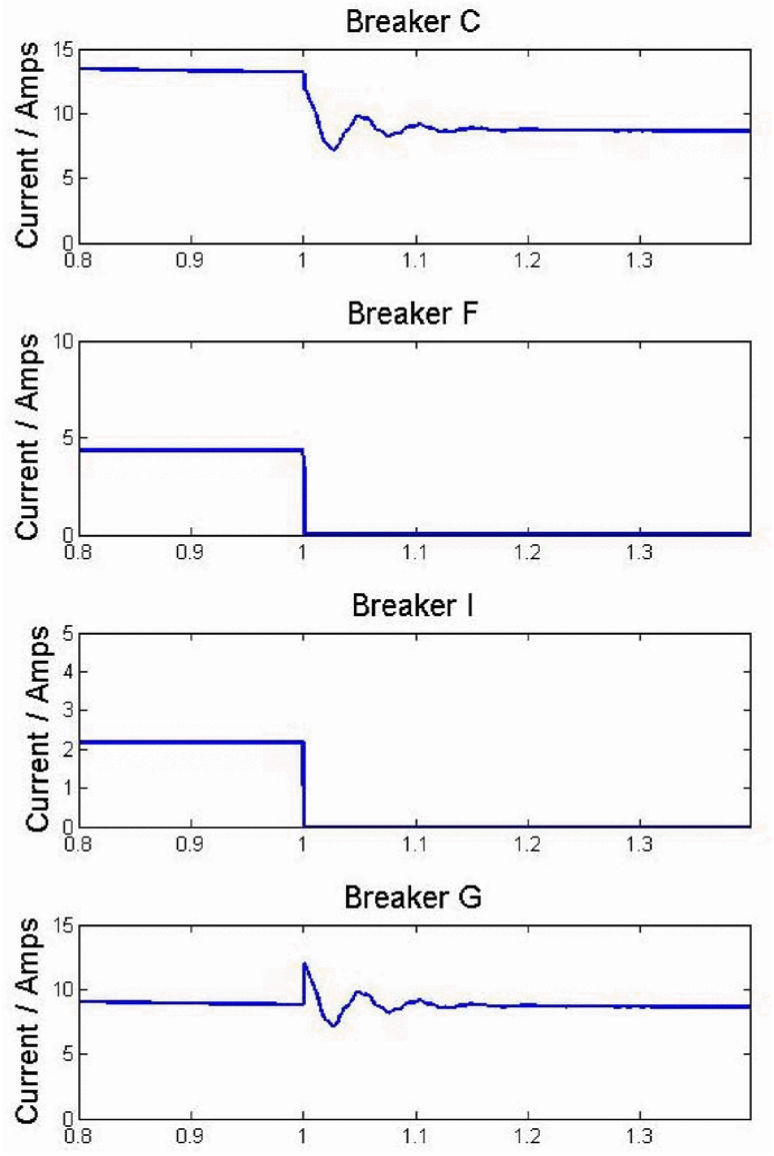

Figure 3.8: Response of the breakers for fault at location 9 with Line 11 offline

assembled. The selected enclosures measures 12 by 10 by 6 inches and one of them being compiled is shown in Figure 3.9. An active rectifier has been put together through IGBT modules and can be controlled to supply a steady output dc voltage in the range 280V to 400V. This rectifier system can be used as a dc source for testing these breakers and is shown in Figure 3.10.

Performance of the rectifier as a dc source and Z-source breaker box is presented

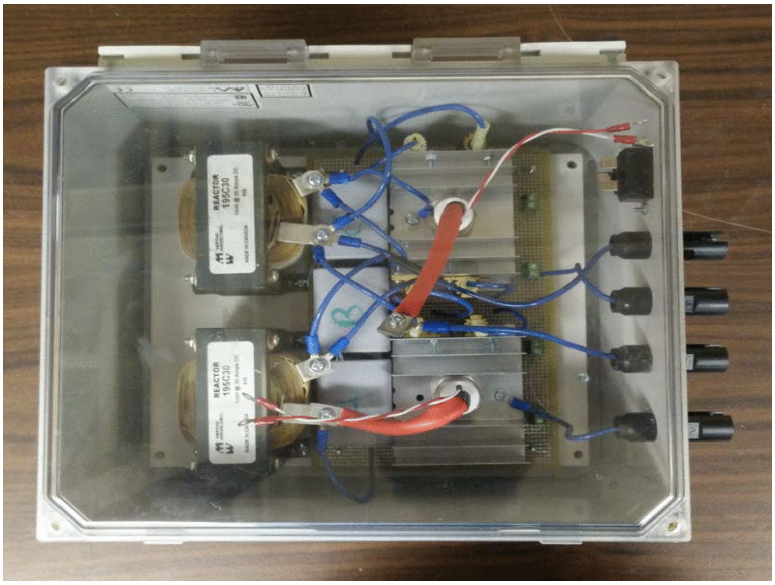

Figure 3.9: Prototype z-source breaker enclosure

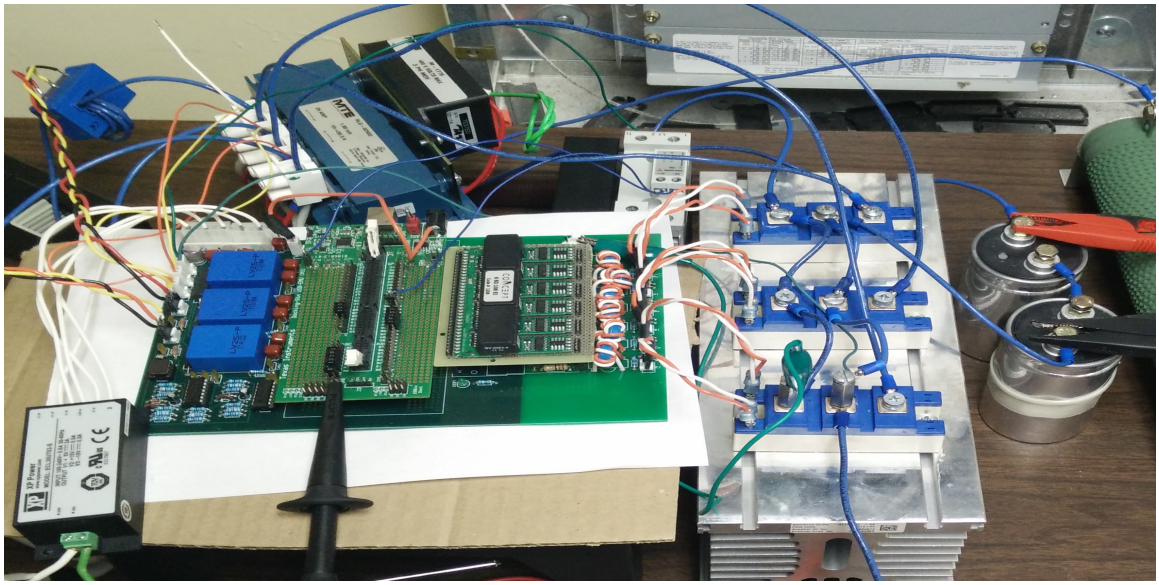

Figure 3.10: Active rectifier assembled in the lab

in this section. A simulation for three phase active rectifier with unity power factor control was run with the same parameters as table 3.3 in MATLAB. Load resistance of 100Ω is used. Results are shown in the Figure 3.11.

In Figure 3.11 the top plot shows the dc voltage which is very close to the required

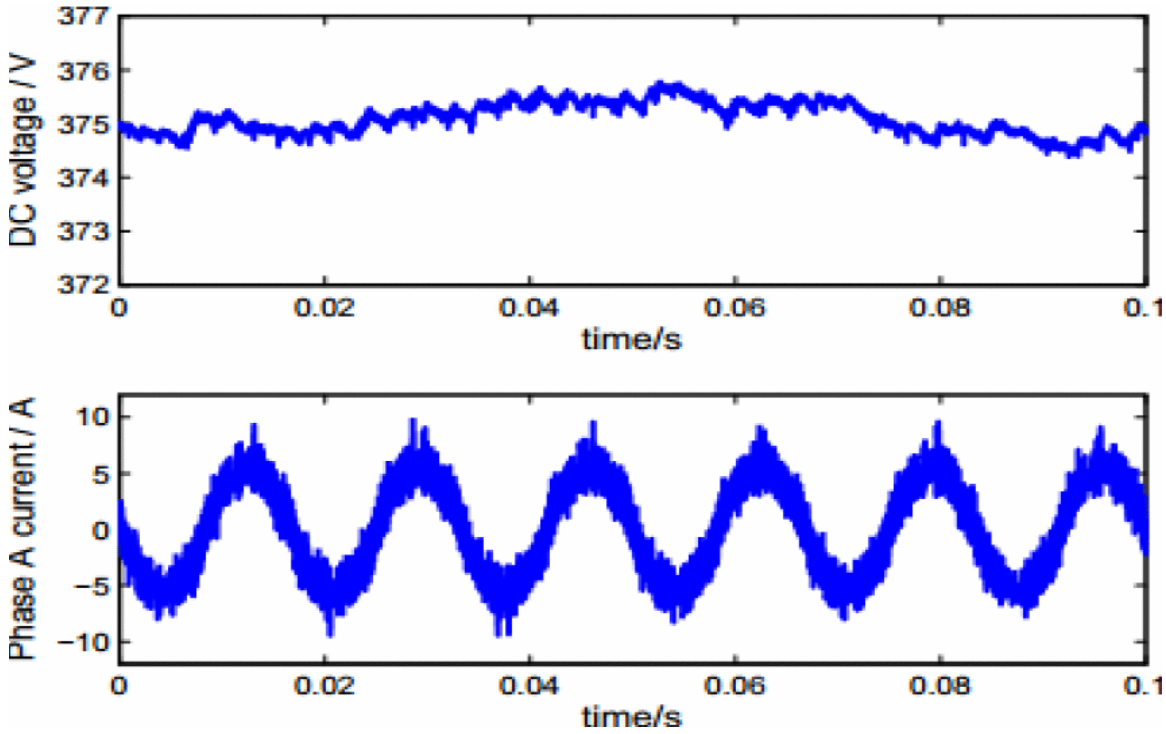

Figure 3.11: Active rectifier MATLAB simulation

voltage of $375V$. The bottom plot is the line current in inductor on phase A. Noise in current is due to hysteresis time step of $25\mu s$ and inductance of $1.8mH$. These values of inductance and time step are selected in the simulation for a fair comparison with hardware results.

The hardware to assemble the dc source is selected according to Table 3.3. Load of 100Ω is used. DSP F28335 is used to control the Gate driver of IGBTs rated at 1200V 50A. The control loop in DSP is triggered every $25\mu s$ which is the limit based on the computational requirements of the code. The Source is run to give a dc output of $375V$ and results are shown in Figure 3.12. The plot from probe 1 shows the dc voltage which has a mean value close to $375V$. The plot from probe 4 is line current from inductor in phase A.

To test the breaker enclosure shown in Figure 3.9, it is connected to the active rectifier dc source and 100Ω load. SCRs in the breaker are powered to connect the source to the load. When steady state is reached the gate signals are removed. A fault is then generated across the load resistance and response of the system is recorded. Important

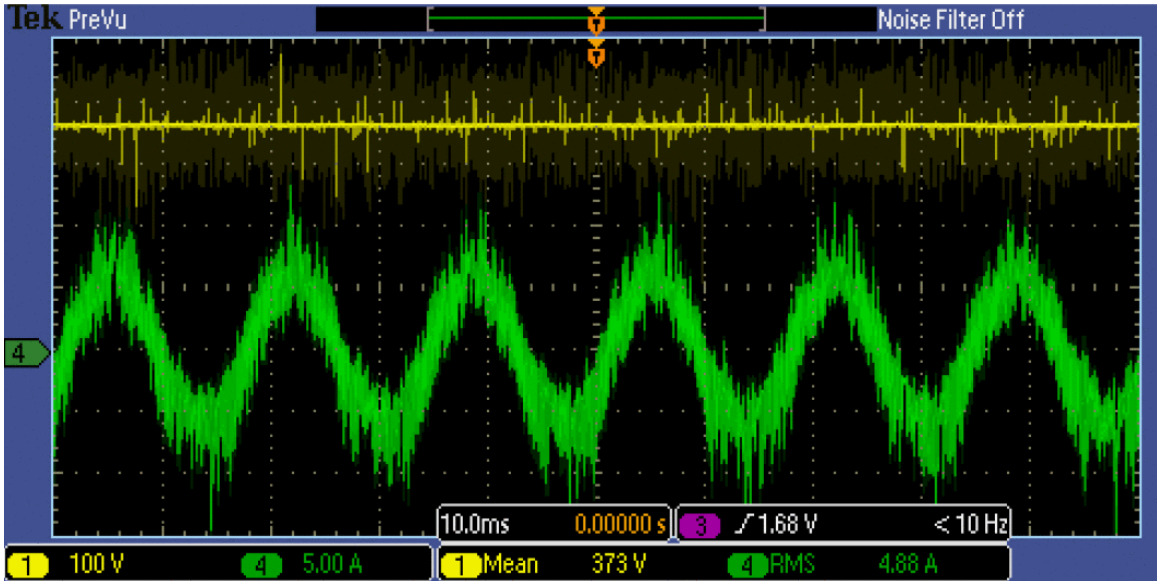

Figure 3.12: Active rectifier output voltage and input line current

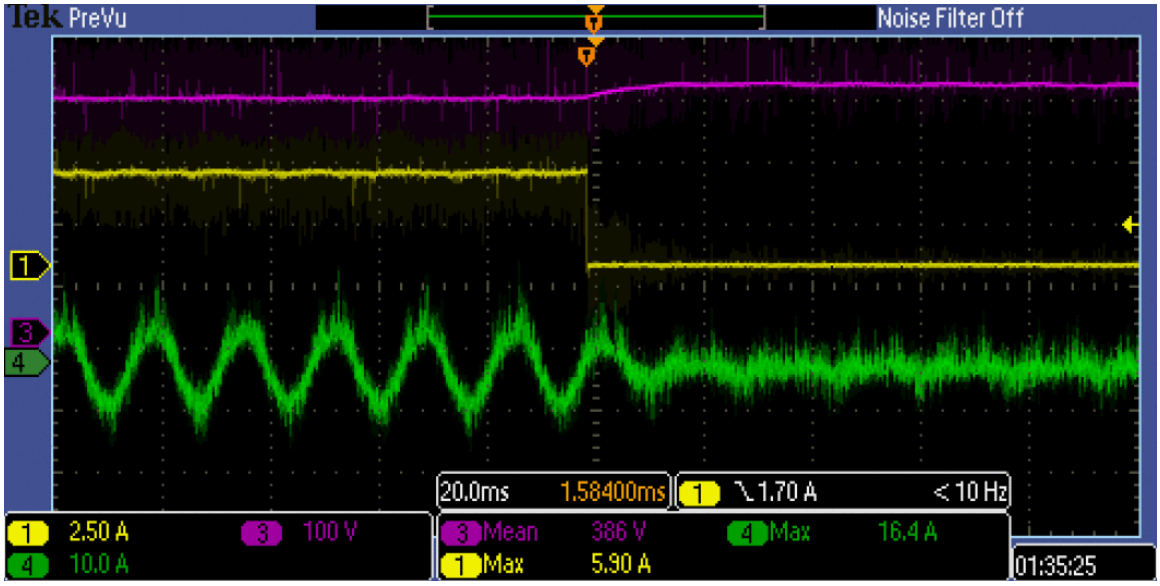

Figure 3.13: dc source input and output currents in response to a fault

results are presented in figures 3.13 and 3.14.

In Figure 3.13 plot from probe 3 shows the dc voltage which is around $375V$ before the fault. After the fault the voltage increases slightly to $390V$ because the load is disconnected from the output capacitor which is unable to instantly discharge now. Probe

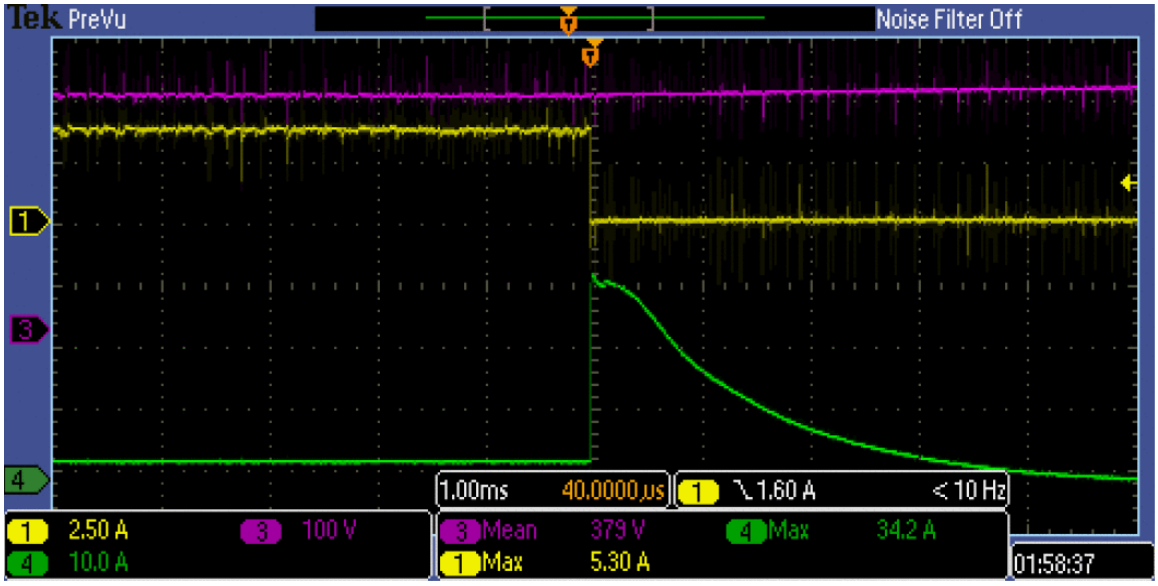

Figure 3.14: Z-source breaker input and output currents in response to a fault

1 shows the input current of the breaker which is also the output current of the source. Before the fault it is steady at around 3.8 amperes but at the fault it instantaneously goes to zero. There is no resonance and the disconnect is smooth showing the merit of this z-source breaker topology. Probe 4 shows the line current of phase A on the ac side of the system. No sign of the fault current can be seen on the ac side of the system. The current keeps charging the output capacitor for few cycles but it is completely isolated from the load.

In Figure 3.14 probe 1 shows the input current of the breaker and probe 4 shows the output current. Before the current both these currents are equal at $3.75A$. At the time of the fault the input current goes to zero instantaneously. The fault current is only seen at the output side. Fault reaches about $35A$ and then dies down. The differential protection scheme utilizes this difference in input and output current to localize the fault. Probe 3 shows the dc voltage which is at about $375V$. It does not show any sharp change at the time of the fault.

Chapter 4

Integration of Z-source breakers into zonal DC ship power system microgrids

4.1 Breaker Placement

Figure 4.1 shows one possible way to integrate Z-source breakers into the zonal distribution system. In normal operation, both breakers are energized. However, either of the breakers can be opened for maintenance without interrupting the load. Further, because the two buses at the port and starboard sides are able to support the load, the zones can be isolated from either one of them by opening the appropriate breakers. Figure 4.1 is a simplified diagram that shows only two zones. For a system with a large number of zones, the breakers can be used to implement some type of power sharing formula between the two buses.

There are several other arrangements for breaker and load placement that can offer unique advantages. For the arrangement shown in Figure 4.1, the power density is low, as there are two breakers for each zone. Using breaker and a half architecture can be explored for optimizing reliability; however, only the double breaker double bus system is considered

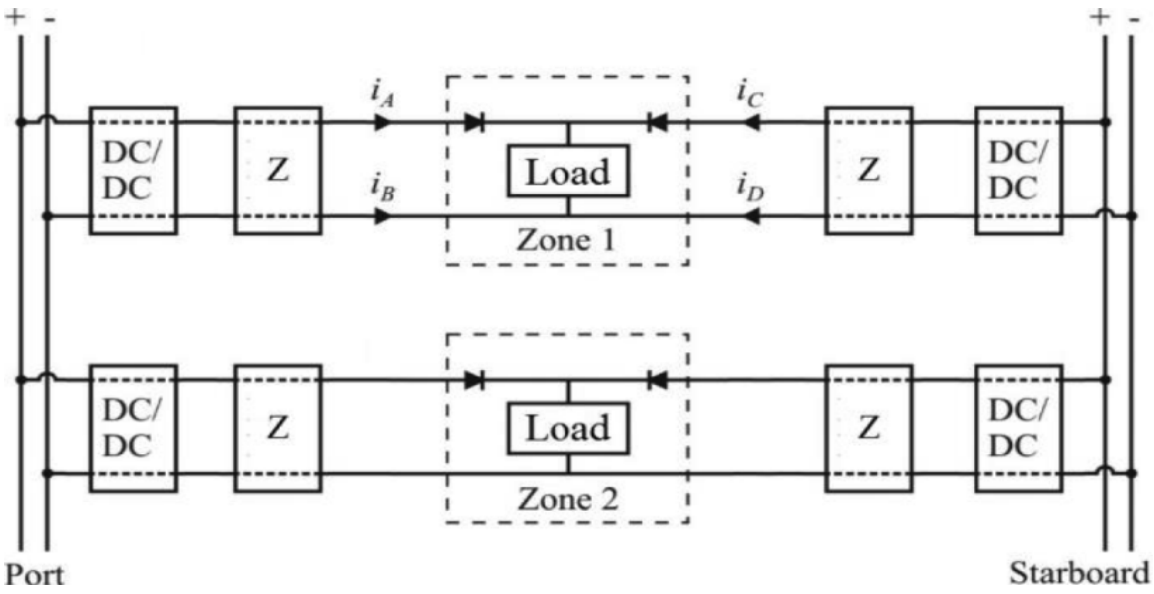

Figure 4.1: MVdc system with Z-source breakers

in this work.

Another notable feature from Figure 4.1 is that the each zone is identical in its structure. This would mean that if the response of the breakers in one zone can be studied, it would provide useful information that can be applied to the entire system. Therefore, the next part of this study will focus on one such zone. This does not imply that the zones are completely independent of each other. Energizing one zone while the other is already active might introduce some transients and there should be some filtering process to ensure that those transients are minimized. In addition, a supervisory control may be required to ensure that the other zones are not interrupted by mistaking those transients as faults.

Within a zone, there are some options present for placing the breaker with respect to the dcdc converter. The first factor to be considered is the probability distribution of fault. If a simplistic approach is used where the probability of fault per unit length of grid is uniform, then a longer transmission would mean higher probability of a fault. Therefore, if the dc converter is located closer to the bus than to the load zone, it is more likely that the fault will happen at the output of converter rather than the input side of the converter.

Carrying forward this assumption that the fault is more likely to happen at the

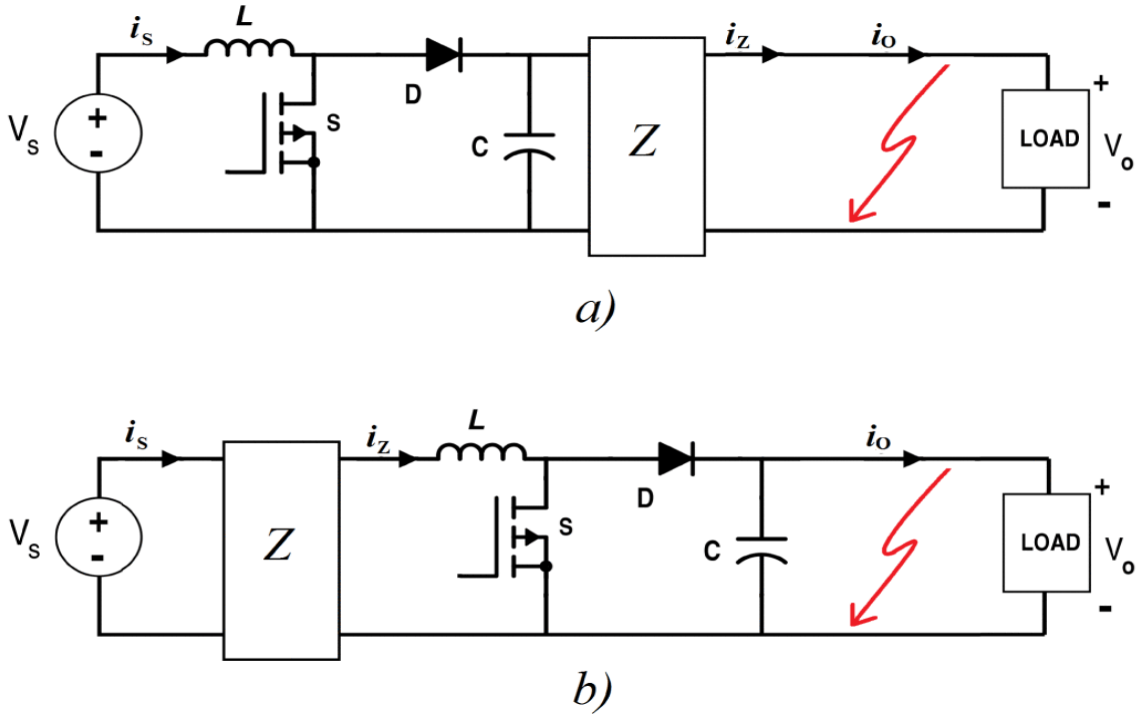

Figure 4.2: Breaker location at a) converter output and b) converter input

output end of the converter, it now remains to decide whether the Z-source breaker should be placed at the output or the input end. With any other kind of breaker, working on the principle of overcurrent detection, this might not be an important decision since the converter will be in series with the breaker. However, the Z-source breaker must be subjected to a sharp spike of current at either its input or output end in order to work, unless its supervisory control is programmed to recognize other faults. This idea is illustrated in Figure 4.2.

Figure 4.2 shows two different locations for a breaker for the same fault location. In Figure 4.2(a), the breaker would see the fault at its output and instantly force its SCR current to zero. In Figure 4.2(b), the output current seen by the breaker is i_Z, which is also the current through inductor L. For any significant value of L, the high-frequency component of fault current will not appear at the output of breaker.

To illustrate this point, consider a simulation of the system shown in Figure 4.2 with

a source voltage V_S of $315V$ and a dc/dc converter boosting it to $400V$. The load is a 50Ω resistor and a fault is created to generate five times the load current. The converter has inductance L and capacitance C of $10mH$ and $1mF$, respectively. The breaker, which is represented by the block labeled Z in Figure 4.2, has the same structure as shown in Figure 1.1 with passive components L_1, C_1, and C_2 as $1mH$, $50\mu F$ and $50\mu F$, respectively.

Figure 4.3 shows the current waveforms from the simulation results. The first plot compares the output current i_Z seen by the breaker in each case. Note that at time of the fault (i.e., $t = 1s$), the breaker in case a) sees an instant discharge by its capacitor due to fault current. In case b), the inductor L is in the path of fault current so that the output current increases gradually. The effect of instant discharge compared with gradual increase is shown in the second plot through comparing the SCR current in each case. For case a), the capacitors discharge through a current path as described in Figure 1.2 and the SCR current is forced to zero effectively open the breaker. However, in case b), the output current changes slowly so that the breakers SCR is able to provide that current through its inductor without discharging the capacitors. As a result, there is no automatic opening of breaker in this case. Therefore, the placement shown in Figure 4.2(a) should be favored.

The other factor to be considered is the topology of the converter. The Z-source breaker requires continuous flow of current for its operation, but the input of a conventional buck converter is zero during the OFF state. Therefore, a Z-source breaker cannot be used with a buck converter in the configuration shown in Figure 4.2(b) without additional input filtering. Figure 4.2(a) shows a boost converter, but the same result will hold true for a buck converter. For an MVdc system, it is more likely that a buck converter will be used between distribution bus and load. Therefore, for the remainder of the simulations, a buck converter will be used in the configuration of Figure 4.2(a).

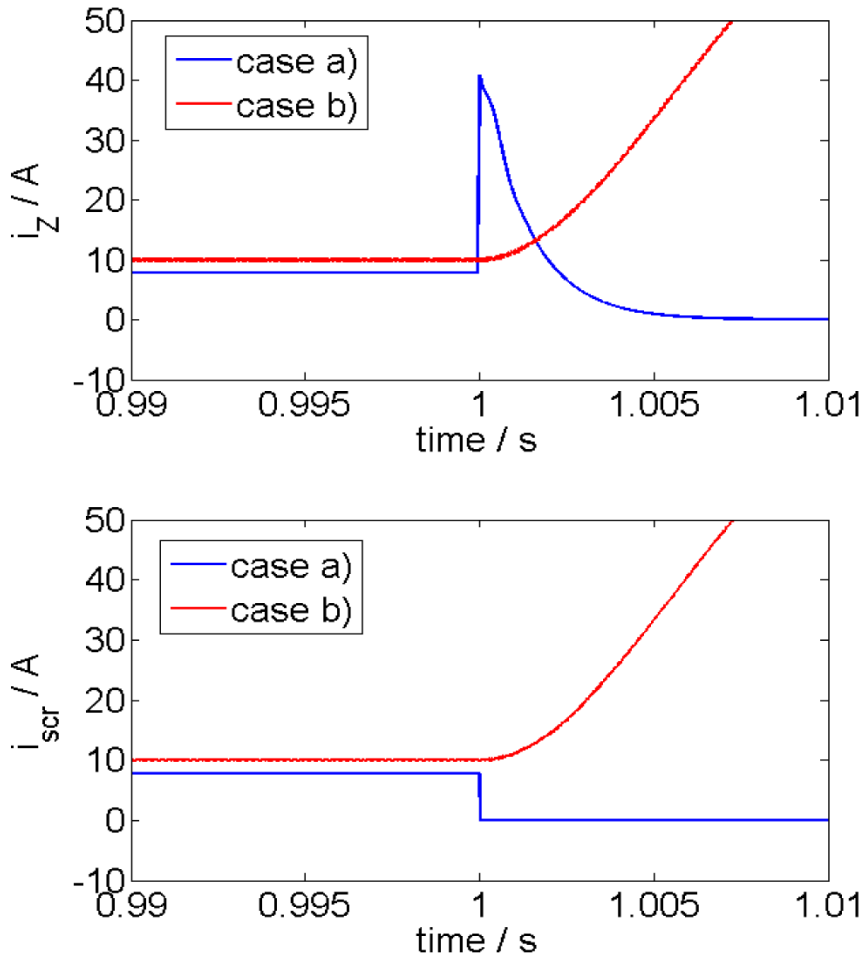

Figure 4.3: Fault response of breaker location at a) converter output and b) converter input

4.2 Effect of auctioneering diodes on Z-source breaker fault detection

4.2.1 Base case simulation

A simulation is run using just one of the zones from Figure4.1. The port- and starboard-side power is supplied from the same source. Buck converters with fixed duty cycles are used as converters and a resistive load is used. The resulting system and fault location are shown in Figure 4.4. The simulation systems specifications are summarized in Table 4.1. These specifications are selected to match the laboratory setup, which is

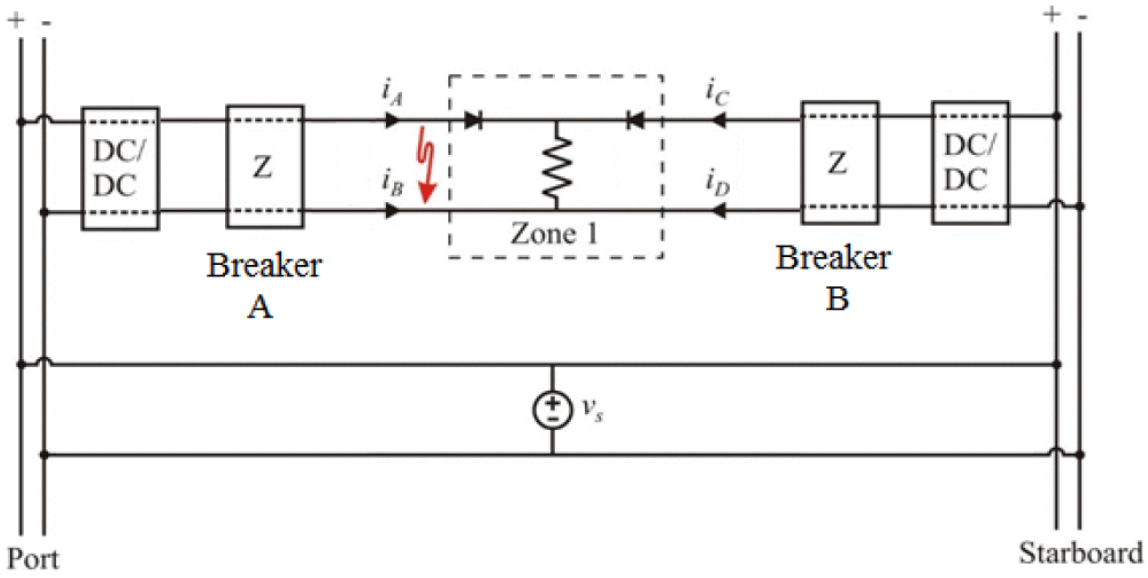

Figure 4.4: Single zone system for simulation and lab setup

Source voltage	**Buck converter output**	**Nominal load current**	**Expected breaker current**	**Threshold breaker fault current**
$315Vdc$	$200Vdc$	$4A$	$2A$	$6A$

Table 4.1: Simulated system specifications

presented in the next section.

Initially, the SCRs in both breakers are provided gate signals, allowing them to conduct. Once the system is steady at around $t = 0.5s$, the gate signals are removed. A fault is created at the location shown in Figure 4.4 at time $t = 1s$. In response to the fault, both of the breakers open. The resulting current and voltage waveforms from the fault simulation are shown in Figures 4.5 to 4.7. Figure 4.5 shows the waveforms labeled in Figure 4.4. Figures 4.6 and 4.7 show the currents and voltages labeled in Figure 1.1 for breakers A and B, respectively. The common feature between the current waveforms of breakers A and B is the SCR current dropping instantly to zero. For breaker A, the fault is right across its output so that the capacitors discharge faster and the transient current through inductors is higher compared with breaker B. The fault is isolated from the system;

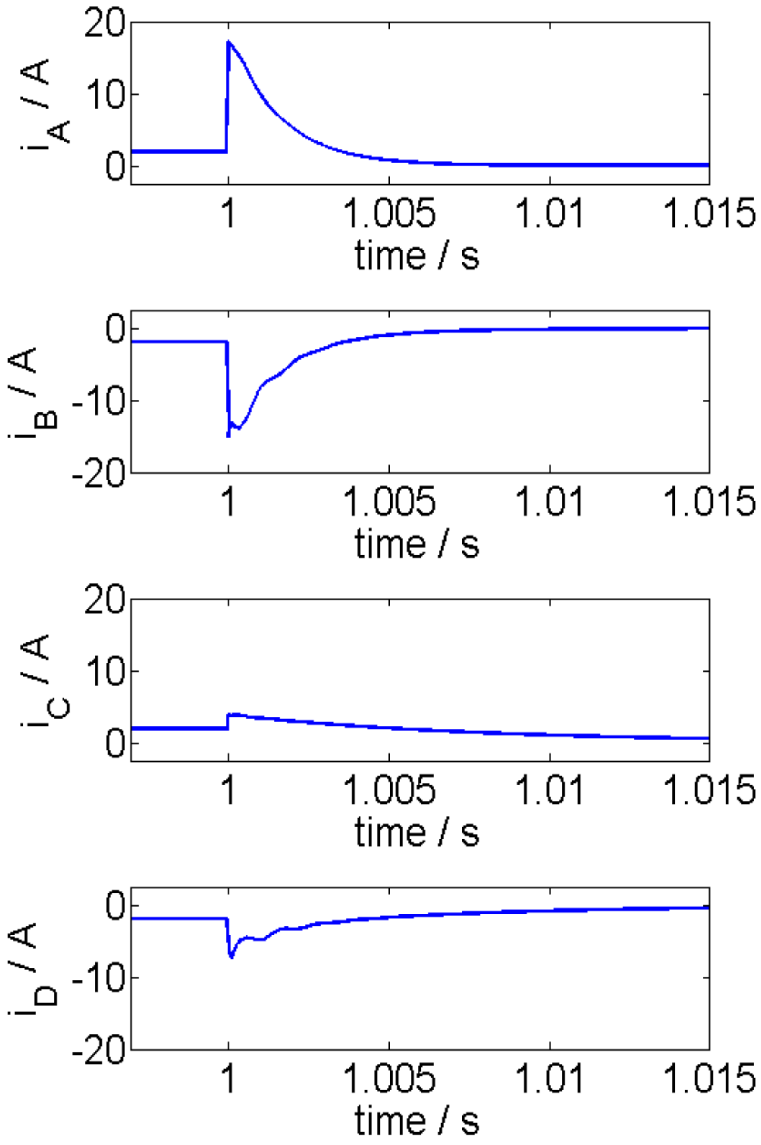

Figure 4.5: Output current waveforms from the simulation

however, this is not the optimum response. Note that due to the presence of the diodes, zone 1 can continue to receive power from starboard side without feeding the fault. Only the breaker at port side needs to be open to isolate the fault from the source. In order to achieve the optimum response using Z-source breakers, one of the following two approaches can be used.

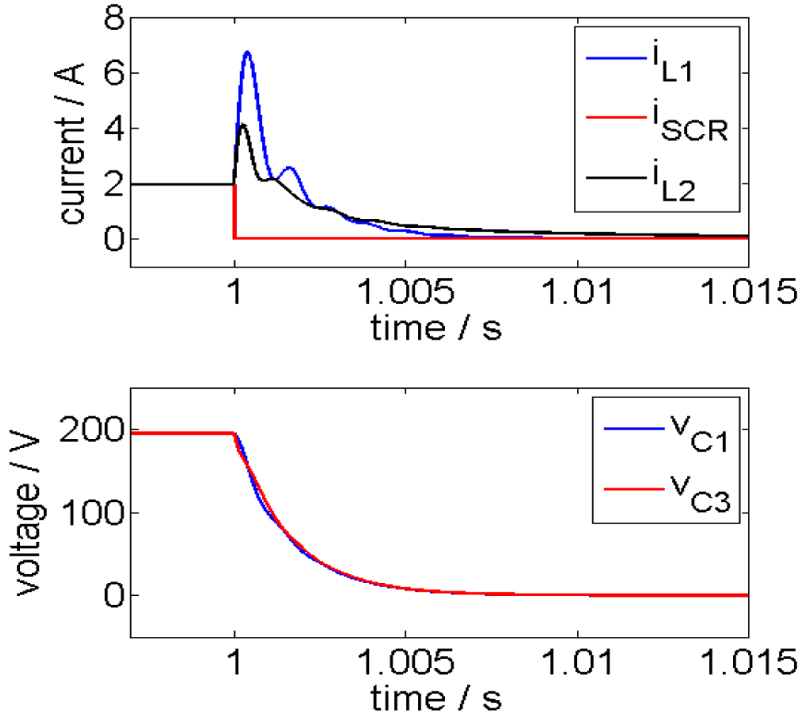

Figure 4.6: Breaker A current and voltage waveforms

4.2.2 Addition of Negative rail diodes

For the system shown in Figure 4.4, neither the Z-source breakers nor the dc/dc converters provide galvanic isolation. This means that there is an electric path from the negative rail of starboard bus to the negative rail of the port bus. This could lead to circuitous current in the system in the case of transients such as a shunt fault. For the fault location shown in Figure 4.4, the path of circuitous fault current is traced and shown in Figure 4.8. The source of this current is the capacitor at the output of the buck converter on the port side of system. The capacitor at the output of buck converter on the starboard side does not see the fault due to blocking diodes. The discharge path of the capacitor creating this circuitous current includes the inductors of Z-source breakers.

The initial injection of this circuitous current in the negative rail of starboard side Z-source causes the SCR in its positive rail to be reverse biased and the current through it falls to zero instantly. One way to prevent this from happening is to block this current

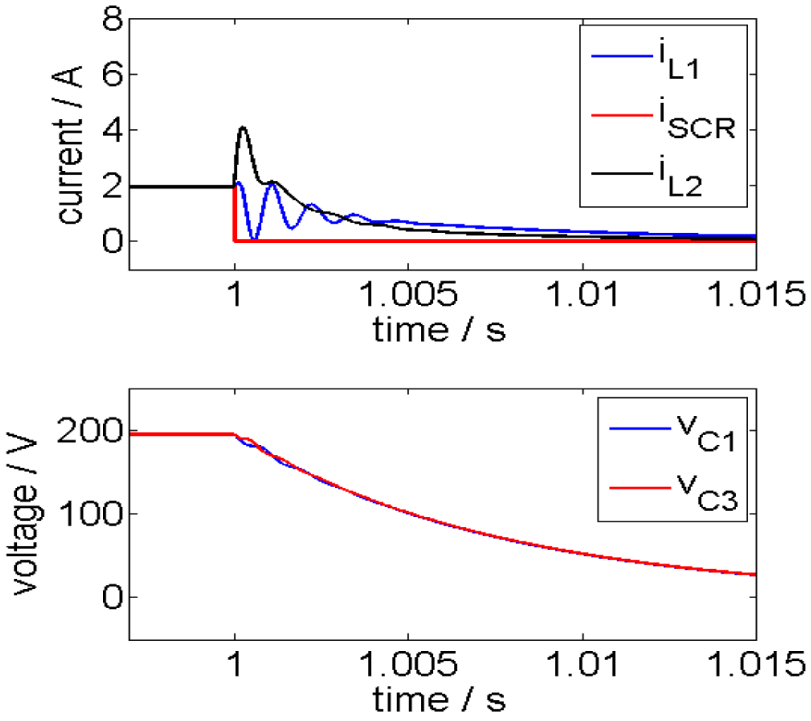

Figure 4.7: Breaker B current and voltage waveforms

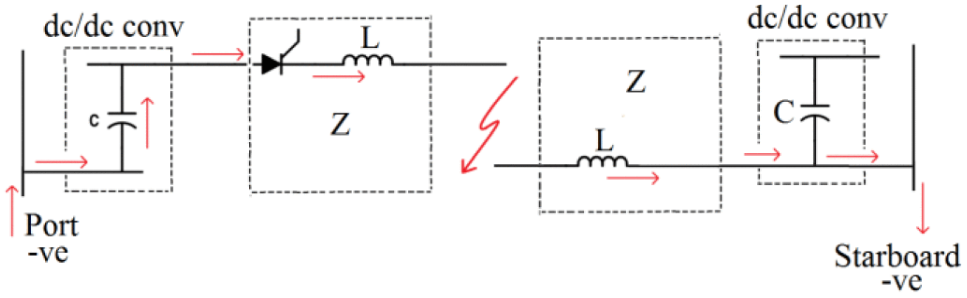

Figure 4.8: Path of circuitous fault current

path using a diode. Another diode should be added to block the path of circuitous current in case the fault occurs at the starboard side. The resulting system with two additional diodes is shown in Figure 4.9. The diode labeled X will block the circuitous current without blocking the current for normal operation.

The system in Figure 4.9 is simulated for the fault location shown. Only the breaker at the port side opens. The resulting transient current waveforms are shown in Figure 4.10. It can be seen that there is no large spike in current for either i_C or i_D. This means that the

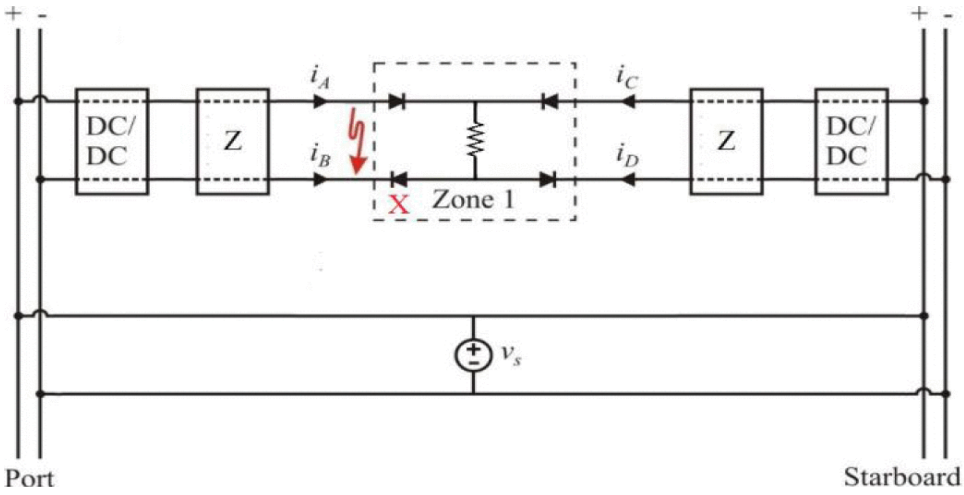

Figure 4.9: Simulated system with additional diodes on the negative rail

injection of capacitive discharge from the port-side converter to the starboard-side breaker has been blocked. As a result, the starboard-side breaker is prevented from opening. The system reaches steady state in about $0.25s$. It can be seen that after the fault, the current through i_C doubles to compensate for loss of power from the port side. The return path is divided equally between i_B and i_D.

4.2.3 Fault location detection

The additional diodes in the system are in the path of the steady-state current so that it would introduce some power losses. Another way to achieve optimum results using Z-source breakers is discussed in this section. Figure 4.5 shows that both of the breakers open even though the output currents differ significantly. There is a large spike in i_A and i_B feeding the fault current caused by the capacitive discharge of the shunt capacitance in the Z-source breaker. In contrast to that, the breaker on the starboard side has only a large increase in current for its negative rail current i_D. The current i_C shows some increase, but compared with the steady-state current, it is only a slight change.

With this information known, the fault location can be determined by comparing the current with a preset threshold. The threshold value should be about four to five times

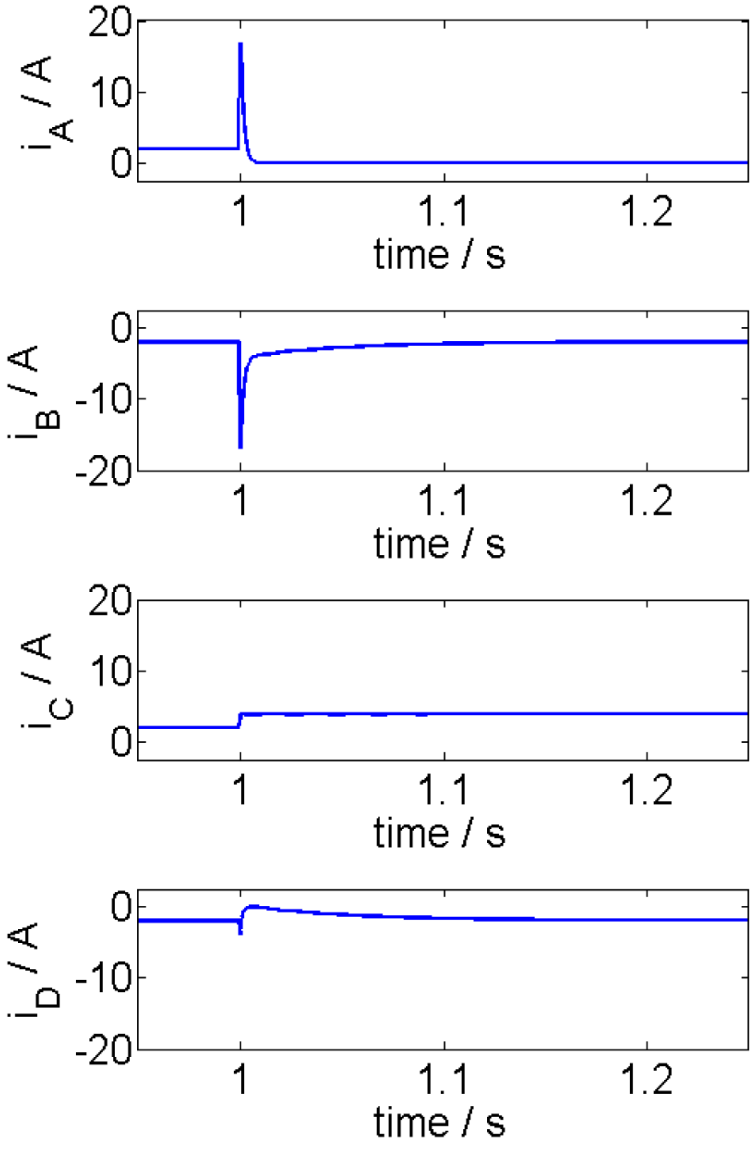

Figure 4.10: Current waveforms of simulated system with additional diodes on the negative rail

the steady-state current. If both positive and negative rail currents exceed that threshold, it can be concluded that the fault is at the output terminals of the breaker and no action is necessary. However, if only the negative rail current exceeds that threshold, a flag will be set indicating that the breaker turned OFF due to a circuitous current and should be reclosed after a reasonable settling time. Table 4.2 presents the summary of required actions for fault locations simulated in locations shown in Figure 4.11.

Fault Location	Port Breaker current response	Starboard breaker current response	Control Action
A	Both output current exceed threshold	Only negative rail current exceed threshold	Close Starboard side breaker after time T
B	Both output current exceed threshold	Both output current exceed threshold	No action required
C	Only negative rail current exceed threshold	Both output current exceed threshold	Close Starboard side breaker after time T

Table 4.2: Control action summary

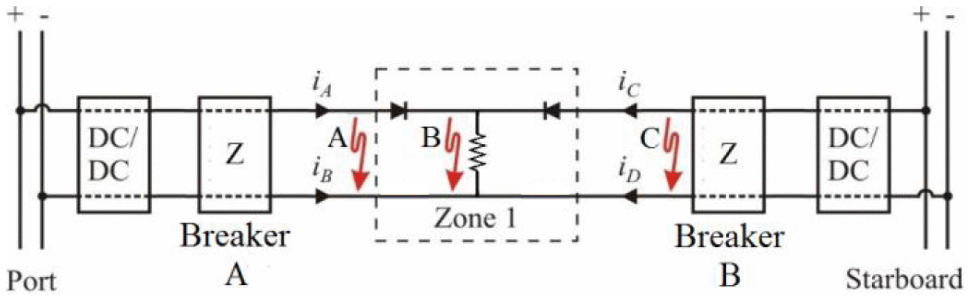

Figure 4.11: Likely fault locations

The advantage offered by this approach is higher efficiency during normal operation. The disadvantage is that the power to the load is interrupted for some time before being restored. It is therefore important to categorize the loads as critical or noncritical. This approach should be preferred for noncritical load that can afford a small interruption in power without harming ships operation or a high current load where efficiency is a critical factor.

The simulation results for one of the cases are shown in Figure 4.12. A delay of $0.15s$ is simulated to match the laboratory setup. The reclosing transients can be observed in the output current waveforms shown in Figure 4.12.

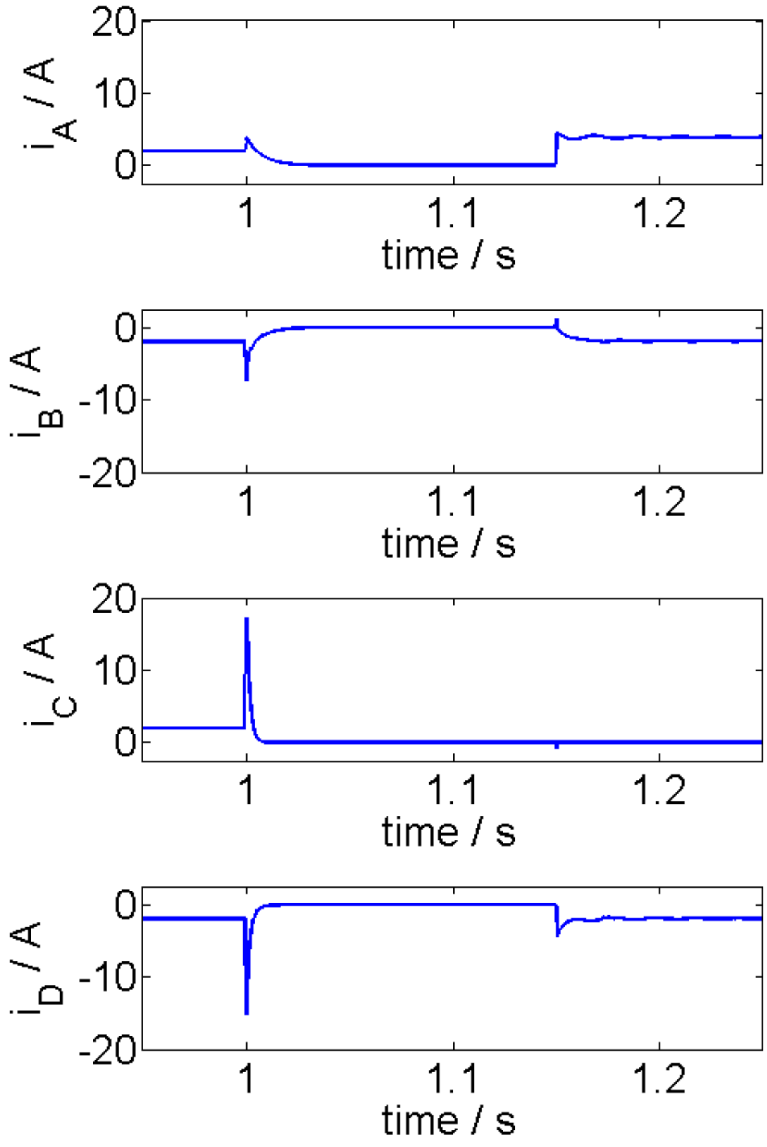

Figure 4.12: Current waveforms from simulation of fault and reclosing the breaker

4.3 Hardware results

To verify the role of auctioneering diodes, circuitous currents and their effect on fault location, the systems of Figures 4.4 and 4.9 are assembled in the lab. The breaker box describe in the previous chapter is used for the Z-source breaker. the design specification for that are provided in Table 3.4. For dc/dc converters, two simple buck converters are designed and assembled. The specifications for these buck converters are provided in Table

Inductor	Capacitor	Base load	Switching device	Switching frequency
$2.2mH$	$200\mu F$	$2k\Omega$	IGBT module	$10kHz$

Table 4.3: Buck converter specifications

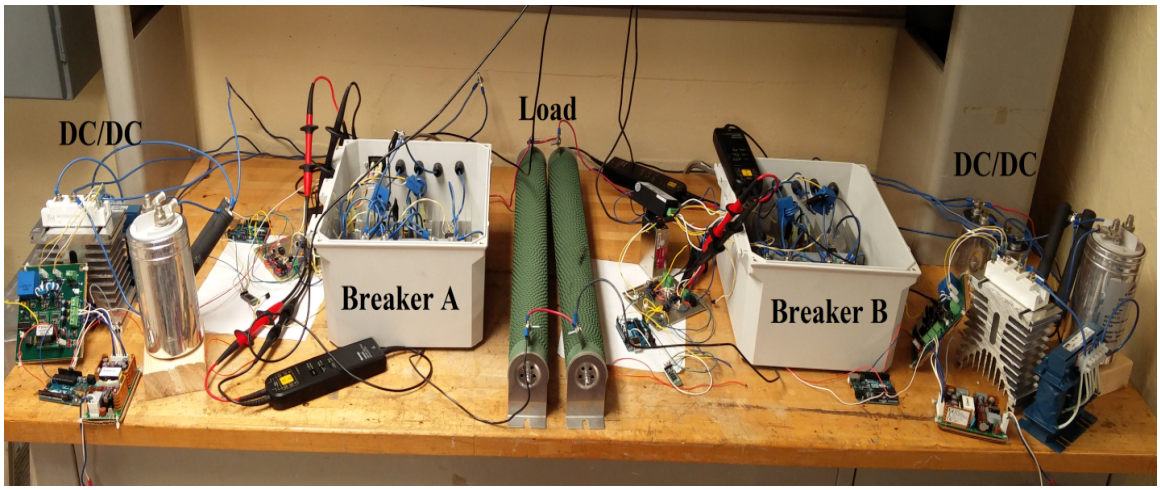

Figure 4.13: Laboratory setup with prototype breakers and dc/dc converters

4.3. Figure 4.13 shows the lab setup for these experiments. All experiments are obtained at converter input voltage of $220V$, output voltage of $150V$ and load of 50Ω.

Figure 4.14 shows the current waveforms corresponding to the laboratory setup where additional diodes are used to block circuitous current. The resulting waveforms look similar to the results in Figure 4.10. The positive and negative rail currents are balanced. Only the breaker at the starboard bus opened and the current through the positive rail of the other breaker doubled to compensate for it.

To verify the approach of fault location detection, the output currents of both breakers are measured using Hall effect sensors. The outputs of those sensors are compared with a set threshold voltage using analog comparators. Once a current crosses the threshold, the state is locked to indicate that a fault has occurred. The gate control device for each breaker will communicate this information to a central control. Based on the summary from Table 4.2, the central controlling device decides the appropriate action and sends the information back to the gate control device.

Figure 4.15 shows the current sensors outputs corresponding to the current wave-

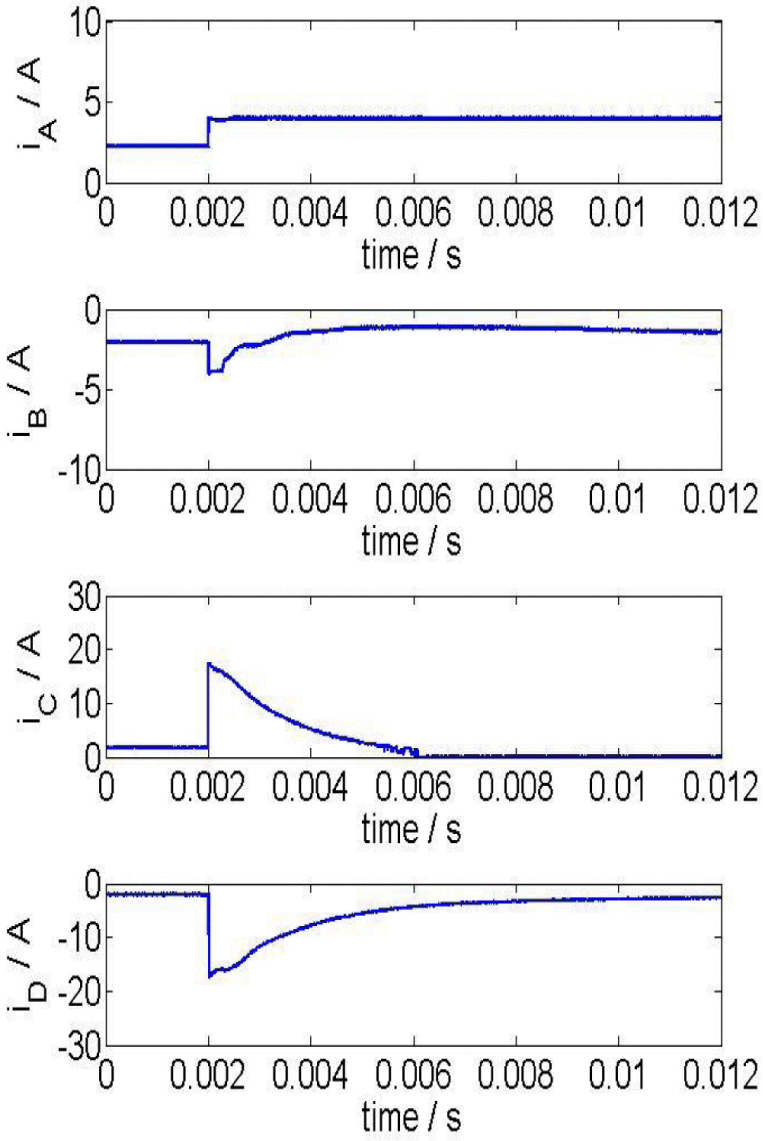

Figure 4.14: Current waveforms for lab setup with additional diodes in negative rail

forms when the fault is created at location C from figure 4.11. It can be seen that initially both breakers turn OFF and this part of waveform is similar to Figure 4.5. After some settling time, the breaker at port side closes and starts conducting again. The return path of the current is shared between the two breakers.

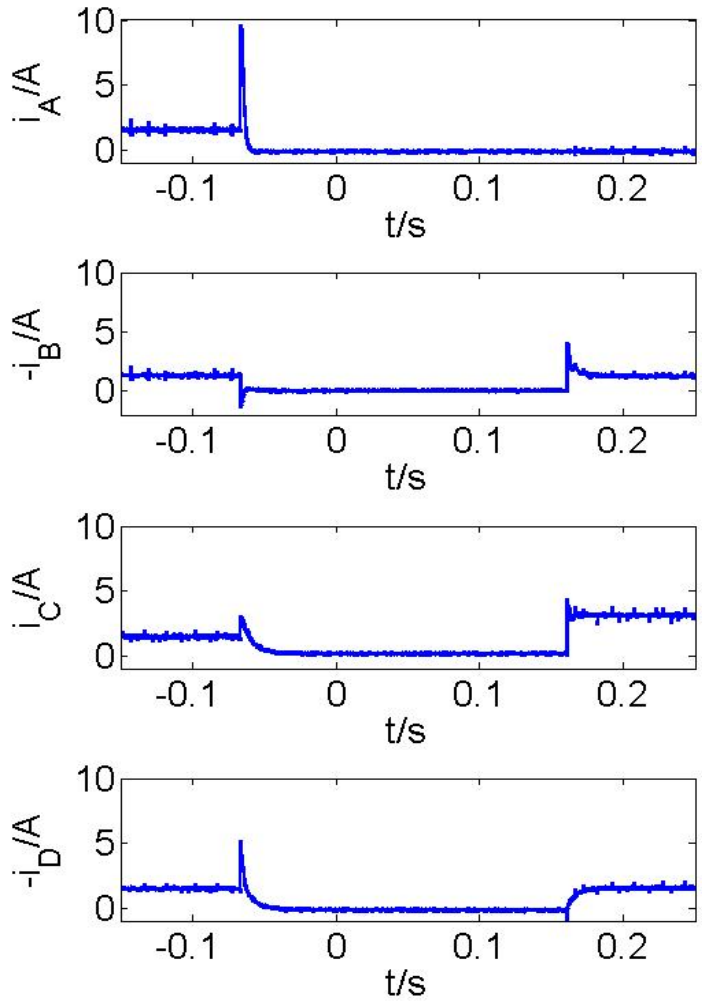

Figure 4.15: Current sensor outputs corresponding to the output current waveforms for the lab setup and fault at location C

Chapter 5

Conclusion

The Z-source breaker has emerged in recent years as a solid-state breaker that is capable of automatically and rapidly opening in response to a fault. Modifications have been made to the design to allow for a common ground and improve the voltage transfer function. This work introduces variations on the designs that also allows for step changes in load. That is, the proposed breaker designs will not mistake a step change in load for a fault. Several new designs are introduced. The voltage transfer functions are analyzed. A method has been outlined for designing the components to achieve certain goals. Simulation and laboratory measurements demonstrate the proper operation of the new designs.

This work also explores the use of coupled inductors in a z-source dc circuit breaker. The coupled design reduces the inductor by weight 30% and the inductor volume by about 25%. Furthermore, with coupled inductors, one of the capacitors in the z-source breaker can be removed. Therefore, the size and weight of the breaker can be considerably reduced. Simulations were carried out comparing two designs to demonstrate the advantage of using coupled inductors in z-source breakers.

Use of the solid-state z-source breaker in a notional dc ship power system has been explored. The z-source breaker, system topology, and control unit were briefly described. Improvements to the z-source breaker topology have been introduced. The new z-source breaker design allows reclosing and this is utilized in the breaker coordination control. Sim-

ulations of the system and control show correct operation for a number of fault locations. Considering future implementation, practical issues related to communication and data processing, are briefly addressed. Furthermore, a design for a low-voltage dc grid is presented. This dc grid will serve as a test bed for different designs and protection schemes involving z-source breakers. A wireless communication architecture based on Bluetooth data transfer is established to allow central remote control of multiple breakers. Preliminary results from the dc source and z-source breaker box are presented.

The final chapter addresses the practical problems of integrating Z-source breakers into a zonal dc microgrid. The placement of breakers with respect to converter type and converter location is presented. A system of two breakers feeding a load is simulated. The fault current is shown to force SCRs in both breakers to turn OFF, hence opening both breakers. This is a result of circuitous current and two methods are suggested to overcome it. One approach is adding diodes in the negative rail, which blocks the path of the circuitous current. The other approach involves monitoring the currents and locating the fault. Both methods are demonstrated through simulation and a low-voltage experimental setup.

Appendices

Appendix A Detailed derivation for minimum fault resistance

A shunt fault occurs at $t = 0$ introducing a small shunt resistance of R_f . Capacitor C_Z is initially charged to source voltage V_S . Assuming R_f to be significantly smaller than R_{load}, expression for v_{out} is approximated as

$$v_{out}(t) = V_S e^{-At} \tag{1}$$

where A is inverse time constant for load capacitor discharge through fault resistance

$$A = \frac{1}{R_f C_{load}} \tag{2}$$

Also with voltages as defined in Figure 2.20

$$-C\frac{dv_Z}{dt} = \frac{v_Z - v_{out}}{R_Z} \tag{3}$$

The expression for $v_Z(t)$ is derived using Laplace transform analysis of 3

$$v_Z(t) = \frac{V_S}{B - A}(Be^{-At} - Ae^{-Bt}) \tag{4}$$

where B is another inverse time constant based on RC network of the Z-source breaker

$$B = \frac{1}{(R_1||R_2)(C||(C_1 + C_2))} \tag{5}$$

In response to a step change in load, the transient impedance of C_1 and C_2 would be very small compared to the series resistors R_1 and R_2 . So, only the resistors determine the total impedance in each branch initially. The current expressions in 6 and 7 are derived using this assumption, as well as the earlier assumption of keeping C_1 and C_2 of similar values.

$$i_Z(t) = \frac{v_Z - v_{out}}{R_1||R_2} \tag{6}$$

$$i_{C2}(t) = \frac{v_Z - v_{out}}{R_2} \tag{7}$$

This expression for i_{C2} is valid for a very small time only whereas the impedance of capacitors is still small however it helps to simplify the analysis. By taking the derivate of 7, equating it to zero and solving it for time, the following expression for t_{max} is obtained:

$$t_{max} = \frac{log\left(\frac{A}{B}\right)}{A - B} \tag{8}$$

After time $t = t_{max}$, $i_{C2}(t)$ will start decreasing, so, if the breaker is able to interrupt the fault it will always do so at or before this time. One of the conditions to turn OFF the SCR is that the current through it must fall to zero. Looking at Figure 2.5 and applying KCL at SCRs cathode shows

$$i_{SCR}(t) = i_{C2}(t) - i_{L2} \tag{9}$$

For this transient analysis, i_{L2} is assumed to stay constant at prefault value of load current. In this case:

$$i_{L2} = \frac{V_S}{R_L} \tag{10}$$

where R_L is load resistance.

Substituting t in 7 with t_{max} from 8 gives the expression for maximum current that flows out of capacitor C_2 during the transient.

$$i_{C2max} = \frac{V_S}{R_2}\left(\frac{A}{B}\right)^{\frac{B}{B-A}} \tag{11}$$

The current i_{C2max} must be greater than or equal to i_{L2} in order to force the SCR current to zero as shown in 9. To turn OFF the SCR, the following equality must hold true when comparing 10 with 11:

$$\left(\frac{A}{B}\right)^{\frac{B}{B-A}} > \frac{R_2}{R_L} \tag{12}$$

Substituting A in 12 by formula for A in 2, the following condition is obtained for the breaker to trip:

$$R_f < \frac{ln\left(\frac{R_2}{R_L}\right)}{C_L B \mathbf{W}\left(\frac{R_2}{R_L} ln\left(\frac{R_2}{R_L}\right)\right)} \tag{13}$$

where **W** represents the product log or Lambert function.

Appendix B Z-source breaker sizing to demonstrate effect of coupling

B.1 System parameters

System Power = $P_S = 60kW$

System voltage = $V_S = 600V$

Current = $I_S = P_S/V_S$

radius of wire = $a = \frac{\sqrt{I_S/kA}}{2} inch$

radius of solenoid = $R = 5inch$

cross sectional area of wire = $A_{cu} = \pi a^2$

Density of copper = $D_{cu} = 8.92gm/cm^3$

B.2 Inductor size without coupling

Number of turns = $N = 23$

Length of wire = $L_{cu} = 2\pi RN$

Volume of wire = $V_{cu} = A_{cu}L_{cu}$

Mass of two inductors = $2M_{cu} = 2D_{cu}V_{cu} = 16.3kg$

Width of inductor = $W_L = 2R + 4a$

Height of inductor = $H_L = N(2a)$

For the cabinet volume the capacitor and SCR size has been ignored because of the high mass of inductors.

Margin width = $cc = 1inch$

Width of cabinet = $W = W_L + 2cc$

Depth of cabinet = $D = W$

Height of cabinet = $H = 2H_L + 2cc$

Volume of cabinet = $vol = WDH = 43.3ltr$

B.3 Inductor size with coupling

Number of turns = $N_2 = \frac{N}{\sqrt{2}}$

Combined number of turns = $N_3 = 2N_2$

Length of wire = $L_{cu} = 2\pi RN_3$

Volume of wire = $V_{cu} = A_{cu}L_{cu}$

Mass of combined inductors = $2M_{cu} = 2D_{cu}V_{cu} = 11.7kg$

Width of inductor = $W_L = 2R + 4a$

Height of inductor = $H_L = N_3(2a)$

Margin width = $cc = 1inch$

Width of cabinet = $W = W_L + 2cc$

Depth of cabinet = $D = W$

Height of cabinet = $H = 2H_L + 2cc$

Volume of cabinet = $vol = WDH = 32.1ltr$

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