Project Description

Design a 5-section (N=5) stepped-impedance maximally-flat microstrip low-pass filter with

capacitor input, cutoff frequency assigned to your group, 50 Ω system.

Use 6mm long 50 Ω feed lines to connect the input and output of your filter (for SMA connection) Verify your design with ADS.

Design Guidelines:

Substrate type: Rogers 4350B ; H (substrate thickness)=1.524 mm

E_r=3.66 ; Mu_r=1

Cond (copper)=5.88e7 T(Thickness of metal)=35 um

TanD=0.0032 Z_{H} =120 Ω , Z_{L} =20 Ω

- a) Design and optimize your filters in ADS schematics and measure S parameters.
- b) Round all final width and length values to 0.01 mm before generating layout (Ex: 5.878mm \rightarrow 5.88mm)
- c) Generate the layout and compare the EM results with schematic.
- d) Export the gerber files of layout and zip them.
- e) Zip file name: Same as labeling (slide 4)



Labeling

Write Group Number and participants initials on the top left corner of board with "silkscreenTop" layer and font size of 1.5 (or the largest that fits)

Example:

If Group #1 participants are Ronald Reagan and John Kennedy, they should label their PCB as: G1_RR_JK

Make sure the label text does not touch any of the metal traces and lies inside the board shape.

Your board shape is defined by the area covered by cond2 (bottom ground plane) rectangle.

Layers Configuration and Use (Important)

Follow these steps when you create a new workspace to make sure all required fabrication layers are present in the design and ready to export

Creating layout in PCB-ready format (1)

Click on File -> New ->Workspace



Creating layout in PCB-ready format (2)

• Select Create PCB technology and click on Next

	🕰 Choose Layout Technology	\times
	Choose Technology for library: 163DA_layout_lib You may cancel. If you do, you will be prompted again when you create a layout or substrate.	
Select this	Add library/PDK., Create PCB Technology Standard ADS Layers, 0.0001 millimeter layout resolution Standard ADS Layers, 0.001 micron layout resolution Custom (opens new Technology dialog) Don't setup layout technology now (cancel)	
	Copy technology into new library instead of referencing it	
	< Back Next > Cancel Help	

Creating layout in PCB-ready format (3)

Select the options indicated and click on Next

	Choose Layout Technology	×
	PCB Layout Technology Setup - Basic Set up units, resolution, and basic board stack parameters	
Select these options	Layout units: millimeti v (change resets all values to default) Layout resolution: 100 v database units per millimeter Number of metal layers: 2 v Center slab of board is core (not prepreg) v Include solder mask and paste	
	☐ Include top cover Height: 25 millimei ∨ ☐ Include bottom cover Height: 25 millim ∨	
	<pre> Click nere < Back Next > Finish Cancel Help </pre>	

Creating layout in PCB-ready format (4)

• Select the options indicated and click on Next

<mark> Choose Layout Tec</mark> l	nnology				×
PCB Layout Technolo Choose materials u	gy Setup - Mate ised in PCB substra	e rials ate			
Dielectric Materials:					
Solder mask material:	SolderMask ~]	Thickness:	0.01	millimeter \lor
Core material:	Rogers4350B 🗸		hickness:	1.6	millimeter $\!$
Conductor Materials	C	lick	here		
Outer metal material:	Copper ~	·]	Thickness:	35	micron ~
Solder paste material:	Typical_solder \sim	·]	Thickness:	1.0	mil v
< Back	Next >		Finish	Cancel	Help

Creating layout in PCB-ready format (5)

• Select the options indicated and click on Next

Conductors	Dielectrics	Se	miconducto	ors Surfac	e Roughness		
Ma	terial			Permittivity (Er)	Permea	bility (MUr)
Aaterial Nam	Library	/	Real	Imaginary	TanD	Real	Imaginar
FR_4_Core	Test_lib		4.6		0.01	1	
FR_4_Prepreg	Test lib		4.6		0.01	1	
Rogers4350B	Test_lib		3.66		0.003	1	
SolderMask	Test lib		3.3			1	

Define Your Desired Substrate

Creating layout in PCB-ready format (6)

• Select the options indicated and click on Next (You can modify later in layout sub stack)

	Choose Layout Technology × PCB Layout Technology Setup - Materials Choose materials used in PCB substrate	
Set These Options	Dielectric Materials: Solder mask material: SolderMask Core material: Rogers4350B Rogers4350B Thickness: 1.524 millimeter Conductor Materials: Outer metal material: Copper Thickness: 35 micron Solder paste material: Typical_solder Thickness: 0.01 Micron Help	Board Thickness Copper Thickness

Creating layout in PCB-ready format (7)

Click on Finish

Default Via Para	meters:			
Via template name	e: round]	
Pad diameter:	1.25	millimeter ~]	
Drill diameter:	0.5	millimeter v]	
Make EM-style	stackable drills			

Creating layout in PCB-ready format (8)

- Now you have defined PCB tech, you do not need to choose anything when placing MSUB in schematics.
- Your substrate stack in layout should look like the picture below.
- Modify the conductors thickness, conductors conductivity, dielectric constant, dielectric TanD, and etc., in both layout stack and schematic (according to your design), if necessary.



Creating layout in PCB-ready format (9)

• Your available layout layers should look like this:

Layers you need to export are listed below

- cond
- cond2
- solderMaskTop
- solderMaskBottom
- silkscreenTop

Layer	Fill	Sel	Vis
silkscreenTop		\sim	\checkmark
solderMaskTop		 Image: A set of the set of the	
solderPasteTop		\checkmark	 Image: A set of the set of the
cond		\checkmark	
cond2		\checkmark	 Image: A set of the set of the
solderPasteBottom		\sim	 Image: A set of the set of the
solderMaskBottom		\sim	\checkmark
silkscreenBottom			 Image: A set of the set of the
cond_cond2		\sim	\checkmark
boardBound		\sim	\checkmark
silk_screen		\checkmark	 Image: A set of the set of the
silk_screen2		\sim	\checkmark
scratch		\sim	\checkmark
ads_y8		\checkmark	 Image: A set of the set of the
ads_drc_error		\checkmark	\checkmark

Important guidelines about use of layers (1)



- You are going to fabricate a 2-layer PCB having top and bottom layers
 - Your design should be done using the top layer (cond in ADS)
 - The entire bottom layer (cond2 in ADS) should act as the ground plane. This can be done by drawing a rectangle using the cond2 layer covering the entire PCB layout

Important guidelines about use of layers (2)



- The solderMaskTop(Bottom) layer covers the parts of the top(bottom) layer where the conductor is to be exposed
 - The **solderMaskTop** layer should cover your entire cond layer
 - solderMaskBottom layer should cover the entire cond2 layer of the PCB
 - In summary, cond2, solderMaskTop, and solderMaskBottom are aligned rectangles of the same dimension that define and cover the board shape. This is to expose all metals and enable soldering SMA connectors.

Important guidelines about use of layers (3)

silkscreenTop	\checkmark	\checkmark	1. 1. 1.
solderMaskTop	\checkmark	\checkmark	
solderPasteTop	\checkmark	\checkmark	
cond	\checkmark	\checkmark	
cond2	\checkmark	\checkmark	
solderPasteBottom	\checkmark	\checkmark	
solderMaskBottom	\checkmark	\checkmark	
silkscreenBottom	\checkmark	\checkmark	
cond_cond2	\checkmark	\checkmark	
boardBound	\checkmark	\checkmark	
silk_screen	\checkmark	\checkmark	

- The silkscreenTop(Bottom) layers are non-conductive epoxy ink layers used for writing text or other information on the PCB
- You should write labelling on the top left corner of your PCB using the silkscreenTop layer

Planning for use of SMA edge connectors





- SMA edge connectors (top left) will be directly soldered to each of the ports of your PCB for the purpose of measurement. You do not need to add pads to your layout.
 - This is the reason metals are left exposed by adding solder mask layers.

Sample Layout (Important)

Layout Considerations



Port Assignment (Important)

More Accurate EM Simulation

- Place two ground pins in layout on the cond2 layer for each port (both sides of the signal pins, around **0.5mm** far from the signal port)

- Make sure ports are touching the metals (bring them inside) and are in a symmetric fashion
- This is called GSG (Ground-Signal-Ground) Port



▫┎♤♤▭

V,s cond:drawing

on your designs.

Using this icon enables you to easily place pins

When you place a pin, position the cursor

directly on the end of the instance-pin or wire

Insert Pin

 \sim

Defining GSG ports

- Go to -> Port Editor

- Drag ground ports from the bottom and drop them on the Gnd of your signal ports at top
- This is how it looks like after (also in EM setup):
- Run EM simulations
- If result does not look smooth and uniform, especially at higher frequencies, try Momentum Microwave and increase Mesh density.



Port Editor

Number	Gnd Layer	Name	Feed Type	Ref Impedance [Ohm]	Ref Offset [mm]	Term Type		
~ 1 1	N/A	P1	Auto	50 + 0i	N/A	inputOutput		
O P	1							
ΦP	3							
ΦP	1							
v 🎎 2	N/A	P2	Auto	50 + 0i	N/A	inputOutput		
O P.	2							
• P.	5							
P	5							
ayout Pins								
ayout Pins	Layer		Net	Connected to	Purpose	X [mm]	Y [mm]	Num
Name	Layer		Net P1	Connected to 1(+)	Purpose drawing	X [mm] 0	Y [mm] 0	Num 1
Layout Pins Name ○• P1 ○• P2	Layer cond cond		Net P1 P2	Connected to 1(+) 2(+)	Purpose drawing drawing	X [mm] 0 45.81	Y [mm] 0 0	Num 1 2
Name Name P1 P2 P3	Layer cond cond cond2		Net P1 P2 P6	Connected to 1(+) 2(+) 1(-)	Purpose drawing drawing drawing	X [mm] 0 45.81 0.1	Y [mm] 0 0 3.7	Num 1 2 3
Name • P1 • P2 • P3 • P4	Layer cond cond cond2 cond2		Net P1 P2 P6 P6	Connected to 1(+) 2(+) 1(-)	Purpose drawing drawing drawing drawing	X [mm] 0 45.81 0.1 0.1	Y [mm] 0 0 3.7 -4.5	Num 1 2 3 4
Layout Pins Name • P1 • P2 • P3 • P4 • P5	Layer cond cond2 cond2 cond2 cond2		Net P1 P2 P6 P6 P6	Connected to 1(+) 2(+) 1(-) 1(-) 2(-)	Purpose drawing drawing drawing drawing drawing	X [mm] 0 45.81 0.1 45.7	Y [mm] 0 0. 3.7 -4.5 4.2	Num 1 2 3 4 5
Layout Pins Name ○• P1 ○• P2 ○• P3 ○• P4 ○• P5 ○• P6	Layer cond cond2 cond2 cond2 cond2		Net P1 P2 P6 P6 P6 P6 P6	Connected to 1(+) 2(+) 1(-) 1(-) 2(-) 2(-)	Purpose drawing drawing drawing drawing drawing drawing	X [mm] 0 45.81 0.1 0.1 45.7 45.7	Y [mm] 0 3.7 -4.5 4.2 -4.8	Num 1 2 3 4 5 6
Aayout Pins Name • P1 • P2 • P2 • P3 • P4 • P5 • P6	Layer cond cond2 cond2 cond2 cond2 cond2		Net P1 P2 P6 P6 P6 P6	Connected to 1(+) 2(+) 1(-) 1(-) 2(-) 2(-)	Purpose drawing drawing drawing drawing drawing drawing	X [mm] 0 45.81 0.1 0.1 45.7 45.7	Y [mm] 0 3.7 -4.5 4.2 -4.8	Num 1 2 3 4 5 6
Layout Pins Name • P1 • P2 • P3 • P4 • P5 • P6	Layer cond cond2 cond2 cond2 cond2 cond2		Net P1 P2 P6 P6 P6 P6	Connected to 1(+) 2(+) 1(-) 1(-) 2(-) 2(-)	Purpose drawing drawing drawing drawing drawing drawing	X [mm] 0 45.81 0.1 45.7 45.7	Y [mm] 0 0 3.7 -4.5 4.2 -4.8	Num 1 2 3 4 5 6

Fabrication Outputs (Important)

Exporting Gerber files

• Click on File -> Export (Use an empty folder for the directory)

	Export	×
	File type	
Select this option	Gerber/Drill ~	More Options
Choose the	Destination directory	
destination directory	C:\Users\arka\163da_demo_wrk\mfg\163da_demo_lib_cell_1\gerber	Browse
	OK Cancel He	łp

Exporting Gerber files

• All files shown below with the exact same name must be present in your zip file

> GerberFiles		~	C $\ensuremath{{}^{^{\ensurem$
Name	Date modif	Туре	Size
🕀 cond	2/14/2024	CAMtastic Layer Gerber Data	1 KB
🕀 cond2	2/14/2024	CAMtastic Layer Gerber Data	1 KB
🕀 silkscreenTop	2/14/2024	CAMtastic Layer Gerber Data	4 KB
solderMaskBottom	2/14/2024	CAMtastic Layer Gerber Data	1 KB
🕕 solderMaskTop	2/14/2024	CAMtastic Layer Gerber Data	1 KB