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Research Article

Comparative Performance Study of Difference Differential Amplifier Using 7 nm and 14 nm FinFET Technologies and Carbon Nanotube FET

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Difference differential amplifiers (DDA), which were built on FinFET and carbon nanotube FET (CNTFET), are frequently used for signal processing owing to their advantages of low-power dissipation and reduced device dimension. In this work, high-performance DDA was established using CNTFET model parameters as well as FinFET 7 nm and 14 nm technology. The DDA circuit used in this scenario was identically the same to the one used previously. With the use of Verilog AMS code-based Stanford model parameters applied CNTFET and 7 nm and 14 nm FinFETs, schematic capture and simulations of the DDA were carried out in the Symica environment. The mostly used measurements for assessing the performance of operational amplifiers were also adopted for DDA. The CNTFET-based difference differential amplifiers have slew rates of 10.8 V/femtosecond and 11.2 mV/femtosecond, respectively, with settling times of 0.65 femtosecond and 0.43 femtosecond, respectively. The power supply rejection ratio (PSRR) is 2.53 dB with a dynamic range of 198 mV and 6 mV for CNTFET DDA operating at 0.6 V DC. The incentives of CNTFET appropriateness for DDA designed in this study for any analogue front end were further demonstrated by using CNTFET for DDA with the achievement of open loop differential gain of 116.03 dB with BW of 4 GHz and phase margin of 270 and common mode gain of -28.65 dB with BW of 55.14 MHz and phase margin of 270.

1. Introduction

The size of transistors must be decreased as integrated circuits (ICs) develop in order to meet the rising requirements for devices with greater speed and reduced power consumption. Currently, silicon planar technologies dominate the market; however, certain of its factors, indeed the regular thickness of the gate oxide layer (Tox), are very close to the physical limit [1]. Thus, in order to build new devices and maintain Moore's law in the growth of integrated circuits, it is necessary to investigate novel materials and production techniques. The carbon nanotube field effect transistors (CNTFETs) and fin field effect transistors (FinFETs), which have electrical properties identical to those of silicon metal-oxide semiconductor field effect transistors (MOSFETs), become two potential candidates.

For any feasible enhancements, numerous technological and device structural variations, namely, single gate FETs, SOI FETs, multiple gate FETs, and CNFETs, are available.

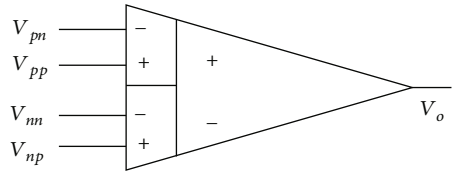


Figure 1: Schematic symbol of the DDA.

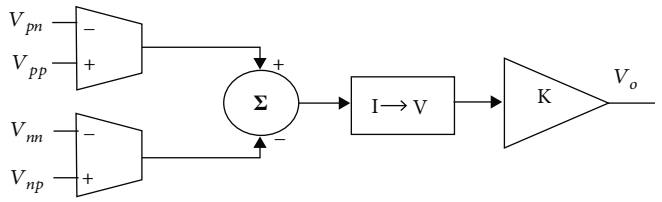


Figure 2: DDA block diagram.

Additionally, FinFETs and CNFETs have recently emerged as crucial advancements for low-power, low-voltage applications. Due to its greater electrostatics, adaptability, and stability, double gate-based transistors can eventually replace CMOS, thus becoming essential component for any types of analogue circuits like differential amplifier and operational amplifier [2]. Current carbon nanotubes are the only known scenario in which the size of exploratory devices will be reduced to incredibly small sizes. It is possible that the results will complement the expectations, enabling, theoretically, for the experimental validation of analytical models and device architecture [3].

It is essential to design phenomenal analogue integrated circuits operate at low supply voltages. Gain, slew rate and power, and other performance metrics were usually traded off at higher supply voltages. In this paper, the proposed design and analysis of low-voltage, low-power difference differential amplifiers (DDAs) using CNTFET and FinFET technologies were focused. The simulation comparative analysis was performed between CNTFET-based DDA and traditional CMOS-based DDA also with FinFET-based DDA. All of the device types, including CNTFET and FinFET, were subjected to simulations of DDA and were then compared for the best outcome from each kind.

1.1. Design of DDA. The main challenges in the design of DDA is making out circuit with supply voltages (vdd) of the order of several saturation voltages of an MOS transistor (Vdsat). Poor signal swing at extreme supply conditions, relatively poor CMRR and PSRR with tail current source, and drawback of CMOS topology are significant limitation on DC responses and the occurrence of asymmetry, if low-voltage processes are used. Figure 1 depicts the schematic representation of the DDA [4, 5] which is an expanded version of an operational amplifier. As opposed to two single-ended inputs like op-amps, it contains two differential input pins. The DDA's output is thus defined.

$$V_o = A_o\left[\left(V_{pp} - V_{pn}\right) - \left(V_{np} - V_{nn}\right)\right]. \tag{1}$$

A_o is an open loop gain. The model equation can be derived provided negative feedback is given to V_{pn} and/or V_{np}, which provides a negative relation in (1):

$$\left(V_{pp} - V_{pn}\right) = \left(V_{np} - V_{nn}\right) \text{ on } A_o \longrightarrow \infty. \tag{2}$$

With increasing open-loop gain, A_o, the difference between the two differential voltages reduces. Figure 1 depicts the DDA. The DDA is actually be implemented as depicted in Figure 2 [3], with two V-I converters acting as the input pins of DDA to transform the two differential voltages into currents that are ultimately subtracted, converted to voltage, and boosted. The use of FinFET/CNTFET devices enabled the development of a DDA with a broad input range. A linear FinFET/CNTFET V-I converter that can be tuned was used to build a DDA with a large input range for wide signal operation.

The main approach for constructing the DDA is to use two differential pairs to develop the V-I converters [6]. The following formula can be used to calculate the differential current I_d of a differential pair biased by a given current source I_s:

$$I_d = \begin{cases} \dfrac{\mathrm{V}_d}{|V_d|} I_s, & \text{for } |V_d| \geq \sqrt{\dfrac{2I_s}{\beta}}, \\ \dfrac{V_d}{|V_d|} V_d \sqrt{\beta I_s \left(1 - \dfrac{\beta {V_d}^2}{4I_s}\right)}, & \text{for } |V_d| < \sqrt{\dfrac{2I_s}{\beta}}. \end{cases} \tag{3}$$

In this equation, V_d is the input differential voltage, $\beta = \mu C_{ox}(W/L)$, W/L is the width to length ratio of the device, μ is their mobility, and C_{ox} is their gate oxide capacitance for anunit area. The component under square root states as the percent deviation from the significance level of $g_m V_d$, wherein g_m is the transconductance when $V_d = 0$, produces nonlinearity in I_d rather than the linear relationship between I_d and V_d. It implies

$$g_m = \left|\frac{dI_d}{dV_d}\right| = \sqrt{\beta I_s}. \tag{4}$$

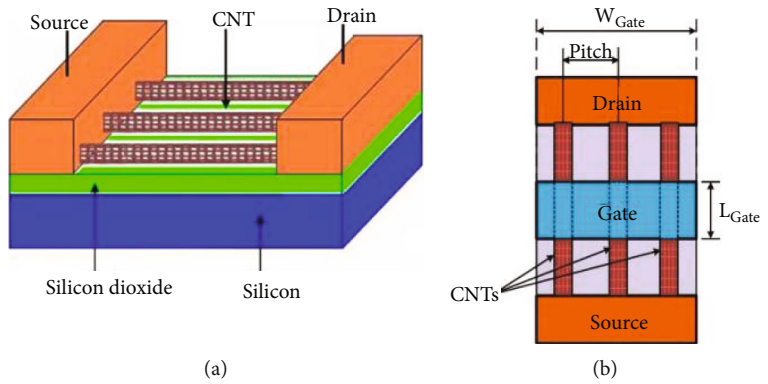


Figure 3: Carbon nanotube field effect transistor (CNFET). (a) Schematic. (b) Top view [26].

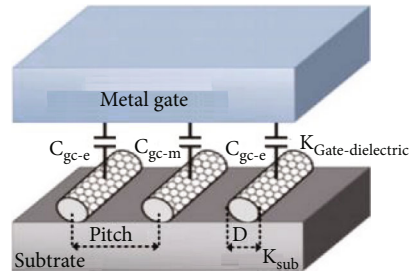


Figure 4: CNFET gate to channel capacitance [26].

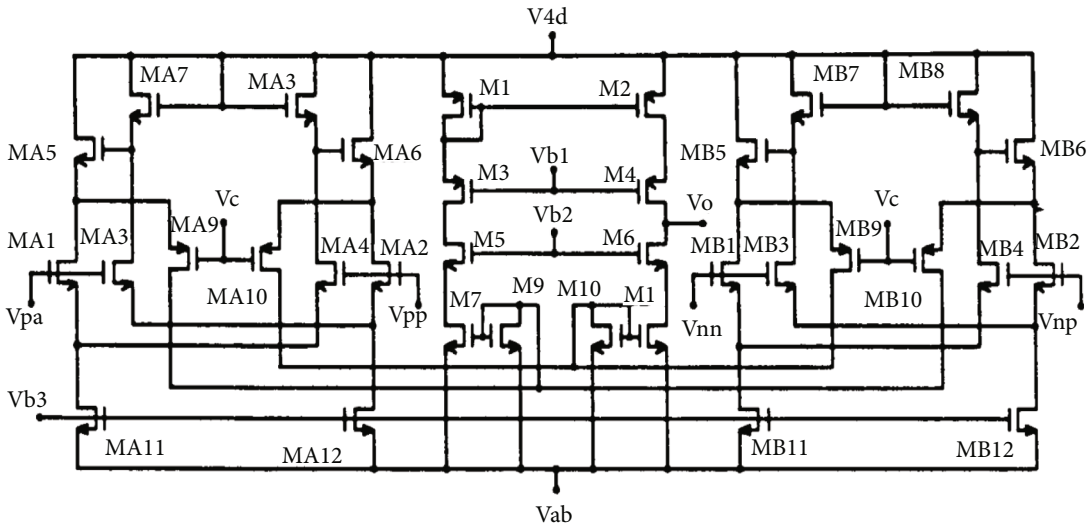


Figure 5: DDA circuit.

The differential pair is always operating at $V_d \approx 0$ due to the virtual short property of op-amps, and thus, the differential pair's transconductance is approximately the g_m.

2. Literature Survey

The extensive survey was done to study the role of CNTFET that started to apply in analogue circuits to enhance their performance. This paper makes an effort to evaluate the performance of DDA using the FinFET and CNTFET.

Crippa et al. [7] analyzed high-gain 90 nm length and 1 μm width CNTFET-based broadband inductor-less low noise amplifier (LNA) and confirmed the overall validity of the proposed high-gain LNA design while comparing both conventional 32 nm CMOS technologies and CNTFET with the limitation of restricted to 90 nm technology. Akhoon et al. [8] designed and simulated a current source load

Table 1: The Stanford CNFET model parameters.

Parameter	Description	Value
V	Power supply	0.7 V
L_g	Physical channel length	16 nm
S_T	CNT pitch	10 nm
(n_1, n_2)	CNT chirality	(19, 0)
L_{ceff}	Mean free path in intrinsic CNT	200 nm
V_{fbn}	N-type CNFET flat band voltage	0
High – K_{ox}	Dielectric material of top gate	HfO_2 (16)
L_s	Source-side length of doped CNT	16 nm
L_d	Drain-side length of doped CNT	16 nm
T_{ox}	Oxide thickness	4 nm
K_{sub}	Dielectric constant	SiO_2 (4)
L_{eff}	Mean free path in doped CNT	15 nm
E_{fo}	Fermi level of n+-doped drain/source CNT region	0.6 eV
N_T	Total number of CNT used per CNFET	~

Table 2: Setting of DC voltage sources for the circuit of Figure 3.

Parameters	7 nm/14 nm	CNTFET
Supply voltage (V)	+0.8/-0.8	+0.6/-0.6
Vb1	0.1	0.1
Vb2	0.1	0.1
Vb3	0.1	0.1
Vc	0	0

differential amplifier (CSL-DA) using n-type carbon nanotube field effect transistors (CNTFET) investigated using HSPICE simulation restricted to 45 nm CNTFET. Yasir and Alam [9] designed CNTFET single-stage-based 5 T single-stage operational transconductance amplifier (OTA) and two-stage operational amplifier using g_m/I_D technique for low-voltage and low-power applications investigated using HSPICE simulation showing the importance of g_m/I_D technique to implement CNTFET-based OTA design. Their results provided accuracy within acceptable limits with input specifications restricted to OTA specifications of GBW and CMRR. Bendre et al. [10] used SPICE compatible Stanford University 32 nm CNFET model and determined that CNTFET-based circuits are considerably competent than that of conventional 32 nm CMOS-based circuits in nanoscale regime. Bhargav et al. [11] designed sinusoidal oscillator CNTFET-based OTA simulated for the transient response, noise analysis, and noise sensitivity restricted to 32 nm CNTFET. Chithambaram et al. [12] proposed voltage differencing transconductance amplifier using CNTFET which operates as a voltage and transconductance operation to achieve high performance and find low power and low voltage and better DC transfer characteristics. Nizamuddin et al. [13] designed and calibrated simulation of multistage operational amplifiers (OP-AMPs) using CNTFET investigated using HSPICE simulation showing increase in DC gain and slew rate of 19.14% and 274.6% and reduced output resistance and power consumption by 133-fold and 200% restricted to 45 nm CNTFET. Puri et al. [14] implemented high-performance, low-power CNTFET-based two-stage op-amp for biomedical A/D converters using SPICE compatible Stanford University 32 nm CNFET model with various numbers of tubes across different transistors and compared DC gain, GBW, and slew rate parameters of CNTFET-based op-amp circuit with 32 nm MOSFET-based op-amp. Loan et al. [15] designed and simulated OTA using n-type carbon nanotube field effect transistors (CNTFETs) investigated using HSPICE simulation increasing gain by 218%, slew rate by 55.2%, and power consumption decrease by 193-fold but compared various channel lengths of CNTFET.

3. Carbon Nanotube Field Effect Transistor

One of the primary benefits of MOSFET technology is its fast-processing speed, but the significant power consumption is a problem and a major roadblock to the development of devices [16]. The basis for developing terascale microchips is complementary MOS (CMOS), which is recognised for its low-power consumption and high noise margin. It is quite difficult to

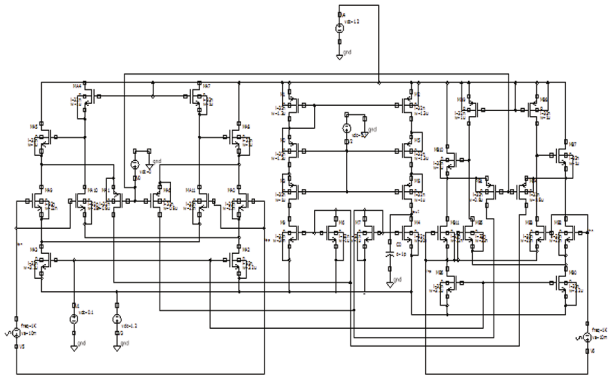


Figure 6: Schematic circuit of FinFET-based DDA used for differential mode gain analysis.

Table 3: 7 nm and 14 nm FinFET device sizes.

Parameters	7 nm process	14 nm process
Gate length (Lg)	10 nm	20 nm
Fin width	4 nm	6.5 nm
Fin height	35 nm	26 nm
Gate height	50 nm	50 nm
EOT	0.65 nm	1.05 nm

scale MOS dimension. The substantial short channel effects, gate leakage, complexity in fabrication, sensitivity to process variables at the nanoscale, and other issues are huge challenges to continually increasing device dimensions [16, 17]. Consequently, a variety of device topologies have been developed, including silicon on insulator [18], FinFETs [19], and carbon nanotube field effect transistors (CNTFETs) [20]. An electrical and mechanical property of it is greatly enhanced when carbon nanotubes (CNTs) are used. A CNTFET is distinguished by its superior electrostatic stability, high carrier transport, large thermal conductivity, and ballistic movement of charge carriers that results in high mobility [19, 21, 22].

A CNTFET, essentially uses an array of single-wall CNTs that are separated and integrated as the conduction channel, is a significant application of CNTs. Iijima of Japan is credited with discovering the first multiwalled CNT in 1991 [23], and Donald Bethune independently developed single-wall (SW) CNTs in 1993. A semiconducting CNT is coupled to two metal electrodes to create the first carbon nanotube field effect transistor, according to Tans et al. [24]. A CNTFET's schematic is shown in Figure 3, and its gate to channel capacitance is shown in Figure 4. The channel has undoped CNTs, while the source and drain areas are identical to those of a typical MOSFET [19, 22, 25, 31].

Owing to its superior electrical, mechanical, chemical, and thermal capabilities, carbon nanotubes (CNTs), which are graphite cylindrical sheets (GCSs), are viewed as the best material for new submicron devices and applications. Single-wall and multiwall CNTs are the two types of CNTs. Whereas multiwall CNT comprises of many GCS, single-wall CNT is focused on a completely GCS. The chirality vector (C_h) affects the single-wall CNT's characteristics [23]. The positive integer vector indices n_1 and n_2 specify the C_h. C_h determines the angle at which the carbon atoms are arranged along the CNT. Based on the vector indexes n_1 and n_2, the single-wall CNT may exhibit crystalline characteristics.

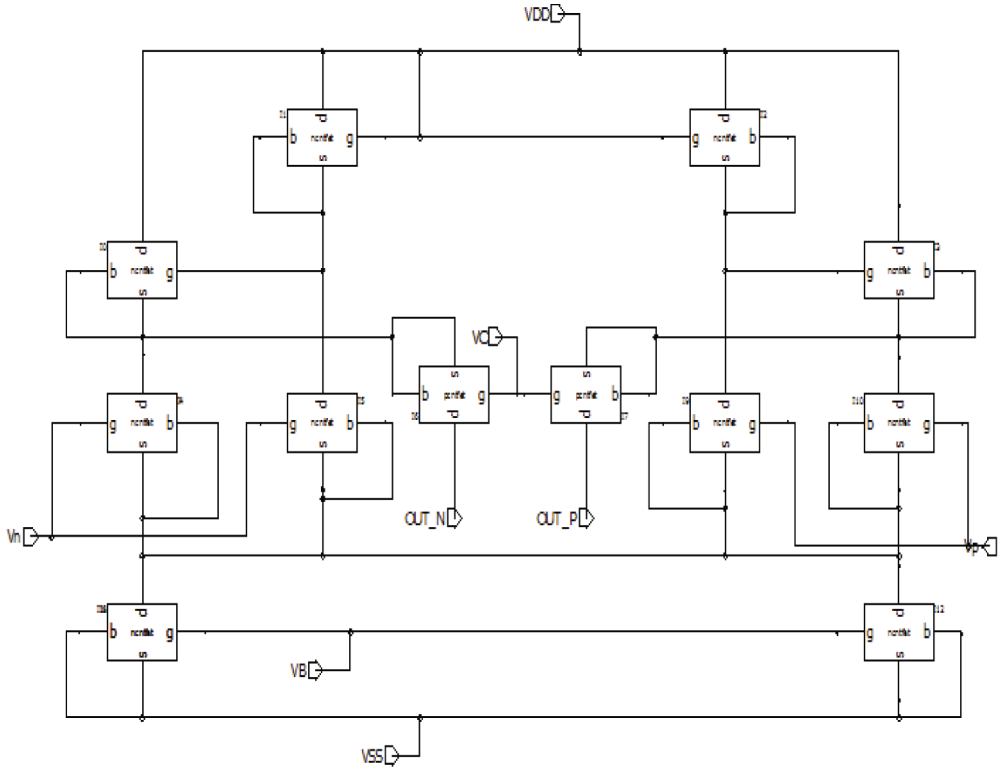
The single-wall CNT operates as a metallic material if $|n_1 - n_2|$ is an integral multiple of 3 or if $n_1 = n_2$, else it operates as a semiconductor. The equations describe the relationships between a CNT's C_h, diameter (DT), and threshold voltage (V_{th}).

$$C_h = a\sqrt{n_1^2 + n_2^2 + n_1 n_2}, \tag{5}$$

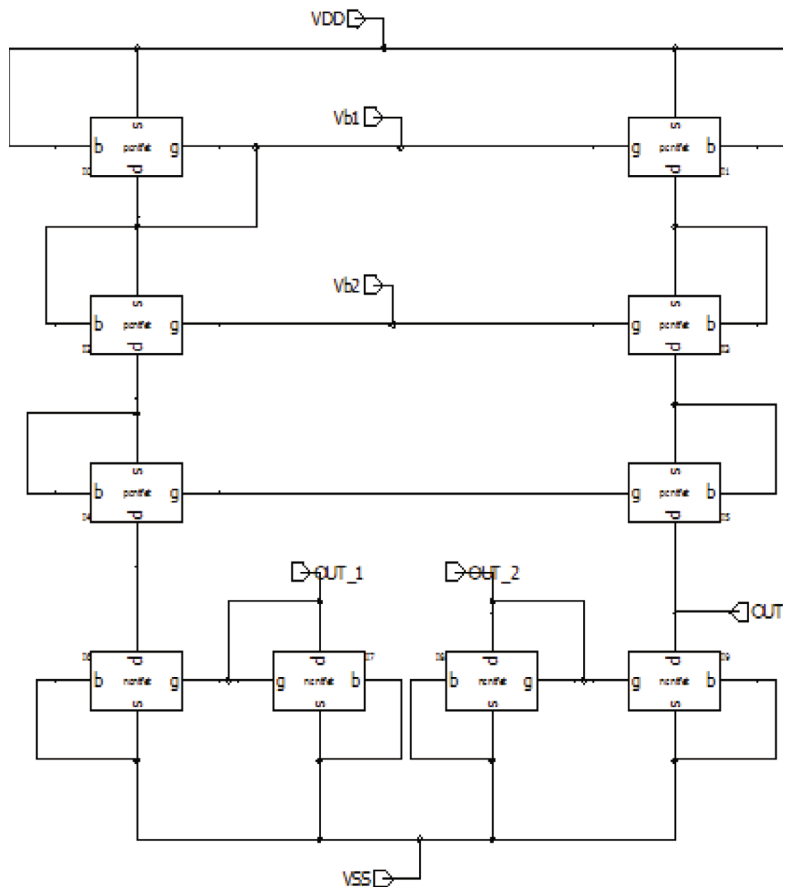
$$D_T = \frac{C_h}{\pi}, \tag{6}$$

$$V_{\text{th}} = \frac{a^{V_\pi}}{\sqrt{3}eD_T}, \tag{7}$$

wherein a is the graphene-lattice factor with a magnitude of 2.49 A^o and e is the standard electron charge. With a magnitude of 3.033 eV, V_π is the π to π bond energy in the tight-bonding model [24]. Carbon nanotube FET (CNTFET) based on different analogue signal processing applications such as inverting amplifier, noninverting amplifier, summer, subtractor, differentiator, integrator, half-wave and full-wave rectifiers, clipper, clamper, inverting and noninverting comparators, peak detector, and zero crossing detector is



(a)



(b)

Figure 7: (a) Schematic circuit of VI converter. (b) Schematic circuit of OTC.

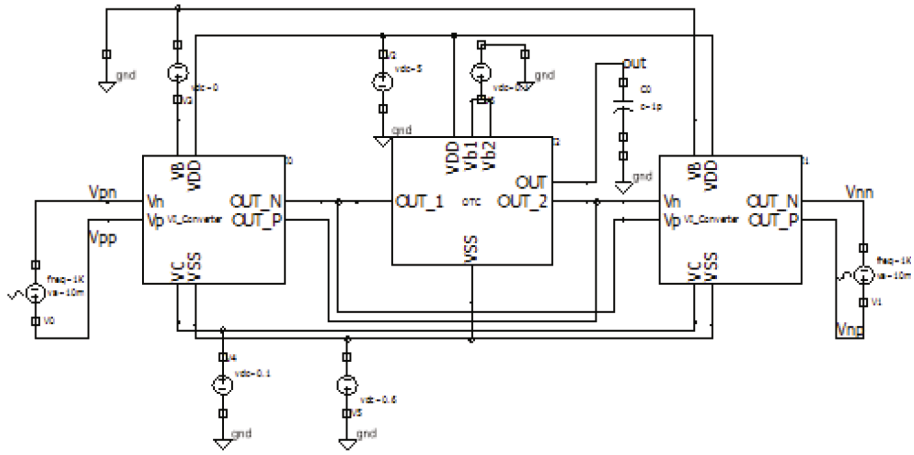


Figure 8: Schematic circuit of CNTFET-based DDA used for differential mode gain analysis.

implemented using low-power folded cascode operational amplifier (op-amp) implemented using CNTFET.

3.1. Circuit Setting for Simulation. To design FINFET technology, use a robust and precise mode to simulate in predictive technology model (PTM). The W/L ratios and PTM models were changed with device technologies. Symica EDA was used to construct the DDA circuits shown in Figure 5. FinFET transistors and CNTFETs were designed in DDA employing Verilog AMS, and Stanford CNFET model parameters are presented in Table 1. Using Symica EDA tool can construct the DDA circuits, FinFET transistors, and carbon nanotube FETs and can employ Verilog AMS and Stanford carbon nanotube FET model parameters.

Performance analyses of DDA CNTFETs with 15 carbon nanotubes in 16 nm technology and FinFETs with 7 nm and 14 nm technologies were done in Symica EDA. Comparative data for DC voltage sources given to a DDA circuits with different devices is shown in Table 2

3.1.1. Differential Mode Gain. To design FINFET technology, use a robust and precise mode to simulate in predictive technology model (PTM). Differential mode gain is obtained by setting the configuration of both input transconductance amplifiers as shown in Figure 6. Verilog A code which includes the device parameters as stated in Table 3 was used to simulate the 7 nm and 14 nm FinFET transistors. Their Symica schematic DDA circuit used for different gain AC analysis is depicted in Figure 7(a) showing the realization of voltage to current (VI) converters and output transconductance (OTC) for the CNTFET-based realization of DDA shown in Figure 7(b).

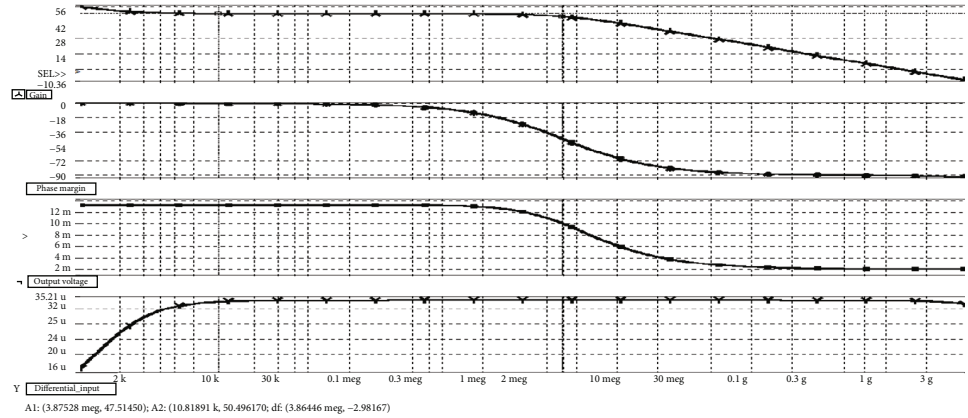
Figures 6 and 8 show the Symica schematic DDA circuits that were used for various gain AC analyses. The comparison results of the AC analysis, including the gain, phase margin, output voltage, and differential input voltage of the DDA, are shown in Figures 9(a)–9(c). The differential inputs of DDA are connected to a sinusoidal source of 10 mV and 1 kHz, and the output is coupled to a 1 pf capacitor. Then, AC analysis is carried out by sweeping the frequency with steps of 10 kHz from 1 kHz to 4 GHz. The parameters of AC sources are shown in Table 4. Table 5 compares the values of the differential mode gain AC analysis of DDA.

3.1.2. Common Mode Gain. The configuration of DDA is established as indicated in Figure 10 to achieve common mode gain. Verilog A is used in the instance of 7 nm/14 nm FinFETs and CNTFET with Stanford parameters. To simulate the transistors, the codes use the device parameters listed in Table 2 for CNTFET and Table 3 for FinFETs. Figure 11 shows the DDA circuits that were utilised for the common mode gain AC analysis. The comparison of AC analysis parameters such as gain, phase margin, output voltage, and common input voltage of DDA is shown in Figure 12.

The differential inputs of DDAs are connected to a sinusoidal source of 10 mV and 1 kHz, and the output is coupled to a 1 pf capacitor. Then, AC analysis is carried out by sweeping the frequency with steps of 10 kHz from 1 kHz to 4 GHz. The parameters of the input sources are shown in Table 6. Table 7 compares the characteristics of the DDA's common mode gain AC analysis.

3.1.3. Common Mode Rejection Ratio (CMRR). The comparison of CMRR, including gain and phase margin, output voltage, and common input voltage of DDA, is shown in Figure 13 because CMRR is the ratio of differential mode gain to common mode gain. These results were produced using Python using SPICE-exported CSV files. The CMRR of DDAs, which were calculated from Figure 13, are compared in Table 8.

3.1.4. Slew Rate. Slew rate measures the ratio of voltage change over time for both the rise and fall of the output voltage in relation to the input voltage. Table 9 compares the slew rate parameters of DDAs using various transistor technologies and varieties. The role of slew rate analysis in carbon nanotube FET DDA gives the maximum rate of change of an amplifier



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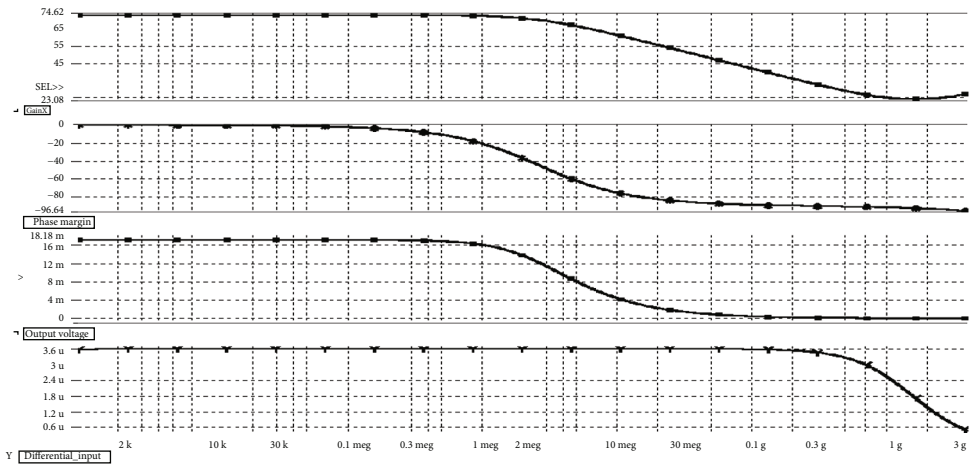

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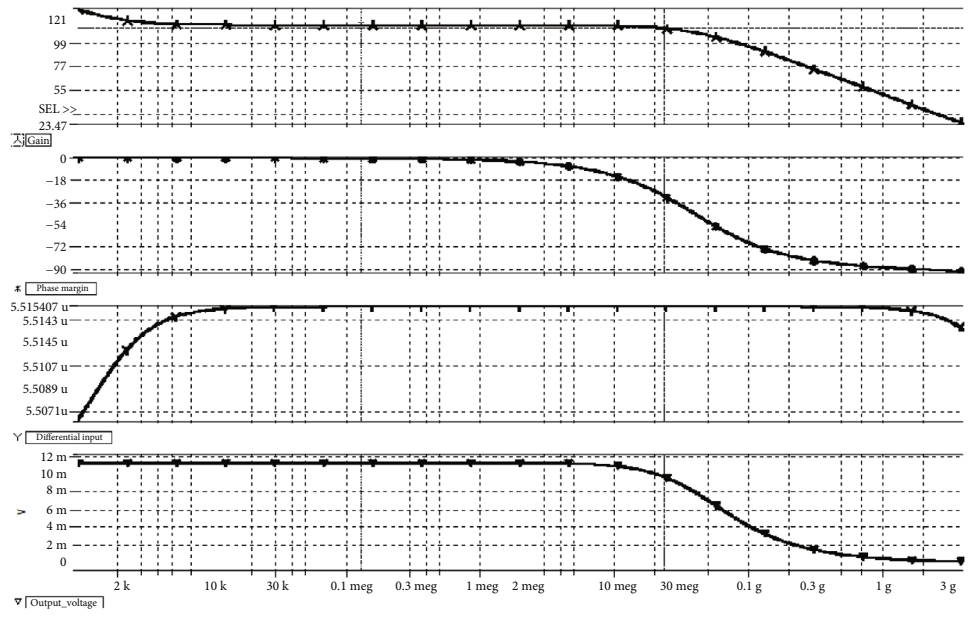


(c)

Figure 9: (a) Differential mode AC analysis of DDA which contains transistors of 7 nm FinFET. (b) Differential mode AC analysis of DDA which contains transistors of 14 nm FinFET. (c) Differential mode AC analysis of DDA which contains transistors of CNTFET.

Table 4: Setting of input source for differential mode gain AC analysis.

Parameters	V_{pp} and V_{pn}	V_{np} and V_{nn}
Source type	AC	AC
Amplitude	10 m	10 m
Frequency	1 kHz	1 kHz
Phase shift	0	180

Table 5: Comparison of differential mode gain AC analysis of DDA.

Parameters/devices	7 nm FinFET	14 nm FinFET	16 nm CNTFET
Gain	50.6	74.62	116.03
Gain 3 dB	47.6	71.62	113.03
3 dB frequency	3.76 MHz	2.1 MHz	23.54 MHz
Phase margin at -3 dB	-44.22	-50	-26.43
Cutoff frequency at 0 dB	1.4 GHz	1.2 GHz	4 GHz
Phase margin at 0 dB	-90	-90	-107
Differential input voltage	34.2 μV	3.6 mV	5.15 μV
Output voltage	11.32 mV	18.18 mV	11.8 mV
Differential input voltage at 3 dB	34.2 μV	3.6 μV	5.15 μV
Output voltage at 3 dB	mV	12 mV	9.9 mV

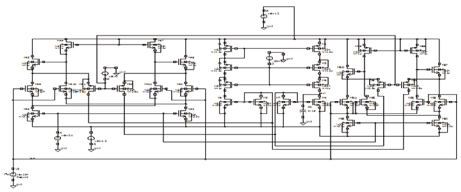


Figure 10: Schematic circuit of FinFET DDA used for common mode gain analysis.

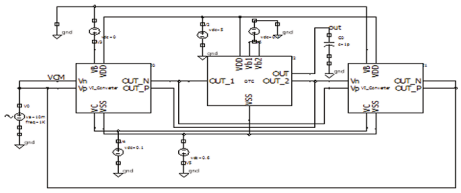


Figure 11: Schematic circuit of CNTFET DDA used for common mode gain analysis.

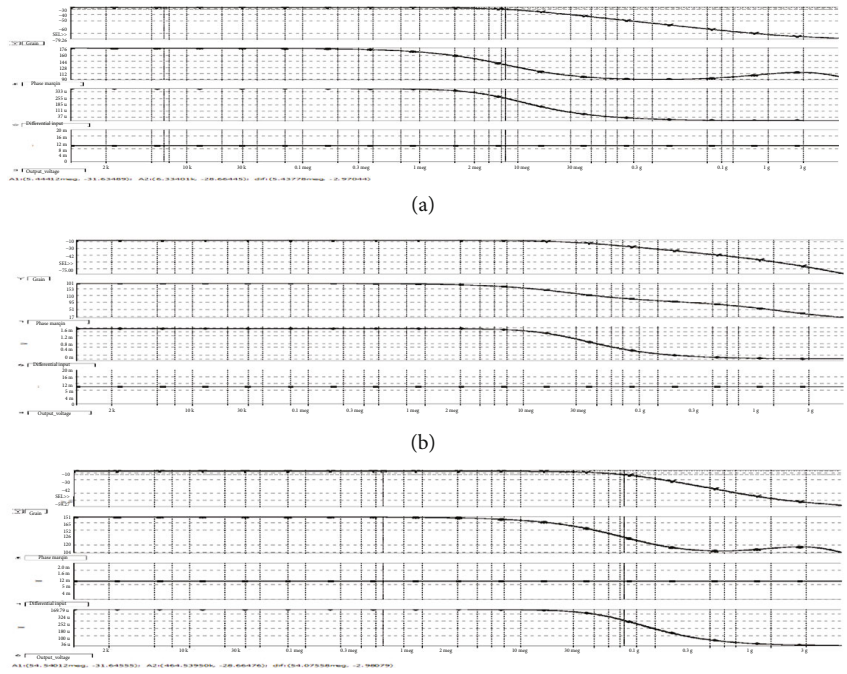
output voltage, and its makes higher bandwidth. Slew rate changes with the change of voltage gain.

3.1.5. Power Supply Rejection Ratio (PSRR). Power supply rejection ratio or PSRR is described as a capacity of the circuit to absorb power supply changes at its output signal. It is also known as supply-voltage rejection ratio. A measure of a capability of an amplifier to maintain a consistent output voltage as the DC power supply voltage varies. So it needs to analyze because a lower output current decreases the dropout voltage and helps improve power supply rejection ratio (PSRR).

The equation in calculating the PSRR is PSRR = 20 log (Power Supply Variation)/(Input Offset Voltage Variation)[dB].

In theory, PSRR is frequency dependent and decreases with increasing frequency. Figures 14 and 15 show the DDA circuits that were used for PSRR. Figure 16 compares PSRR metrics like gain and phase margin of DDA. The comparison of PSRR of DDA parameters that were calculated from Figure 16 is shown in Table 10.

PSRR decrease in carbon nanotube FET is beneficial for circuits because a lower output current decreases the dropout voltage and helps improve power supply rejection ratio (PSRR) which is the ratio of O/P noise and I/P noise.



(a)

(b)

(c)

Figure 12: (a) Common mode AC analysis of DDA of 7 nm FinFET based. (b) Common mode AC analysis of DDA of 14 nm FinFET based. (c) Common mode AC analysis of DDA of CNTFET based.

Table 6: Setting of input source for common mode gain AC analysis.

Parameters	V_{pp}, V_{pn}, V_{np}, and V_{nn}
Source type	AC
Amplitude	10 mV
Frequency	1 kHz
Phase shift	0

Table 7: Comparison of common mode gain AC analysis of DDA.

Parameters/devices	7 nm FinFET	14 nm FinFET	16 nm CNTFET
Gain	-28.66	-37.8	-28.65
Gain 3 dB	-31.66	-40.8	-31.65
3 dB frequency	5.44 MHz	21 MHz	55.14 MHz
Phase margin at -3 dB	-56.22	-119	-136
Common input voltage	10 mV	10 mV	10 mV
Output voltage	368.78 μV	1.6 mV	369.79 μV
Common input voltage at 3 dB	10 mV	10 mV	10 mV
Output voltage at 3 dB	259.43 μV	0.8 mV	255 μV

3.1.6. Input Common Mode Range (ICMR). The device comparison of the ICMR change in V_0 vs. V_{ss} is shown in Figure 17. The supply voltage is V_{ss}. Offset voltage is used as the differential input for the ICMR analysis, and a DC sweep is then run on V_{ss} to measure changes in the output voltage V_0. Table 11 compares the ICMR DDA parameters that were generated from Figure 17 in terms of each other.

4. Results and Discussions

Table 12 compares the DC analysis of DDA for various devices, including CNTFET, 7 nm FinFET, and 14 nm FinFET. According to Table 12, the CNTFET operates with DC voltage of 0.6 V, which is lower than that of other devices using 7 nm and 14 nm FinFETs but still essential for determining chip size. The 2.1 nA drawn by the CNTFET is less than that of other devices using 7 nm and 14 nm FinFETs, making it a crucial requirement in deciding the chip power. Additionally, the input impedance of the CNTFET is 255 MΩ, which is higher than that of analogous devices made of 7 nm and 14 nm FinFETs and is also more important for evaluating the sensitivity of devices to input signals.

According to Table 13, the differential mode gain of CNTFET, which is higher than those of other transistors using 7 nm and 14 nm FinFETs, is 116.03 dB with a BW of 23.4 MHz. The differential mode gain must be high, and those frequencies must be in the low frequency range for any instrumentation amplifier.

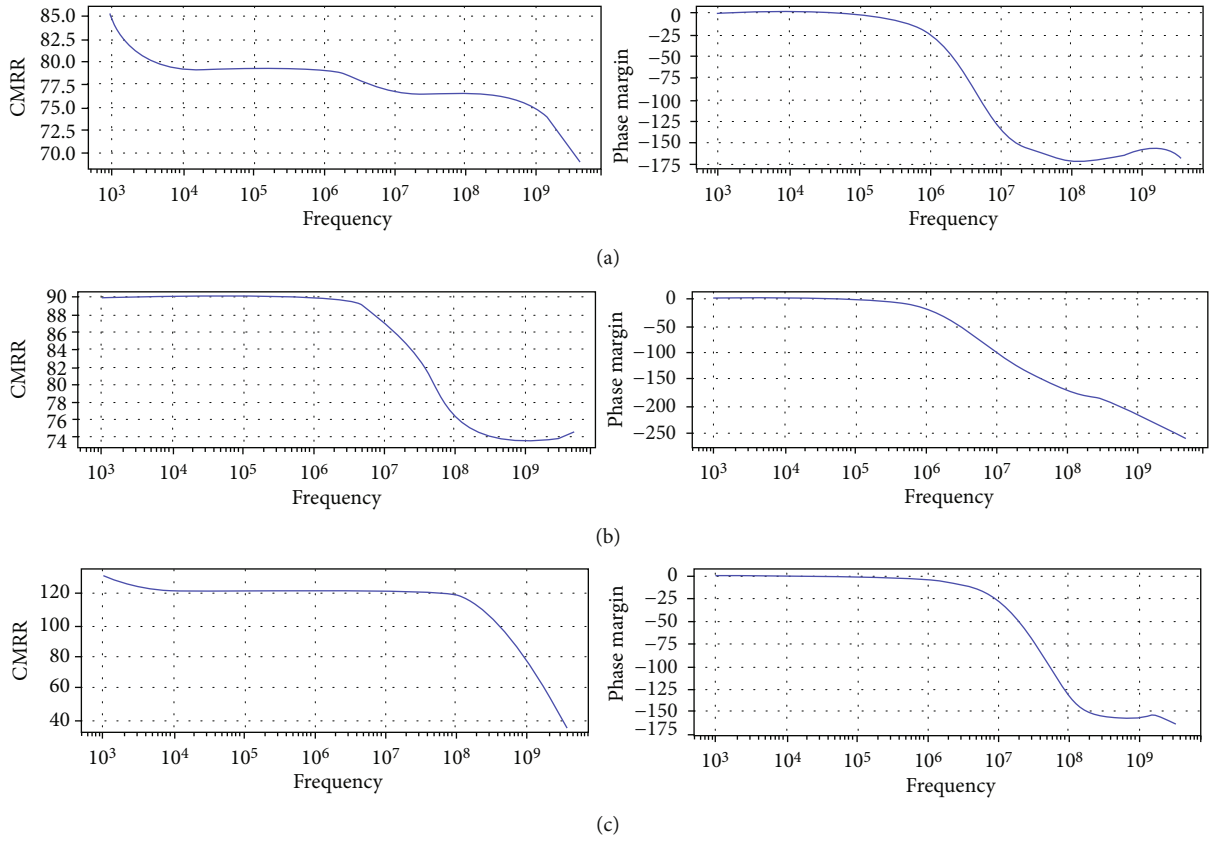


Figure 13: (a) CMRR of DDA of 7 nm FinFET based. (b) CMRR of DDA of 14 nm FinFET based. (c) CMRR of DDA of CNTFET based.

Table 8: Comparison of CMMR of DDA.

Parameters/devices	7 nm FinFET	14 nm FinFET	16 nm CNTFET
Gain	79.18	89.8	131.78
Gain 3 dB	76.18	86.8	128.78
3 dB frequency	238.5 MHz	20 MHz	134.2 M
Phase margin at -3 dB	-166.22	-150	-152.22

Table 9: Comparison of slew rate of DDA.

Parameters/devices	7 nm FinFET	14 nm FinFET	16 nm CNTFET
Rise slew rate	110 V/fs	127 V/fs	10.8 V/fs
Fall slew rate	107 V/fs	126 V/fs	11.2 V/fs
High amplitude	1.5 mV	1.84 mv	1.58 mV
Low amplitude	1.39 mV	1.83 mV	1.53 mV

Compared to other devices, such as 7 nm and 14 nm FinFETs, the CNTFET's common mode gain of -28.65 dB with a BW of 55.14 MHz is more tolerable. The common mode gain must be exceptionally low for any instrumentation amplifier, and those frequencies must be in the low range.

According to Table 13, the CNTFET has a CMRR of 131.78 dB and a BW of 134.2 MHz, which is better than previous devices with 7 nm and 14 nm FinFETs. The CMMR needs to be high and they need to have a greater bandwidth for any instrumentation amplifier.

According to Table 13, the CNTFET possesses output slew rates of 10.8 V/femtosecond for input rise and 11.2 V/femtosecond for input fall that are more acceptable when compared to other devices, such as 7 nm and 14 nm

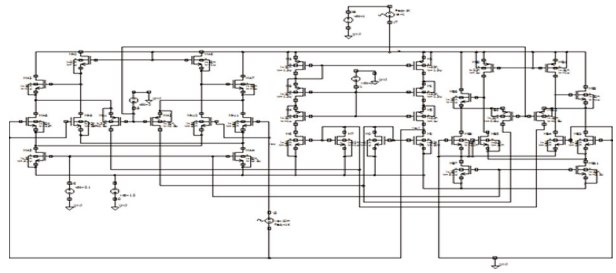


Figure 14: Schematic circuit of DDA used for PSRR analysis by FinFET devices.

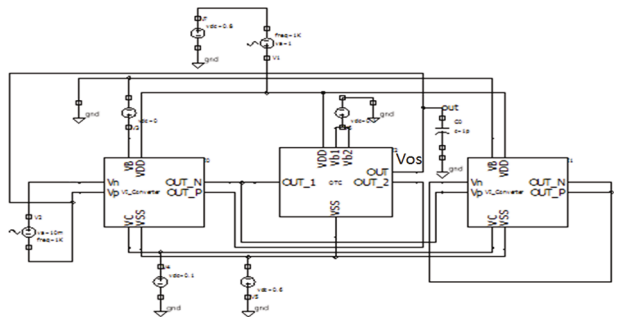
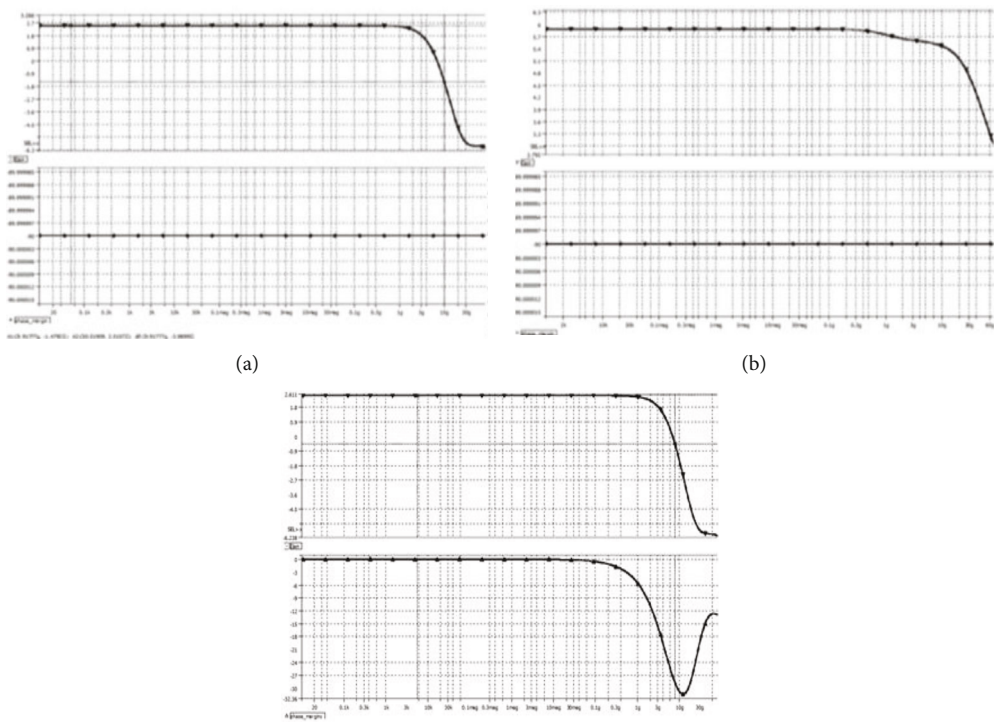


Figure 15: Schematic circuit of DDA used for PSRR analysis by CNTFET device.

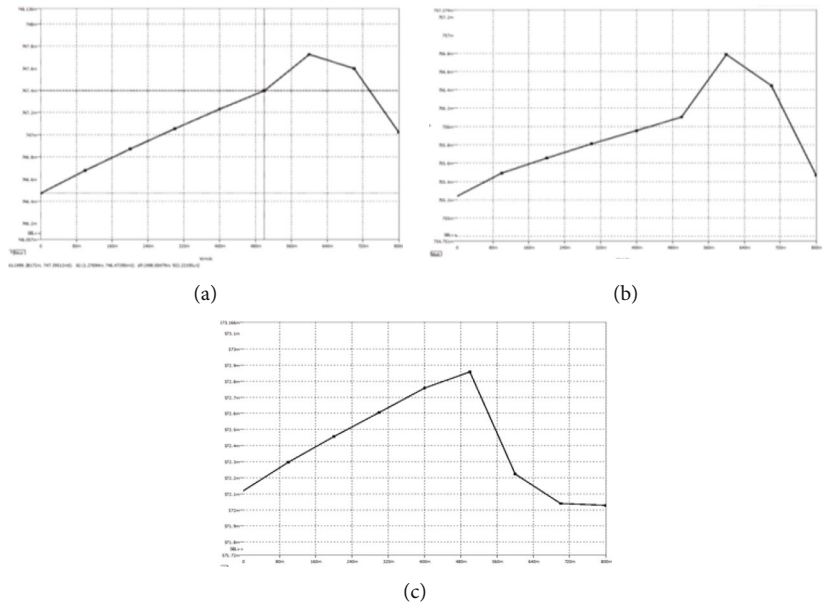


(a) (b) (c)

Figure 16: PSRR of DDA using (a) 7 nm FinFET, (b) 14 nm FinFET, and (c) CNTFET.

Table 10: Comparison of PSRR of DDA.

Parameters/devices	7 nm FinFET	14 nm FinFET	16 nm CNTFET
Gain	6.51	7.02	2.53
Gain 3 dB	3.51	4.02	-0.47
3 dB frequency	9.73 GHz	70 GHz	998 kHz
Phase margin at -3 dB	-90	-90	-28



(a) (b) (c)

Figure 17: ICMR of DDA using (a) 7 nm FinFET, (b) 14 nm FinFET, and (c) CNTFET.

Table 11: Comparison of ICMR of DDA.

Voltage levels	7 nm FinFET	14 nm FinFET	16 nm CNTFET
Low	0	752 mV	572.15 mV
High	mV	758 mV	572.8 mV

Table 12: Comparison of DC analysis of DDA.

Technology	Vdc	Rin	Io^+/Io^-
32 nm CMOS	1.2	9.1 MΩ	1.43 μA
22 nm CMOS	1.2	41.3 MΩ	0.27 μA
7 nm FinFET	0.8	123 MΩ	6.5 nA
14 nm FinFET	0.8	186 MΩ	4.3 nA
CNTFET	0.6	255 MΩ	2.1 nA

FinFETs. Any instrumentation amplifier needs a high enough slew rate to function properly.

According to Table 13, the CNTFET has a PSRR of 2.53 dB and a BW of 998 kHz, which is better than comparable devices like 7 nm and 14 nm FinFETs. The PSRR needs to be high and the bandwidth needs to be wider for any instrumentation amplifier.

According to Table 11, the ICMR values for the CNTFET are between 572.15 mV and 572.8 mV, which is more acceptable when compared to other devices like 7 nm

Table 13: Comparison of the performance between current and previous researches.

Parameters	Matthus et al. [27]	Khateb et al. [28]	Khateb and Kulej [29]	Anand Kumar et al. [30]	This research
Technology	0.18 μm bipolar, CMOS	0.18 μm CMOS TSMC	0.18 μm CMOS TSMC	14 nm FinFET PTM model	16 nm CNTFET
DC supply	1.8 V	0.5 V	0.3 V	0.8 V	0.6 V
Gain	46 dB	61.4 dB	60 dB	74.62 dB	116.03 dB
Bandwidth	2 MHz	6.98 kHz	1.85 kHz	20 MHz	23.4 MHz
Power consumption	—	246.6 nW	22 nW	3.44 nW	1.42 nW
CMRR	—	100 dB	—	89.8 dB	131.78 dB
PSRR	—	127.8 dB	57 dB	7.02 dB	2.53 dB
Slew rate	—	500 V/μs	1.55 V/μs	127 V/fs	10.8 V/fs

and 14 nm FinFETs. The ICMR must be low for any instrumentation amplifier to detect low signal voltages; however, 14 nm FinFET performance is subpar and has limited linear operation. Table 13 shows that the 16 nm CNTFET outperforms earlier research in terms of performance.

5. Conclusions

This paper provided a useful comparison of various FinFETs and CNTFET device technologies applied to a differential difference amplifier (DDA) and ultimately recommended CNTFET as a remarkable optional device for DDA-based instrumentation amplifier in order to improve the performance of DDA on fairly close rail-to-rail input changes and with output changes, a rather increased DC input resistance, and with incredible CMRR. Anywhere where a comparison between two weak differential voltages is required, this CNTFET-based DDA can be used. This device can also be used as a versatile building block to create a variety of useful analogue circuits, some of which will be investigated in the future. By substituting alternative polymer devices for CNTFET, future study will aim to further enhance DDA performance, such as improved open loop gain and PSRR.

CNT FinFETs with optimized threshold voltages can provide an EDP advantage of approximately 50 times over Si FinFETs under a low supply voltage (V dd = 0.4 V), suggesting great potential for CNT FinFET. Compared with a Si FinFET, the CNT FinFET presents obvious advantages in speed and EDP arising from its almost much larger current density but also results in a higher total power dissipation, especially at a low threshold voltage (V th = 1/3 V dd). Carbon nanotube FET DDA will be better than silicon because carbon nanotubes are almost thin ferry electricity. In principle, carbon nanotube could run three times faster while consuming about one-third of the energy of silicon. Carbon nanotube FET DDA replace silicon with their excellent electrical conductivity, and carbon nanotubes have long been seen as a potential replacement for silicon. Three main challenges are involved: material defects, manufacturing defects, and functional issues.

If carbon nanotube FinFET is compared with a Si FinFET, CNT FinFETs with optimized threshold voltages can provide an EDP advantage of approximately 50 times over Si FinFETs under a low supply voltage (V dd = 0.4 V), suggesting great potential for CNT FinFET. Compared with a Si FinFET, the CNT FinFET presents obvious advantages in speed and EDP arising from its almost much larger current density but also results in a higher total power dissipation, especially at a low threshold voltage (V th = 1/3 V dd). Carbon nanotube FET DDA was used as a versatile building block to create a variety of useful analogue circuits, some of which will be investigated in the future. Substituting alternative polymer devices for CNTFET can enhance DDA performance, such as improved open loop gain and PSRR.

Data Availability

The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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