0.5-V Analog Circuit Techniques and Their Application in OTA and Filter Design

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***Abstract*—We present design techniques that make possible the operation of analog circuits with very low supply voltages, down to 0.5 V. We use operational transconductance amplifier (OTA) and filter design as a vehicle to introduce these techniques. Two OTAs, one with body inputs and the other with gate inputs, are designed. Biasing strategies to maintain common-mode voltages and attain maximum signal swing over process, voltage, and temperature are proposed. Prototype chips were fabricated in a 0.18-μm CMOS process using standard 0.5-V V_T devices. The body-input OTA has a measured 52-dB DC gain, a 2.5-MHz gain-bandwidth, and consumes 110 μW. The gate-input OTA has a measured 62-dB DC gain (with automatic gain-enhancement), a 10-MHz gain-bandwidth, and consumes 75 μW. Design techniques for active-RC filters are also presented. Weak-inversion MOS varactors are proposed and modeled. These are used along with 0.5-V gate-input OTAs to design a fully integrated, 135-kHz fifth-order elliptic low-pass filter. The prototype chip in a 0.18-μm CMOS process with V_T of 0.5-V also includes an on-chip phase-locked loop for tuning. The 1-mm^2 chip has a measured dynamic range of 57 dB and draws 2.2 mA from the 0.5-V supply.**

***Index Terms*—Active filters, analog integrated circuits, body bias, low voltage, operational amplifiers, varactors.**

I. Introduction and Motivation

CONTINUING technology feature-size scaling requires a proportional downscaling of the supply voltage to maintain device reliability. At the same time, a relatively large threshold voltage (V_T) needs to be maintained to limit the OFF current [1] in transistors. These two factors pose significant challenges for the design of analog circuits in future standard digital CMOS processes. Charge pump techniques are sometimes used to boost on-chip voltages beyond the supply; this may lead to reliability problems in some cases. However, a number of techniques can make possible true low-voltage operation without voltage boosting; these include the use of weakly inverted devices where feasible, the use of the body node as a fourth control or signaling terminal, and the use of circuit topologies avoiding stacked transistors. To investigate the synergistic use of such techniques, we have designed two operational transconductance amplifiers (OTAs) and an automatically tuned fifth-order low-pass filter, and have pushed their operation to supply voltages as low as the V_T of the standard devices, in our case, 0.5 V [2], [3].

In Section II, we discuss two different true low-voltage OTA design techniques using standard CMOS technology, first using the body nodes of the MOS devices to apply the signal with biasing accomplished through the gates, and then using the gate nodes of the MOS device for the signal with biasing through the body. We contrast the two techniques using prototypes on a CMOS 0.18-μm process with measurement results. In Section III, we propose and analyze a low-frequency weak-inversion 0.5-V MOS varactor for use in active varactor-R filters. In Section IV, we demonstrate the design of a filter using gate-input OTAs and the varactors as building blocks. The prototype chip has been extensively characterized and experimental results for different chips, different supply voltages, and different temperatures are presented. Note that future CMOS technologies will offer much faster transistors that also have a lower V_T compared to 0.18-μm transistors. The techniques demonstrated here are thus expected to yield higher performance once these technologies become available [1].

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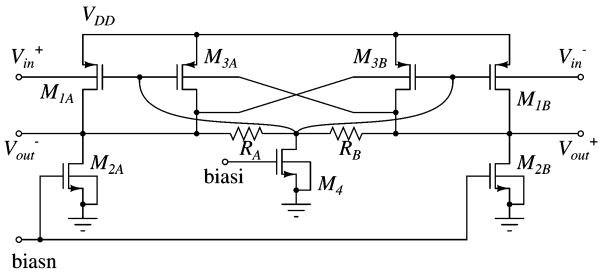


Fig. 1. Fully differential body-input gain stage with local common-mode feedback.

II. 0.5-V Fully Differential Operational Transconductance Amplifiers

For any high-performance application that requires high bandwidth or sampling rate, MOS devices are biased in strong inversion, i.e., $(V_{GS}-V_T)>0.2$ V. The devices act as transconductors or current sources as long as $V_{DS} \geq V_{DS,sat}$. A good estimate of $V_{DS,sat}$ at the edge of strong inversion or in weak and moderate inversion is about 0.15 V [4]. So, in any region of operation, we need to maintain V_{DS} of at least 0.15 V, irrespective of the device V_T. The common-source configuration thus has the potential to operate at supply voltages of 0.5 V.

Forward biasing of the body-source junction has been applied in low-voltage digital circuits [5]–[8] and it is applied here to lower the V_T of the transistors. We typically apply a forward bias of about 250 mV, which results in a lowering of the V_T by about 50 mV. In the context of 0.5-V operation, the risk of forward-biasing the junctions is minimized since parasitic bipolar devices cannot be activated even when the full power supply is

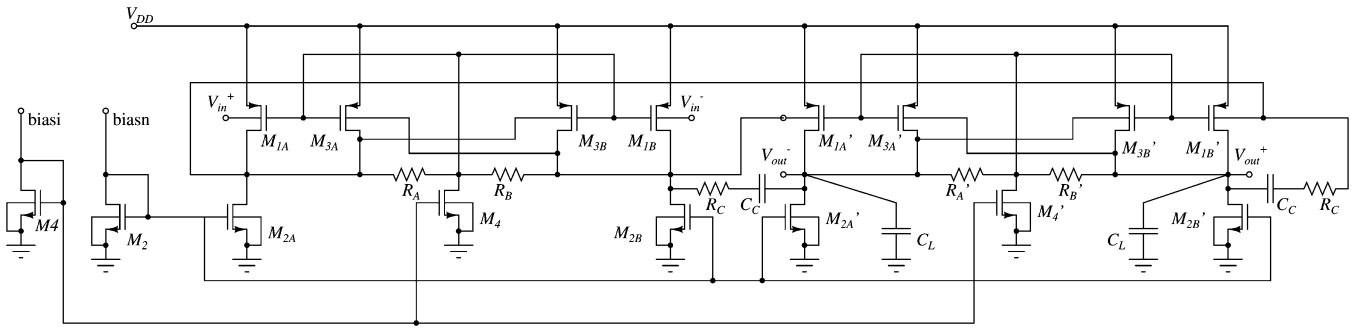


Fig. 2. Two-stage fully differential body-input OTA with Miller compensation.

used as forward bias, provided that supply transient overvoltages are adequately kept under control.

A. Body-Input OTA

Body-input operational amplifiers with a single-ended output have been investigated for low-voltage applications down to 0.7 V [9]–[13]. In order to operate a MOS transistor at or near moderate inversion, a large voltage can be applied as a gate bias, and the signal can be applied to the body of the device. A very low-voltage basic gain stage is shown in Fig. 1. The two inputs are at the bodies of pMOS transistors M_{1A} and M_{1B}, and their g_{mb} provides the input transconductance. For an input common-mode voltage of $V_{\rm DD}/2$ (0.25 V), the resulting small body-source forward bias lowers the V_T and further increases the inversion level. Operation near the weak-moderate inversion boundary is preferred, in order to attain a relatively large body transconductance, g_{mb}. M_{1A} and M_{1B} are loaded by the nMOS transistors M_{2A} and M_{2B}, which act as current sources. The body inputs of M_{3A} and M_{3B} form a cross-coupled pair that adds a negative resistance to the output and boosts the differential DC gain. Resistors R_A and R_B detect the output common-mode voltage which is fed back to the gates of the pMOS devices M_{1A}, M_{1B}, M_{3A} and M_{3B} for common-mode rejection. A DC level shift between the output common-mode voltage at 0.25 V and the gate bias at 0.1 V is created by pulling a small current through R_A and R_B with M_4.

In the following, g_{mb_N} is the body transconductance of M_N, g_{m_N} is the gate transconductance of M_N, and g_{ds_N} is the drain-source conductance of M_N. The differential DC gain is

$$A_{\rm diff} = \frac{g_{mb_1}}{g_{ds_1} + g_{ds_3} + g_{ds_2} + \frac{1}{R} - g_{mb_3}}. \quad (1)$$

The common-mode DC gain is given by

$$A_{cm} = \frac{g_{mb_1}}{g_{ds_1} + g_{ds_3} + g_{ds_2} + g_{mb_3} + g_{m_1} + g_{m_3}}. \quad (2)$$

The common-mode signal is strongly suppressed as a result of g_{m_1} being larger than g_{mb_1} and is intrinsically less than 1. In our design, $A_{\rm diff}$ was 24 dB per stage, and A_{cm} was -14 dB per stage. The input-referred white noise spectral density $[V^2/{\rm Hz}]$ is given by

$$8kT \cdot \frac{2}{3} \cdot \frac{1}{g_{mb_1}} \left(\frac{g_{m_1}}{g_{mb_1}} + \frac{g_{m_2}}{g_{mb_1}} + \frac{g_{m_3}}{g_{mb_1}} \right) + \frac{2 \cdot 4kT}{g_{mb_1}^2 R}. \quad (3)$$

TABLE I
TRANSISTOR SIZES AND ELEMENT VALUES FOR THE BODY-INPUT OTA

First stage			Second stage		
Transistors	W [μm]	L [μm]	Transistors	W [μm]	L [μm]
M_{1A}, M_{1B}	240	0.5	M'_{1A}, M'_{1B}	240	0.5
M_{2A}, M_{2B}	75	0.5	M'_{2A}, M'_{2B}	75	0.5
M_{3A}, M_{3B}	40	0.5	M'_{3A}, M'_{3B}	40	0.5
M_4	3.5	1.0	M'_4	3.5	1.0
Resistors and Capacitors					
R_A, R_B	100 kΩ		R'_A, R'_B	100 kΩ	
			R_C	6.5 kΩ	
			C_C	6 pF	

The input-referred noise is intrinsically large because the body transconductance g_{mb} is small in comparison to the gate transconductance g_m.

By cascading two identical gain blocks, a two-stage OTA is obtained as shown in Fig. 2. The amplifier is stabilized by adding Miller compensation capacitors C_C with series resistors R_C to move the right half-plane zero to the left half-plane. The frequency response has a gain-bandwidth product approximately given by $g_{mb_1}/(2\pi C_C)$, where g_{mb_1} is the body transconductance of the input transistors of the first stage; the second pole frequency is approximately at $g'_{mb_1}/(2\pi C_L)$, where g'_{mb_1} is the body transconductance of the input transistors of the second stage and C_L is the load capacitance. In applications with multiple OTA stages, the input pMOS n-well to p-substrate parasitic capacitance presents a load to the previous OTA stage. However, this capacitance will form part of the total compensation capacitance, which will be dominated by the compensation capacitors themselves.

M_{1A} and M_{1B} were sized for a gain-bandwidth product of 2.5 MHz for a bias current of 40 μA and a load of 20 pF on each output. Throughout the design, a channel length of 0.5 μm was used to limit the influence of the reverse short-channel effect. M_{3A} and M_{3B} were sized conservatively for a 9-dB gain improvement. The design had a nominal power dissipation of 100 μW. The transistor widths and lengths and the values of the passive elements are shown in Table I. Currents of 40 and 4 μA were input through the nodes "biasn" and "biasi" as shown in Fig. 2. The current mirrors reflect these currents through M_{2A}, M_{2B}, and M_4, respectively.

A prototype of total area 0.13 mm $\times$ 0.2 mm was fabricated on a CMOS 0.18-μm mixed-signal process. High-resistivity

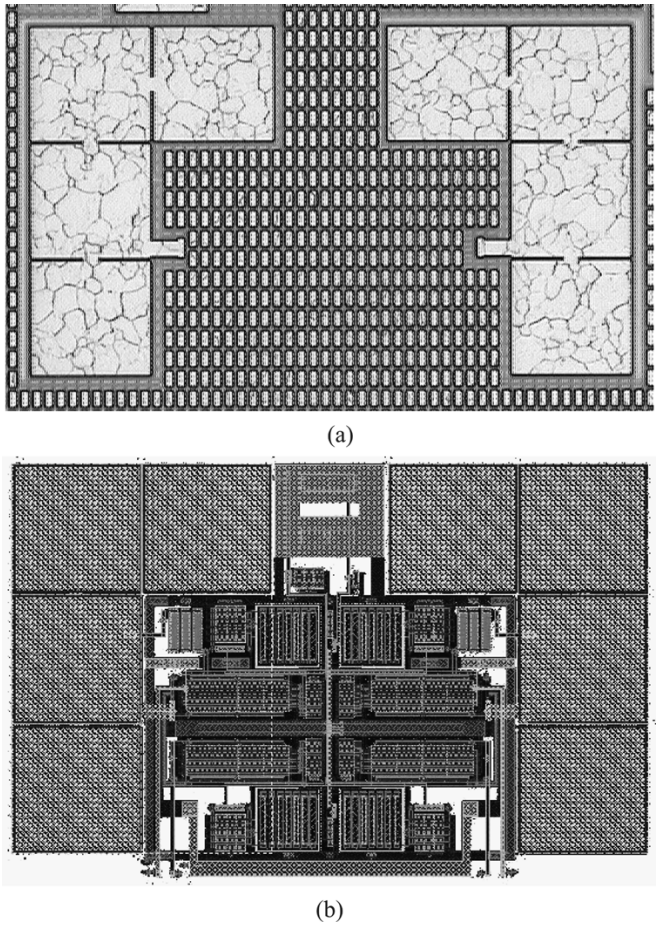


Fig. 3. (a) Chip micrograph of the body-input OTA. (b) Body-input OTA layout.

poly resistors and MIM capacitors were used. The chip micrograph is shown in Fig. 3(a) (there is exhaustive metal fill over the entire circuit), with the corresponding layout in Fig. 3(b).

B. Gate-Input OTA

The second OTA developed in this work uses gate inputs with the body terminal for biasing. To access the body terminals of nMOS devices, triple-well devices were extensively used. Fig. 4 shows an amplifier configuration using resistive feedback around an OTA. For a maximal output signal swing, the output common-mode level, $V_{cm,o}$, is typically set to $V_{\rm DD}/2$; since the input of each stage is driven from a similar stage, the input common-mode level, $V_{cm,i}$, is also $V_{\rm DD}/2$. In order to turn the input devices of the OTA on (assuming nMOS input devices), we need to set the virtual ground common level, $V_{cm,vg}$, as high as possible. Such a common level can be maintained by a resistor, R_b, shown in Fig. 4, without affecting the overall gain of the circuit [14], [15], as long as $R_f \ll A \cdot (R_i \parallel R_f \parallel R_b)$ where A is the open-loop DC gain of the amplifier. For $V_{\rm DD}$ of 0.5 V and $V_{cm,i}$, $V_{cm,o}$ of 0.25 V, to push $V_{cm,vg}$ to 0.4 V, $R_b = 2/3 \cdot (R_i \parallel R_f)$. Thus, we can use a gate-input low-voltage OTA, with the signal common-mode voltage at $V_{\rm DD}/2$, and yet maintain the OTA input devices in moderate inversion.

Current sources could be used in place of the resistors R_b [16]. A DC current pushed into the virtual ground nodes will

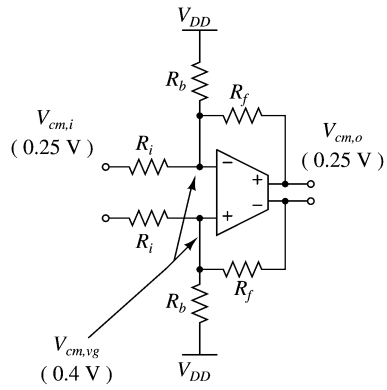


Fig. 4. Setting common-mode voltages of the gate-input OTA.

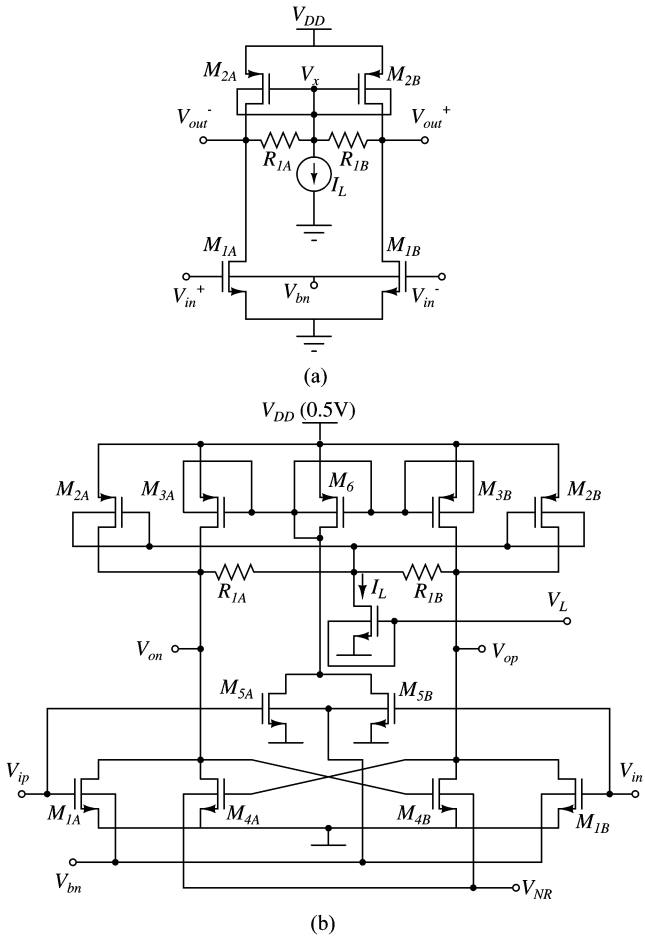


Fig. 5. Circuit development of the gate-input OTA. (a) Basic configuration. (b) Schematic of one stage of the gate-input OTA.

maintain a DC voltage drop across the feedback resistor, R_f, as well as the input resistor R_i. The current can be adjusted to maintain $V_{cm,vg}$ at the desired DC value. However, this method injects $1/f$ noise (as well as white noise) from the current source directly to the input of the OTA.

In the basic differential amplifier in Fig. 5(a), the input differential pair M_{1A} and M_{1B} and the active loads M_{2A} and M_{2B} amplify the differential input voltage. The resistors R_{1A} and R_{1B} provide common-mode feedback through the active load. A level-shifting current I_L develops a 0.15-V drop across R_{1A} and R_{1B} to maintain V_x around 0.1 V so that M_{2A} and M_{2B}

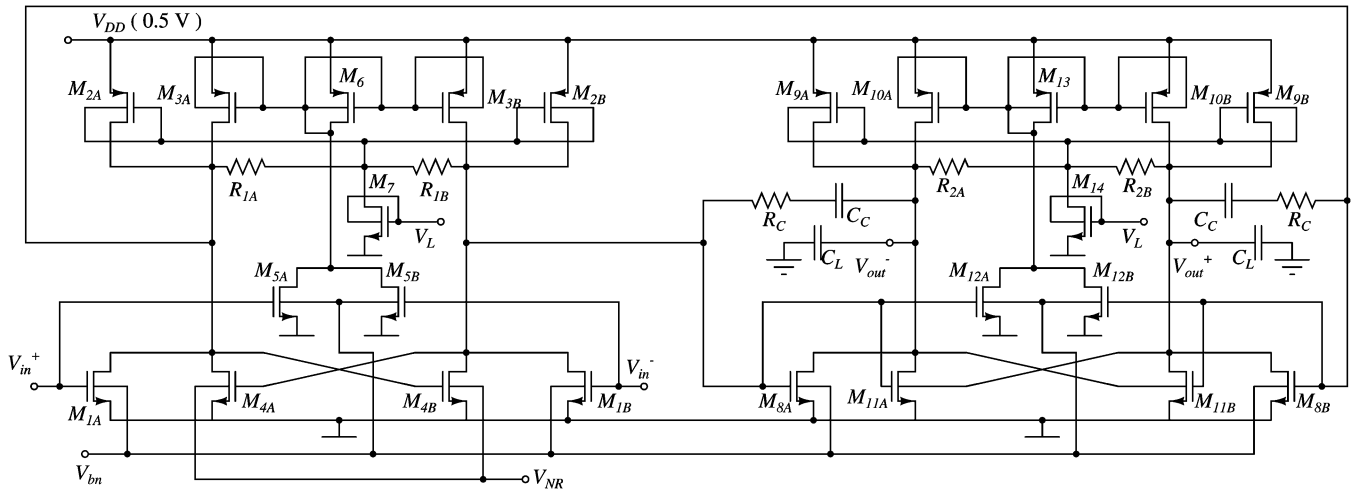


Fig. 6. Two-stage fully differential gate-input OTA with Miller compensation.

operate in moderate inversion. The bodies of M_{2A} and M_{2B} are connected to the gates to further reduce their V_T. Using the biasing arrangement shown in Fig. 4, the input common-mode voltage is maintained around 0.4 V. To lower the V_T, the body of the input devices M_{1A} and M_{1B} is forward-biased.

The ratio of the transconductance of M_{1A} and M_{1B} to the total transconductance of M_{2A} and M_{2B} sets the common-mode gain. In the process used, the pMOS transconductance is not sufficiently large compared to the nMOS transconductance to obtain a low common-mode gain. Therefore, a common-mode feed-forward cancellation path [17], [18] is added, as shown in Fig. 5, through M_{5A}, M_{5B}, M_6 and M_{3A}, M_{3B}. In M_{3A}, M_{3B} and M_6, the gate and the body are connected to each other to obtain a forward bias across the body-source junctions; this pushes these devices towards moderate inversion.

The overall DC small-signal differential gain is

$$A_{\text{diff}} = \frac{g_{m_1}}{g_{ds_1} + g_{ds_2} + g_{ds_3} + g_{ds_4} + \frac{1}{R_1} - g_{m_4}}. \quad (4)$$

The common-mode small-signal gain is given by

$$A_{cm} = \frac{g_{m_1} - 2g_{m_5}\dfrac{g_{m_3} + g_{mb_3}}{g_{m_6} + g_{mb_6}}}{g_{m_4} + g_{m_2} + g_{mb_2}}. \quad (5)$$

In this design, we made $M_3/M_6 = 0.25 \cdot M_1/M_5$ so that we get 6 dB of rejection through the common-mode feed-forward path. In our design, A_{diff} was 25 dB per stage, and A_{cm} was -10 dB per stage.

The input-referred white-noise spectral density $[\text{V}^2/\text{Hz}]$ is given by

$$8kT \cdot \frac{2}{3} \cdot \frac{1}{g_{m_1}} \left(1 + \frac{g_{m_2}}{g_{m_1}} + \frac{g_{m_3}}{g_{m_1}} + \frac{g_{m_4}}{g_{m_1}}\right) + \frac{2 \cdot 4kT}{g_{m_1}^2 R_1}. \quad (6)$$

Compared to the input-referred noise in the body-input OTA (3), the noise here is substantially less because of g_{m_1} in the denominator.

To obtain a DC gain greater than 50 dB, two gain stages are cascaded to form a two-stage OTA as shown in Fig. 6. By increasing the DC drop accross R_{1A} and R_{1B} in the first stage to 0.3 V, the output common-mode voltage of the first stage is set to about 0.4 V, which assures proper biasing of the input devices of the second stage; a DC drop of 0.15 V across R_{2A} and R_{2B} sets the output common-mode level to 0.25 V. The differential gain is further enhanced with a cross-coupled pair, M_{4A}, M_{4B}, in the first stage which acts as a negative conductance and decreases the output conductance. As an added benefit, the common-mode gain is also further reduced. The body of this cross-coupled pair is set through an on-chip automatically controlled bias voltage, V_{NR}. A similar pair, M_{11A} and M_{11B}, is added in the second stage, only its body terminal can operate from the low common voltage at the output and its body transconductance is used to provide a negative conductance; its gate transconductance is in parallel with the input transconductance. M_{11A} and M_{11B} are sized conservatively.

The OTA is stabilized through the Miller capacitors C_C across the second stage. The gain-bandwidth product is approximately $g_{m_1}/(2\pi C_C)$ and the second pole frequency of the amplifier is approximately at $g_{m_8}/(2\pi C_L)$ where C_L is the single-ended load capacitance. The series resistor R_C moves the zero introduced by C_C from the right half-plane to the left half-plane. The OTA is designed in a 0.18-μm triple-well CMOS process. A channel length of 0.36 μm was used in order to limit the influence of the reverse short-channel effect. The lengths and widths of the transistors as well as other component values are given in Table II.

C. On-Chip Biasing Circuits for the Gate-Input OTA

In this section, we discuss how the gate-input OTA can be biased reliably over process, supply voltage, and temperature. Similar techniques can be adopted to bias the body-input OTA. For proper operation, the gate-input OTA in Fig. 6 requires three biasing voltages: V_{bn}, the voltage to bias the bodies of device pairs M_1, M_5, M_8, M_{12}; V_L, to bias the level shifting current source I_L and maintain a process–temperature-independent voltage drop across R_{1A}, R_{1B}; and V_{NR}, the voltage to bias the

TABLE II
COMPONENT SIZES AND VALUES FOR THE GATE-INPUT OTAMPLIFIER (FIG. 6)

First stage			Second stage		
Transistors	W [μm]	L [μm]	Transistors	W [μm]	L [μm]
M_{1A}, M_{1B}	72	0.36	M_{8A}, M_{8B}	100	0.36
M_{2A}, M_{2B}	270	0.36	M_{9A}, M_{9B}	240	0.36
M_{3A}, M_{3B}	270	0.36	M_{10A}, M_{10B}	240	0.36
M_{4A}, M_{4B}	9	0.36	M_{11A}, M_{11B}	25	0.36
M_{5A}, M_{5B}	9	0.36	M_{12A}, M_{12A}	10	0.36
M_6	67.5	0.36	M_{13}	48	0.36
M_7	64	0.36	M_{14}	32	0.36
Resistors and Capacitors					
R_{1A}, R_{1B}	25 kΩ		R_{2A}, R_{2B}	20 kΩ	
			R_C	2 kΩ	
			C_C	3 pF	

bodies of the cross coupled pair, M_4, in the first stage of the amplifier and set the DC gain.

1) Error Amplifier: In our bias loops, we make extensive use of replica circuits in combination with active feedback loops, which require an error amplifier. We use a carefully sized inverter as an inverting error amplifier; this inverter compares the input voltage to its own switching threshold voltage and amplifies the difference. For a 0.5-V supply, the amplifier's devices operate in weak inversion, but the resulting slow frequency response can be tolerated in the DC biasing loops.

In [7], [8], [19], and [20], adaptive body bias techniques have been used to optimize the delay through critical paths in digital circuits. In this work, the switching voltage of the error amplifiers is adjusted by controlling the bodies of the nMOS devices through a negative feedback arrangement with three identical stages, as shown in Fig. 7(a). The switching threshold voltage is set to $V_{\rm DD}/2$ independent of variations in process and temperature, as follows. If the switching threshold voltage of "ErrorAmpA" is smaller than $V_{\rm DD}/2$, the input voltage of "ErrorAmpB" decreases, the output voltage of "ErrorAmpC" decreases, the body biasing of the nMOS devices is reduced, and the switching threshold voltage increases. Similarly, when the switching threshold voltage is greater than $V_{\rm DD}/2$, the feedback will react and decrease the switching threshold voltage. The feedback loop accurately sets the switching threshold voltage to 0.25 V for nominal operation. The stability of the feedback loop is established through C_{ea} with a zero-canceling series resistor R_{ea}. Every replica error amplifier biased from $V_{\rm amp}$ is now an inverting error amplifier that compares its own input to 0.25 V. The DC input–output characteristics of an inverting error amplifier are shown in Fig. 7(b). The amplifier has a gain-bandwidth of 20 kHz with a current consumption of 2 μA for a load of 1 pF.

2) Generating a Fixed Level Shift: The bias current I_L in Fig. 5(b) creates a level shift across resistors R_{1A} and R_{1B}. This level shift is essential in maintaining the pMOS devices in moderate inversion, and in maintaining the correct common-mode level for the output of the first stage of the OTA. A current source is designed using a single nMOS device. To increase the inversion level of this device, the bias voltage is applied both through the gate and the body. A replica of this current source is used in the biasing circuit as shown in Fig. 8. A current is drawn by the device which creates a voltage drop across the resistors. V_L is generated such that V_Y is 0.25 V. The corresponding drop

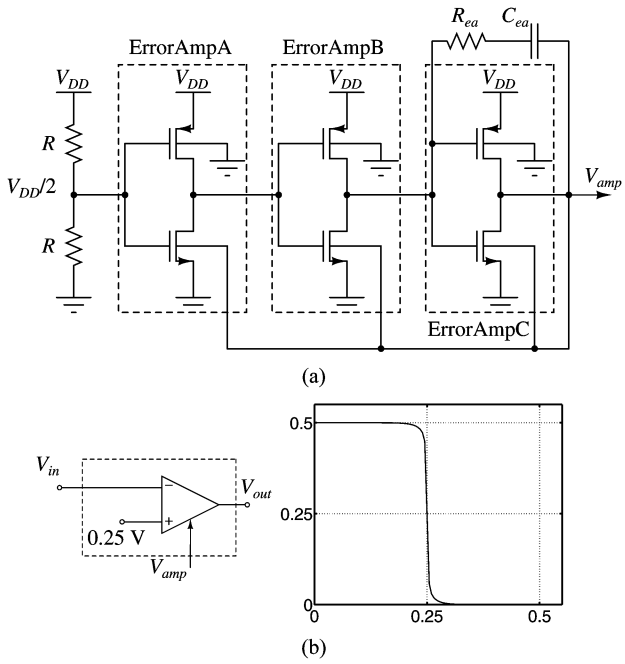


Fig. 7. (a) Error amplifier biasing loop to fix the switching threshold voltage to $V_{\rm DD}/2$. (b) DC input–output characteristics of a biased error amplifier.

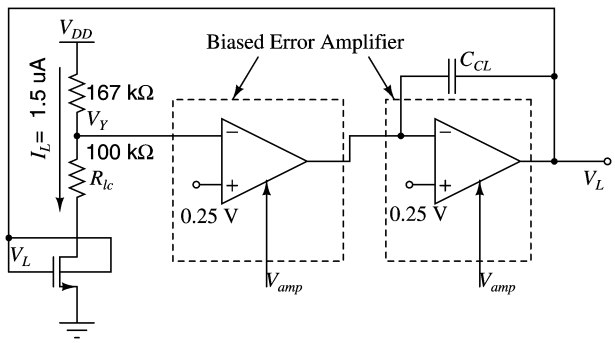


Fig. 8. Biasing the level-shifting current source.

across the 100-kΩ resistor R_{lc} is 0.15 V. This well-defined IR voltage drop is ratioed and transferred to the level shifters in Fig. 6 through M_7, R_{1A}, R_{2A} and M_{14}, R_{2A}, R_{2B}. A compensating capacitor, C_{CL}, is used to stabilize the feedback loop.

3) Setting the OTA Output DC Common-Mode Voltage: The bias voltage V_{bn} in Fig. 5(b) adjusts the biasing level of the nMOS devices compared to the pMOS devices and allows to control the DC output common-mode voltage of the OTA. As V_{bn} increases, the DC output common-mode voltage of the amplifier decreases. To generate V_{bn}, we use the circuit of Fig. 9 to sense the output common-mode of a replica of the amplifier for an input common-mode voltage of 0.4 V. In this design, this voltage, 0.4 V, is supplied externally, for nominal operation. The output common-mode voltage is compared to 0.25 V and the difference is amplified to control V_{bn} through negative feedback. A compensating capacitor, C_{bn}, is used to stabilize the feedback loop. Note that this low-bandwidth bias circuit only sets the DC value of the output common-mode voltage and adjusts it for process, temperature, and supply voltage variations. The

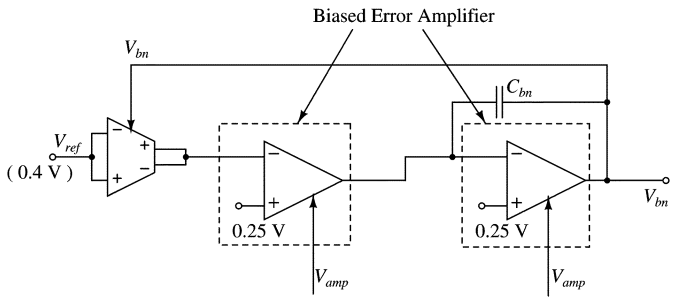


Fig. 9. Biasing bodies of input nMOS devices to set the OTA output common-mode voltage.

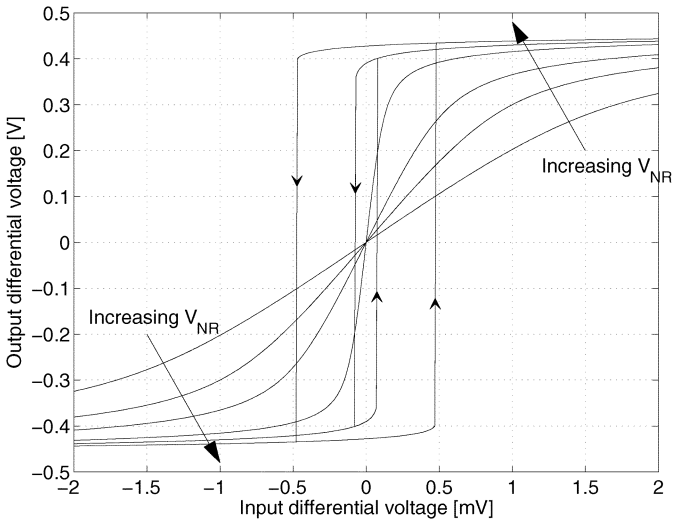


Fig. 10. OTA DC transfer characteristics as V_{NR} changes; hysteresis marked with arrows as g_{m_4} becomes too large.

rejection of common-mode signals in performed locally in each stage of each OTA.

4) Gain Enhancement: The cross-coupled pair of devices in Fig. 6, M_{4A}, M_{4B}, provides a negative resistance load to the first stage of the amplifier and enhances its gain. The amount of negative resistance can be controlled through the bodies of the two devices by changing their V_T. If $g_{m_4} = \sum_1^4 g_{ds_i} + 1/R_1$, the OTA gain is theoretically infinite; for a smaller g_{m_4}, the gain is positive, and for a larger g_{m_4}, the gain appears to be negative. A closer investigation leads to the OTA DC transfer characteristics in Fig. 10. As g_{m_4} increases, the gain first increases until it becomes infinitely large and then the amplifier develops hysteresis. An OTA with hysteresis behaves as a Schmitt trigger.

To sense the onset of this behavior, we designed an OTA-based Schmitt-trigger oscillator, shown in Fig. 11, which oscillates at a frequency given by

$$f_0 = \frac{1}{2RC} \cdot \frac{1}{\ln \frac{1+\beta}{1-\beta}}$$

where $\beta = V_{\text{hyst}}/V_{HL}$, with V_{hyst} the difference between the trigger voltages for the rising and falling edges and V_{HL} the difference between the high and low outputs. The output of the XNOR gate decreases when oscillations are present. When the oscillator amplitude is large, V_{NR} is reduced; when the oscillator ceases to oscillate, V_{NR} is increased. In practice, the determined V_{NR} will still cause oscillations in the Schmitt-trigger oscillator, which will be so fast that the XNOR gate will be too slow to respond. The loop guarantees that V_{hyst} is very small, and so the oscillation amplitude is very small and the oscillation frequency is very high. The resulting V_{NR} is converted through a gain less than, but close to, 1, and is applied to all of our OTAs, which guarantees that each OTA stage small-signal gain is positive.

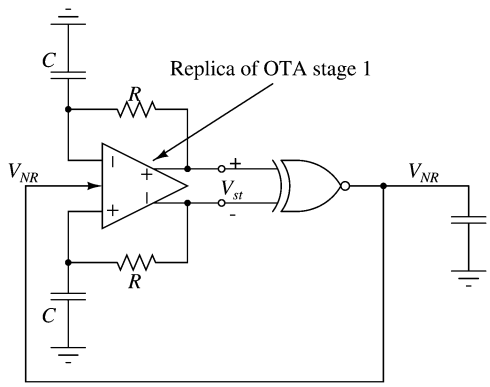


Fig. 11. Gain enhancement; general Schmitt-trigger-based oscillator and biasing technique to improve the gain of the OTA.

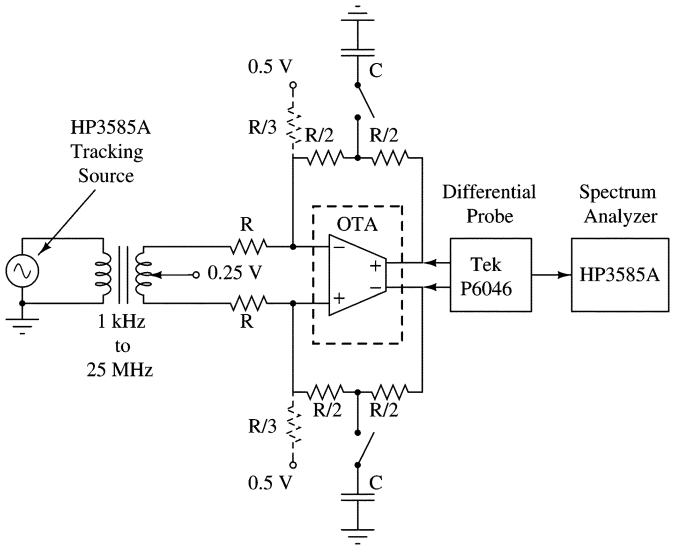


Fig. 12. General measurement setup for the body and gate-input OTAs. The switches are closed for open-loop measurements and are left open for closed-loop measurements. The dashed resistors are required for testing the gate-input OTA only. The input capacitance of the probe, C_L, is differential 10 pF.

5) Start-Up: At power-on, the error-amplifier bias circuit starts up by itself. Once V_{amp} is stable, the level-shifting current-source biasing circuit stabilizes and provides V_L. The V_{bn} biasing requires the external voltage V_{ref}, V_L and the error-amplifier bias, V_{amp}. The Schmitt-trigger-based oscillator starts up after this—it uses stable V_{bn} and V_L voltages. The forward-only dependencies in biasing ensure a smooth start-up.

D. Measurements for the Body-Input and Gate-Input OTAs

The general measurement setup is shown in Fig. 12. A transformer was used to convert a single-ended signal to differential

TABLE III
KEY PARAMETERS OF THE BODY-INPUT AND GATE-INPUT OTAS

Parameter	Body-Input OTA		Gate-Input OTA	
	Measured	Simulated	Measured	Simulated
Nominal supply voltage [V]	0.5	0.5	0.5	0.5
Power dissipation [μW]	110	100	75	100
Area [mm^2]	0.026		0.017	
Offset (standard deviation, 20 samples) [mV]	3		2	
Input current @ 27^o C [nA]	< 1	0.25	NA	NA
Open-loop DC gain [dB] (diff.)	52	48	62 42*	72 46*
Open-loop unity-gain BW [MHz] (diff.)	2.5	2.4	10.0	15.0
Slew Rate [V/μsec] (diff.)	2.89	2.92	2.0	2.7
Closed-loop unity-gain BW [MHz] (diff.) †	2.2	2.0	5.0	6.5
CMRR @ 5 kHz [dB]	78	78	74.5	85
CM input to differential output gain [dB]	-63		-56	
PSRR @ 5 kHz [dB]	76	NA	81.4	NA
Input ref. noise @ 10 kHz [nV/$\sqrt{\text{Hz}}$] † (diff.)	280	220	225	120
Input ref. noise @ 1 MHz [nV/$\sqrt{\text{Hz}}$] † (diff.)	80	90	70	100
Load capacitance [pF] (single-ended)	20	20	20	20
Output amp. for 1% HD_3 [mV p-p] (diff.) †	400		712	
Output clipping level [mV p-p] (diff.) †	520		752	

* With the gain enhancement biasing disabled.
† Measurements were done in a closed-loop inverting configuration as shown in Fig. 12. For the body-input OTA, 10 kΩ resistors were used; for the gate-input OTA, 50 kΩ resistors were used. Additional resistors from the virtual grounds to V_{DD}, of 16.7 kΩ, were used for the gate-input OTA to maintain input and output common-mode voltage levels.

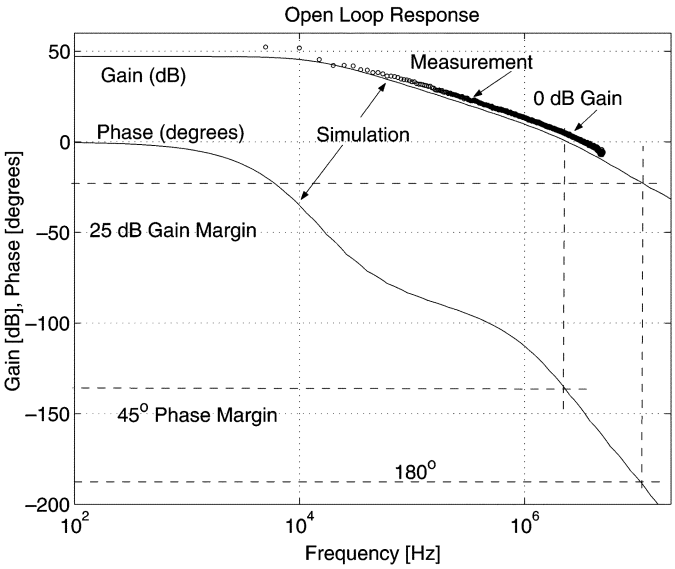


Fig. 13. Simulation and measurements of the body-input OTA in open loop.

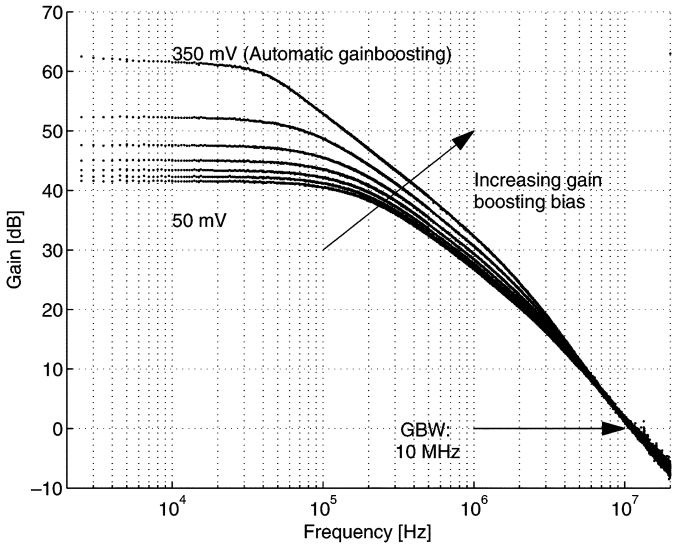


Fig. 14. Measured open-loop frequency transfer function of the gate-input OTA for different V_{NR}.

with a common-mode voltage of 0.25 V. This signal was applied to the circuit as an input. The Tektronix P6046 differential probe was used to sense the outputs of the OTA. Extensive measurements were taken using the HP3585A Spectrum Analyzer. The values of various parameters, from both measurements and simulation, are shown in Table III in the corresponding columns.

1) Body-Input OTA: The open-loop frequency response of the body-input OTA was measured at a power supply of 0.5 V, and is shown in comparison to simulated results in Fig. 13.

At voltages higher than 0.5 V, the bias currents were not changed and the input common-mode voltage was adjusted to be 0.25 V less than the power supply. As expected, the OTA worked with unchanged gain-bandwidth and a little higher current consumption. As we increased the supply from 0.5 to 1 V, the current consumption increased from 220 to 245 μA. This shows that the amplifier is robust and maintains performance over a large power supply range. As we decreased the supply voltage below 0.5 V, we adjusted the bias currents for maximum speed. At 0.4 V, the gain bandwidth product was 840 kHz with a current consumption of 66 μA and a maximum output swing of 320 mV differential peak-peak. At these low supply voltages, the gain bandwidth was largely limited by the limited available bias current from the biasing current sources, M_2 and M_4, for such low gate-source voltages.

2) Gate-Input OTA: The gate-input OTA, along with its associated bias circuits, was used in a filter, to be discussed in Section IV. A stand-alone gate-input OTA was included on the same chip as a test structure. In simulation, the design had a DC small-signal gain of 55 dB, a nominal unity gain bandwidth of 15 MHz and a phase margin of 60°. The measured open-loop frequency response of the OTA is shown in Fig. 14 for different

TABLE IV
COMPARISON WITH OTHER LOW VOLTAGE OTA DESIGNS

Parameter	[10]	[11]	[12]	[13]	[21]	[22]	Body-input OTA	Gate-input OTA
Supply [V]	1	1	0.8	0.9	1.3	0.9	0.5	0.5
DC Gain [dB]	49	70	53	70	84	59	52	62
GBW [MHz]	1.3	0.2	1.3	6kHz	1.3	4	2.5	10.0
Power [μW]	300	5	–	0.5	460	–	110	75
C_L [pF]	22	7	20	12	–	14	20	20
Single-ended (S) / Diff.(D)	S	S	S	S	S	D	D	D
Technology [μm]	2	0.35	0.5	2.5	0.7	0.5	0.18	0.18
Devices	Lat. BJT	–	Lat. BJT	Depl. MOS	–	–	–	Triple well
100 η [1/V] *	9.5	28	–	13	–	–	22.7	133.4

$$^{*}\ \eta = \frac{\text{GBW} \cdot C_L}{I_{\text{supply}}}$$

V_{NR}. The negative resistor bias circuit automatically sets V_{NR} such that the OTA DC gain is 62 dB. These measurements were done for a load resistor of 50 kΩ. The DC gain is expected to be much higher for smaller loading.

E. Discussion on the Two OTA Design Techniques and Comparisons

We compare the two designed OTAs with measured results of other low-voltage CMOS OTA designs in Table IV. The gate-input OTA performs better than the body-input OTA in terms of gain-bandwidth and power consumption. This is primarily due to the use of g_m of the input devices as opposed to g_{mb}. The input-referred noise is also smaller in the gate-input OTA. However, when the gate-input OTA is used in feedback, extra resistors are required to set the input common-mode voltage as in Fig. 4. This adds resistor white noise directly at the inputs of the OTA and significantly contributes to the total noise of the circuit in a feedback configuration. The body-input OTA has a large input common-mode range and has functionality for all input common-mode voltages from 0 to 0.5 V. The common-mode gain increases at low input common-mode voltages. The gate-input OTA, on the other hand, is designed to have large gain only at input common-mode voltages larger than 0.4 V.

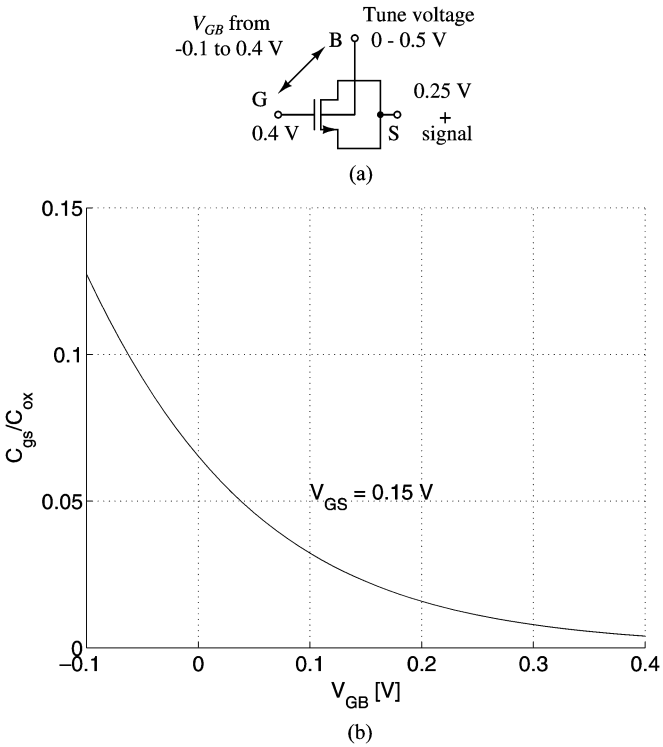


Fig. 15. (a) Gate (G) to source/drain (S) capacitance tuned by body (B). (b) Normalized capacitance as a function of V_{GB} for different V_{GS}. $N_a = 3.5 \times 10^{17}$ cm^{-3}, $V_{FB} = -1$ V.

III. WEAK INVERSION MOS VARACTORS FOR TUNABLE INTEGRATORS

A tunable integrator is the basic building block of a tunable filter. Traditionally, tunability can be accomplished using a MOSFET-C structure with MOS devices replacing resistors, or using switches and banks of resistors and capacitors for discrete tuning, or using transconductance-C techniques, or using a varactor-R structure with varactors replacing capacitors. A MOSFET-C structure typically requires the MOS devices to be in strong inversion, which might not be feasible given the ultra-low supply voltage requirement. Using switches in the signal path would require voltage boosting to turn on the switches, which raises reliability concerns. The design of highly linear tunable transconductors at very low supply voltages is very challenging. We have thus investigated the use of varactor-R techniques. Variable capacitors, along with resistors and low-voltage OTAs, enable us to build active-RC circuits at 0.5 V. For this, we propose the use of a weak-inversion MOS capacitor as a three-terminal varactor, with the capacitance between the gate and the combination of drain and source, denoted here as C_{gs}, and the tuning voltage applied at the body [23], as shown in Fig. 15(a). In strong inversion and in accumulation, this capacitance is the oxide capacitance C_{ox}. In depletion, the intrinsic capacitance is zero as there is no inversion layer. From weak to moderate inversion through strong inversion, the intrinsic C_{gs} changes from zero to C_{ox}. Changing the body voltage changes the device threshold voltage V_T and also changes the inversion level of the device. This changes C_{gs} and the device now behaves as a three-terminal varactor.

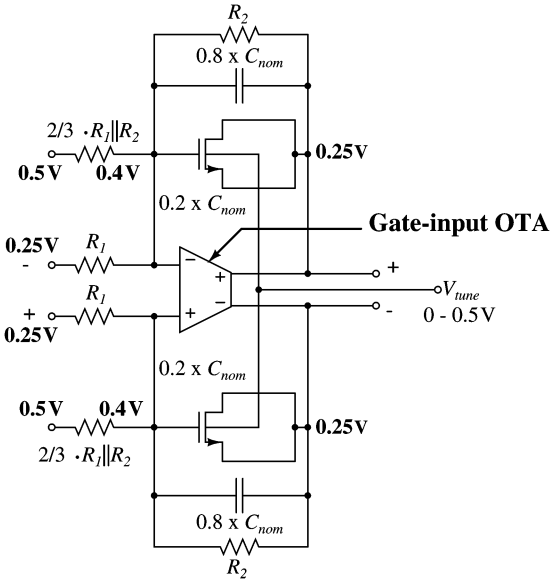


Fig. 16. 0.5-V tunable damped integrator. DC common-mode voltages of the different nodes are shown in bold.

A long-channel nMOS device (15 fingers, each of width 100 μm and length 20 μm) was fabricated on a 0.18-μm triple-well CMOS process, with the body accessible through the p-well and the drain and source shorted together. The normalized gate-source capacitance of this device, for different bias voltages, is shown in Fig. 15(b). In this fabrication process, at an operating point for V_{GS} of 0.15 V, the capacitance varies from 0 to 0.1 C_{ox}, over the range of V_{GB} from -0.1 to 0.4 V.

The implementation of a low-voltage tunable damped integrator, using the proposed varactors and a gate-input OTA, is shown in Fig. 16. Resistors to $V_{\rm DD}$ at the inputs of the gate-input OTA maintain a common level of 0.4 V at the virtual grounds when the integrator input and output common-mode voltages are 0.25 V, and do not affect the transfer function of the integrator.

With a V_{GS} of 0.15 V, in the process used, the proposed varactor has a low capacitance density of about 0.3 fF/μm^2. This limitation is offset by adding a fixed capacitor in shunt with the variable capacitor. Any available fixed capacitor type can be used, and, to satisfy the area restrictions for our prototype, we use native devices (zero-V_T) as the fixed capacitors; they operate in strong inversion under the above biasing conditions and have a density of 8 fF/μm^2. This gives us an overall capacitance density of 1.3 fF/μm^2. An added benefit is a better quality factor for the composite capacitance. If the fixed capacitor is linear, the linearity of the composite varactor is improved. In this implementation, the fixed capacitor was chosen to be 80% of the nominal capacitance required, and the varactor was sized to be 20% of the nominal capacitance at the center of its range. This enables a tuning range of $\pm$20%.

The varactor was measured and characterized using the Agilent 4284A LCR meter. The measured effective capacitance and series resistance are defined in Fig. 17(a). The effective capacitance is shown in Fig. 17(b) as a function of V_{GS} for different V_{GB}. Due to the lack of a strong inversion layer, there is a significant resistance in series with the capacitance, that can be attributed to distributed effects, which reduces the

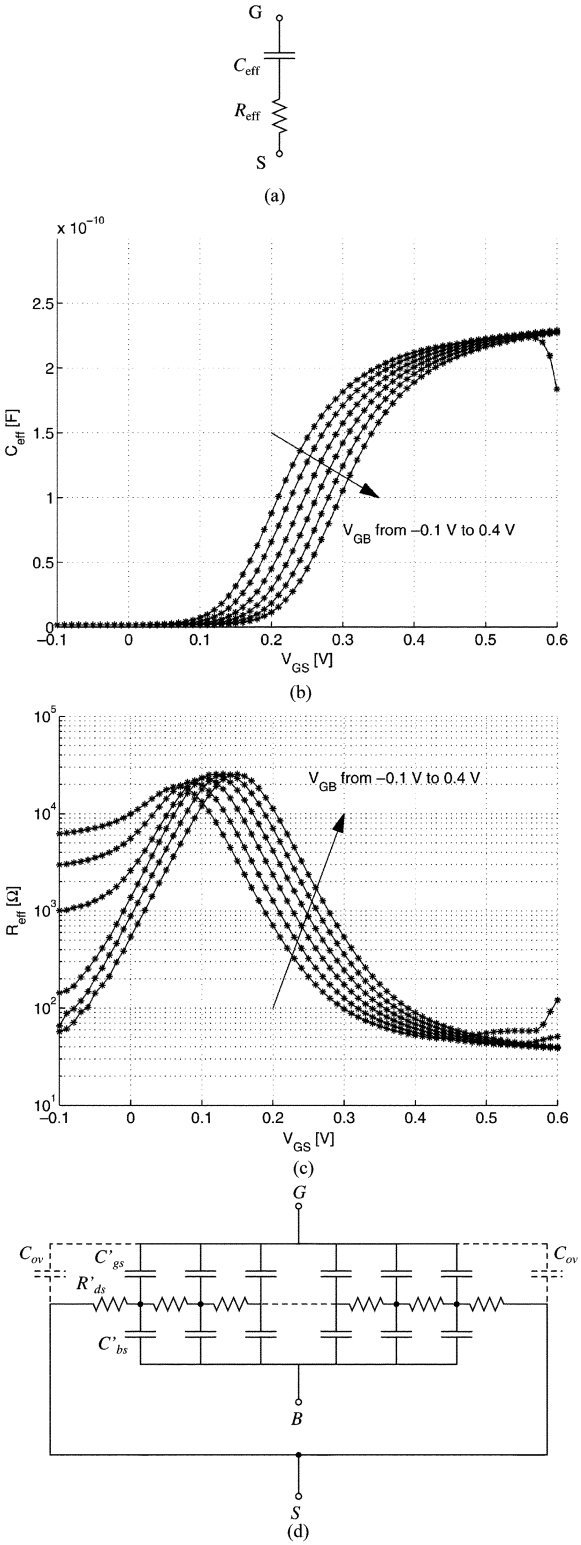


Fig. 17. (a) Lumped model of the capacitor showing effective capacitance and series resistance. (b) Measured effective capacitance, $C_{\rm eff}$, and (c) series resistance, $R_{\rm eff}$, as a function of V_{GS} for different V_{GB}. A measurement frequency of 1 MHz was used. (d) Conceptual model of the capacitor. C'_{gs}, C'_{bs}, and R'_{ds} are the gate to source/drain capacitance per unit length, body to source/drain capacitance per unit length, and drain to source resistance per unit length, respectively.

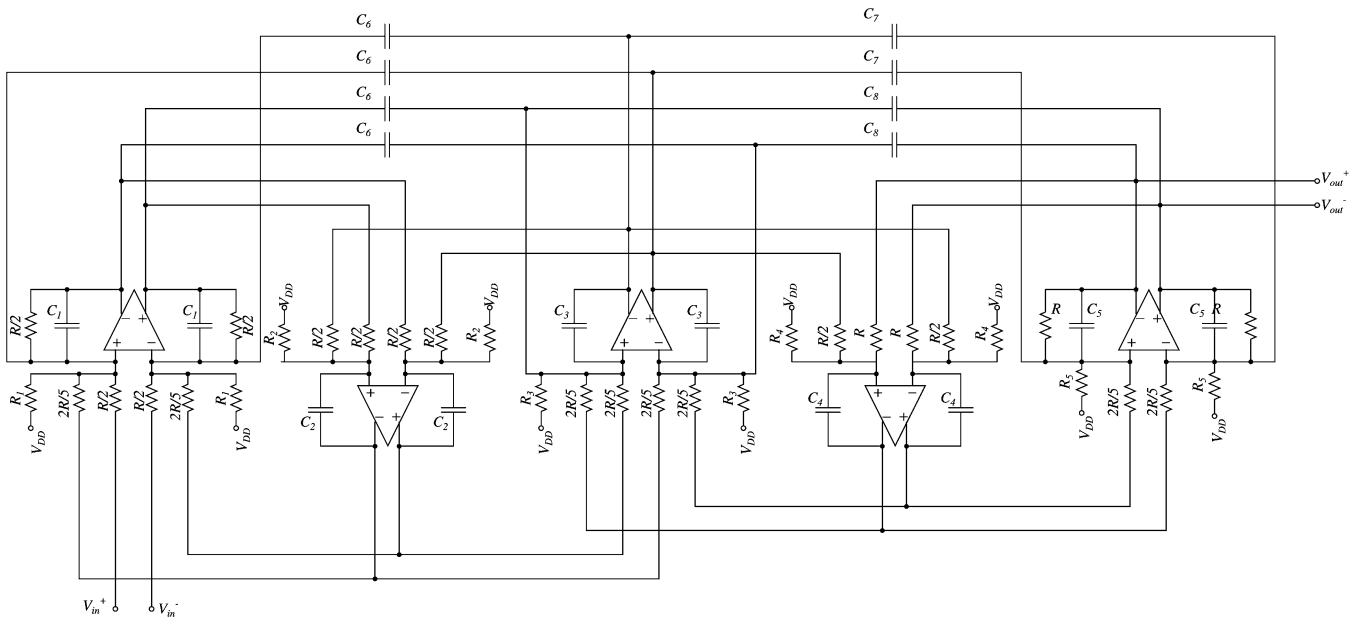


Fig. 18. Low-voltage fifth-order low-pass elliptic filter.

quality factor of the capacitor. The resistance measured in series with the capacitance at 1 MHz is shown in Fig. 17(c) and a distributed model to predict this is shown in Fig. 17(d). Techniques to accurately predict the series resistance have been discussed in [24]. More details on the varactor modeling are given in the Appendix.

IV. 0.5-V Fifth-Order Active-RC Filter

A. Filter Topology

To demonstrate the capabilities and synergy of the proposed ultra-low-voltage design techniques, we designed a fifth-order low-pass elliptic filter with a 135-kHz cut-off frequency. For minimum sensitivity requirements, a leap-frog topology was used. The design in [25] was frequency-scaled to 135 kHz, such that the signal amplitude maxima at all OTA outputs are at the same level. The sizing of the individual gate-input OTAs is scaled depending on the loading requirements, by connecting multiple units in parallel, with all internal nodes of the OTAs connected to each other. This allows comparable phase and distortion performance for all five stages. To obtain an accurate transfer characteristic, the OTA should have substantial open-loop gain all the way up to 280 kHz, the second zero of the filter. The proposed amplifier has a worst case gain of 20 dB at 280 kHz, which is sufficient. The filter resistors and capacitors were scaled so that the total noise contributions from the OTAs and from the resistors, integrated in the passband, are equal. The schematic is presented in Fig. 18, with component values given in Table V.

The simulated overall dynamic range—ratio of input rms value at which there is 1% total harmonic distortion (THD) to the input referred noise—is 57 dB. The varactors contribute substantially to the distortion of the circuit. Using ideal linear capacitors instead of varactors, the simulated dynamic range is 69 dB, whereas, using ideal OTAs instead of the low-voltage OTAs, the simulated dynamic range is only 58 dB.

TABLE V
Filter Resistor and Capacitor Values

Capacitor	Value	Resistor	Value
C_1	9.2 pF	R	300 kΩ
C_2	13.1 pF	R_1	30 kΩ
C_3	20.2 pF	R_2	50 kΩ
C_4	8.8 pF	R_3	40 kΩ
C_5	5.3 pF	R_4	66.7 kΩ
C_6	1.8 pF	R_5	57.2 kΩ
C_7	5.7 pF		
C_8	2.9 pF		

B. On-Chip PLL-Based Automatic Frequency Tuning Loop

An ultra-low-voltage voltage-controlled oscillator (VCO), shown in Fig. 19, was built using tunable integrators with the resistors and capacitors matched to those in the filter. The oscillator frequency, f_0, was chosen to be close to the second zero of the filter, 280 kHz. A three-stage oscillator was chosen in preference to a double-integrator oscillator. The OTAs have enough gain-bandwidth to set a phase lag of 60° per stage along with the required gain of greater than 1, at f_0, to reliably sustain oscillations. The oscillator has a nominal frequency of oscillation given by

$$f_0 = \frac{\sqrt{3}}{2\pi R_a C_a}$$

and oscillations are possible only when $R_a \geq 2R_b$. In Fig. 19, R_a is 427 kΩ, R_b is 207 kΩ, R_{VDD} is 93 kΩ, and C_a is 2.3 pF.

A phase-locked loop (PLL) is built around the VCO using an XOR gate as a phase detector. With a 0.5-V power supply voltage, the devices in the XOR gate are in weak inversion, but they are still sufficiently fast for 280 kHz. This detector compares the VCO frequency to an external reference clock and controls the body voltage of the capacitors in the VCO, until the PLL is in lock. The same capacitor body voltage is applied to the filter as well. The filter varactors and resistors are matched to those in the VCO and, in this manner, the corner frequency of the filter

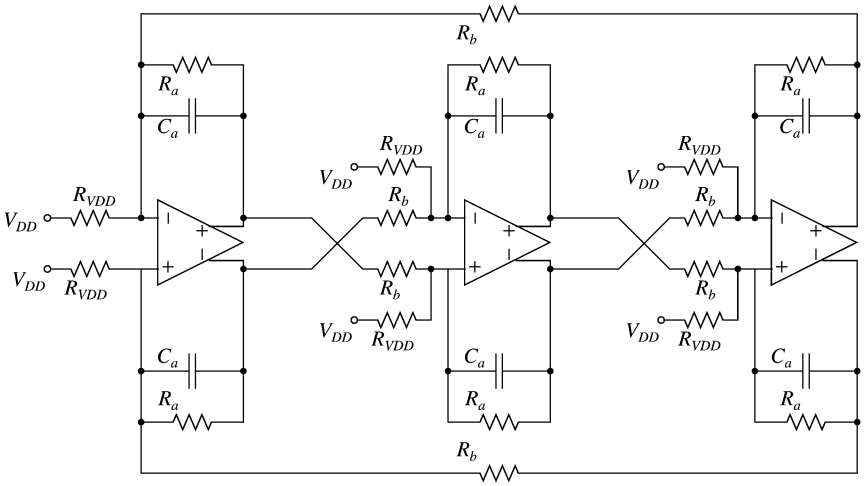
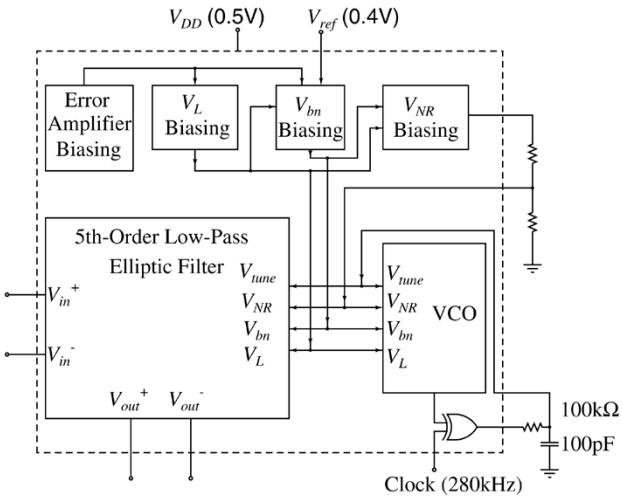
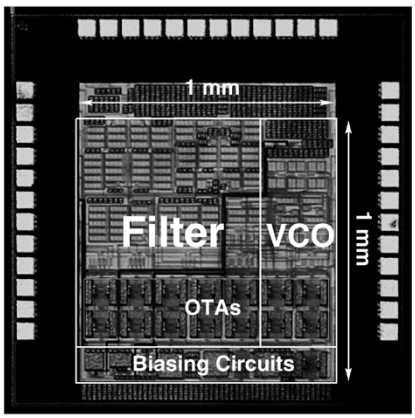


Fig. 19. Three-stage low-voltage oscillator schematic.



(a)



(b)

Fig. 20. (a) Block diagram of the full chip. (b) Die photograph.

is tuned. For characterization flexibility, a first-order PLL loop filter is built externally using discrete components.

C. Prototype Chip

The full chip, shown in Fig. 20(a), containing the fifth-order filter, VCO, bias circuits, and phase detector, was fabricated on a 0.18-μm CMOS process, taking advantage of triple-well nMOS devices, high resistivity resistors, and MIM capacitors. The total active chip area is 1 mm $\times$ 1 mm. The die photograph is shown in Fig. 20(b). Only one external voltage reference of 0.4 V is used for biasing. An external frequency reference of 280 kHz is used to tune the filter.

D. Characterization Results

1) Test Set-Up: A center-tap transformer was used to convert a single-ended signal to a differential signal with a common-mode voltage of 0.25 V. A Tektronix P6046 differential probe was used to measure the differential outputs of the filter. Extensive measurements were taken using the HP3585A Spectrum Analyzer. Results are reported in Figs. 21–23 and in Table VI.

2) Frequency Response: The measured filter frequency response agrees closely to simulation, as shown in Fig. 21(a). The pass-band ripple is 1 dB. Fig. 21(b) shows the frequency response of the filter with and without automatic gain-enhancement. With gain-enhancement, the filter response improved by 1 dB in the pass-band. With a 10-kHz common-mode tone, the measured common-mode rejection ratio (CMRR) was 65 dB. With a 10-kHz tone on the power supply, the measured power supply rejection ratio (PSRR) was 43 dB. Better PSRR can be achieved if we use a separate regulated power supply for all the biasing resistors, R_b, as in Fig. 4.

3) Noise: The measured output noise is compared to simulation in Fig. 22. At low frequencies, the output noise is dominated by $1/f$ noise; the small flat region in the passband of the filter is a result of white noise. The later peaking at around 135 kHz is a result of the filter topology and transfer function. The observed $1/f$ noise corner is about 40 kHz. The OTAs contribute to the noise at lower frequencies while the filter resistors dominantly contribute beyond the $1/f$ noise corner frequency.

4) Distortion and Characterization Over Tuning Range: Harmonic distortion was measured for an in-band tone of 20 kHz for which the harmonics are also in-band, and for an in-band tone of 100 kHz for which the harmonics are out-of-band. In the worst case, a 1% THD was observed at an input rms differential voltage of 50 mV. Intermodulation

TABLE VI
PERFORMANCE AT DIFFERENT POWER SUPPLY VOLTAGES, WITH THE PLL ENABLED

V_{DD} [V]		0.45	0.5	0.55	0.6
-3 dB cut-off frequency [kHz]		135.0	135.0	135.0	135.0
Total current [mA]		1.5	2.2	3.3	4.3
Noise† [μV rms]		87	74	68	65
Input‡ [mV rms] (20kHz / 1% THD)		80	80	80	80
Input‡ [mV rms] (100kHz / 1% THD)		50	50	50	50
In-band IIP_3 [dBV]		-5	-3	-3	-3
Out-of-band IIP_3 [dBV]		3	5	3	5
Dynamic range* [dB]		55.2	56.6	57.3	57.7
Tuning range [kHz]	$V_{tune} = V_{DD}$	96	88	84	69
	V_{tune} = 0.0 V	153	154	148	150
PLL tone feed-through [μV rms] @280 kHz		104	85	72	72

† : Input-referred, differential, integrated over 1kHz to 150kHz
‡ : Differential
* : Ratio of input @100kHz for 1% THD to integrated input noise

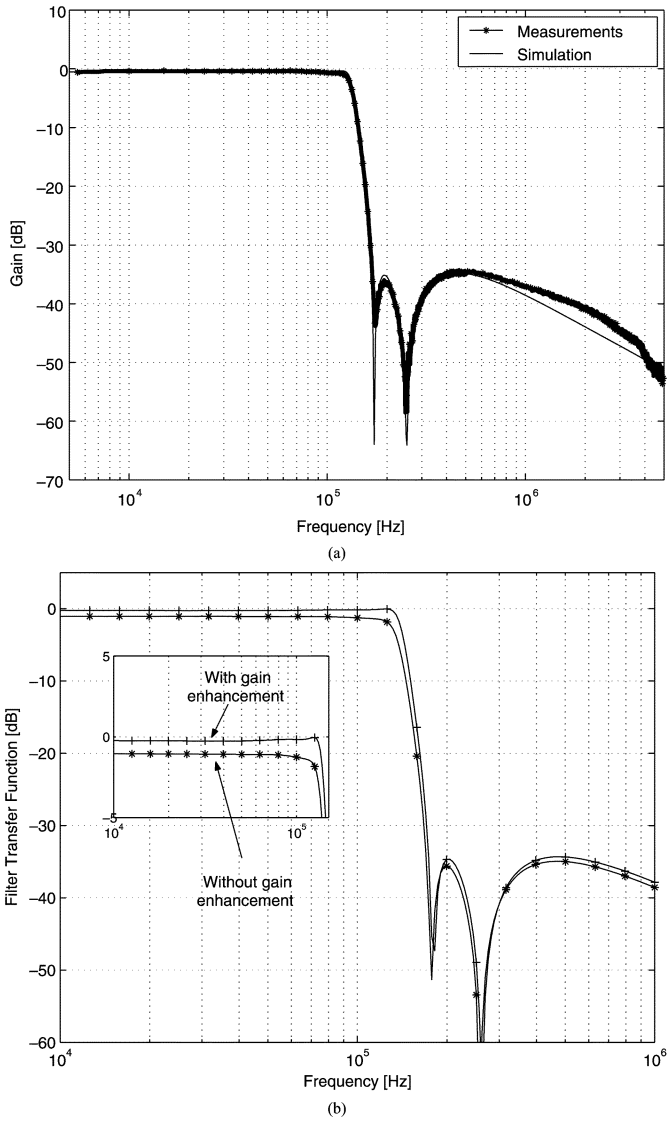


Fig. 21. Frequency response of the filter. (a) Simulation and measurement. (b) With and without gain enhancement.

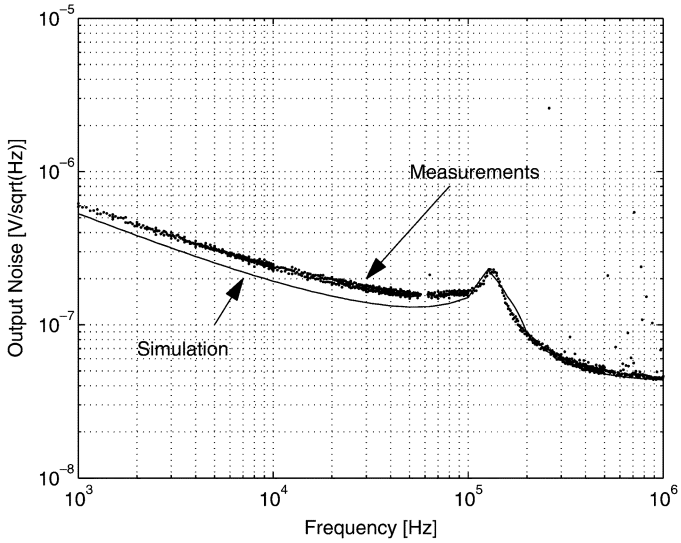
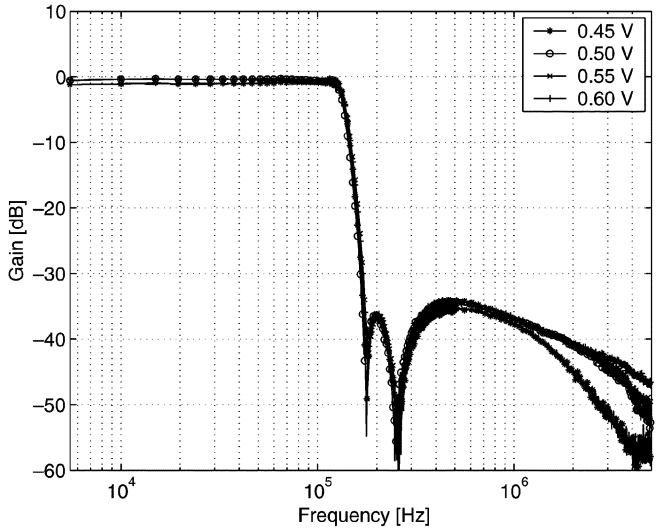


Fig. 22. Simulation and measurement of filter noise for 0.5-V supply voltage (output noise).

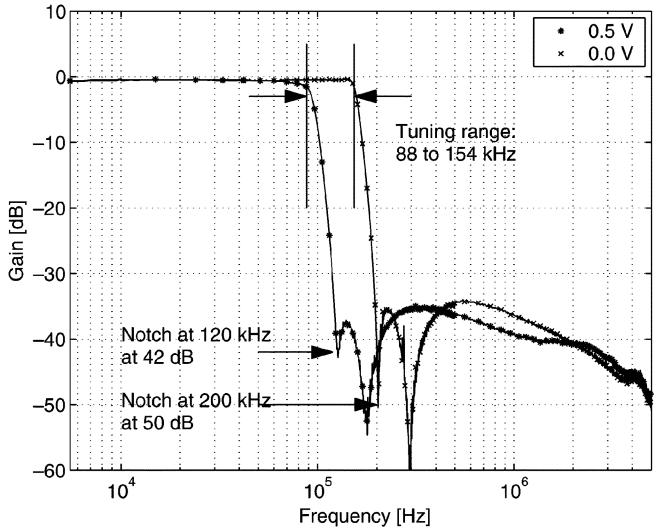
measurements were taken for a pair of in-band input tones at 40 and 60 kHz such that their intermodulation products are at 20 and 80 kHz, and also for a pair of out-of-band input tones at the two peaks in the stop-band, nominally at 180 and 460 kHz. The respective input rms differential IIP_3s observed are -3 and 5 dBV. For this paper, dynamic range is defined as the ratio of the input differential rms voltage at which there is 1% THD (worst case) to the input integrated noise [25] from 1 to 150 kHz. The observed dynamic range was 56.6 dB, which is in close agreement with the simulated dynamic range of 57 dB.

To observe the contribution of the varactor to the distortion of the filter, the PLL was deactivated, and the distortion was measured for different tuning voltages applied through the bodies of the varactors. For a tuning voltage of 0.0 V, the capacitance nonlinearity is eliminated as the capacitors consist of fixed strong inversion transistors in shunt with only the overlap capacitance of the varactors. The observed dynamic range is 61 dB at this tuning voltage. For a tuning voltage of 0.5 V, the observed dynamic range decreases to 55 dB.

The frequency response of the filter at different tuning voltages, with the PLL deactivated, is shown in Fig. 23(b). The depths of the filter notches in Fig. 23(b) depend on the OTA gain and on the quality factor of the capacitors. For the fifth-order filter, to obtain the effect of the series resistance, the varactor



(a)



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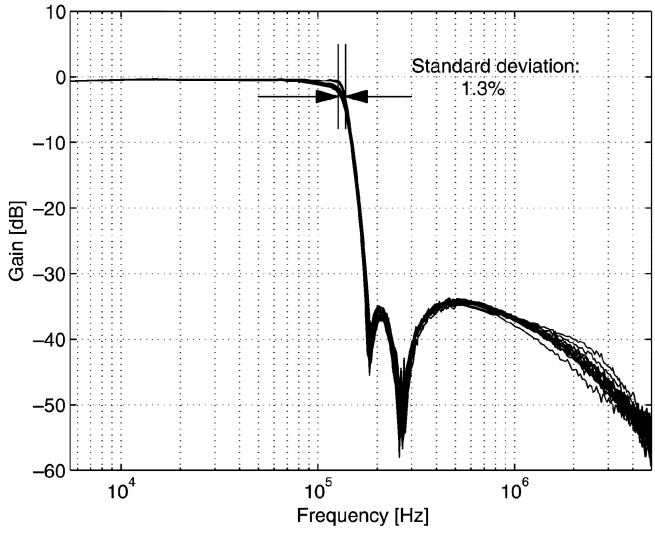

(c)

Fig. 23. (a) Measured filter frequency response at different power supply voltages (PLL active). (b) Measured frequency response at different tune voltages (PLL disabled). (c) Measured frequency response for 20 chips (PLL active).

TABLE VII
MEASURED TOTAL CURRENT CONSUMPTION AT DIFFERENT TEMPERATURES

Temperature [^{o} C]	5	25	50	85
Total current [mA] (measured)	1.8	2.2	2.5	3.0
Total current [mA] (simulated)	1.9	2.2	2.6	2.9

was simulated by including a calculated resistance (see the Appendix) in series with the device, as well as by using a segmented model (see the Appendix). The simulated depths of the first notch in Fig. 23(b), in either case, at body tuning voltages of 0.0 and 0.5 V are -53 and -46 dB, as opposed to measured -50 and -43 dB, respectively. The difference of 3 dB in both cases can be attributed to differences in the OTA gain-bandwidth product.

5) Performance at Different Power Supply Voltages: The performance of the filter was evaluated at different power supply voltages and is summarized in Table VI. The PLL locks under nominal conditions at these different power supply voltages and all measurements, except the filter tuning range were taken with the PLL active. The filter transfer function for different power supply voltages is shown in Fig. 23(a).

6) Performance Over Different Chips: The nominal performance was evaluated for a batch of 20 chips. The filter -3 dB cut-off frequency had a standard deviation of 1.3%. The measured filter characteristics of different chips are shown in Fig. 23(c) and are found to agree closely. The mean current consumption at 0.5 V was 2.2 mA with a standard deviation of 0.1 mA.

7) Performance Over Temperature: A Delta Design 3900 temperature chamber was used to characterize the filter at different temperatures. The chip was fully functional from 5 °C to 85 °C and no leakage problems were observed. The -3 dB cut-off frequency had a variation of $\pm 8\%$ over this range. This somewhat large deviation was diagnosed to be a systematic shift in the VCO characteristic over temperature, caused by relative amplitude variations, which are significant at the 0.5-V supply voltage used. This can be fixed with additional oscillator amplitude stabilization circuitry. The nominal current consumption at different temperatures is shown in Table VII. Device threshold voltages decrease with increasing temperature. The biasing circuits establish fixed DC bias voltages independent of temperature. As a result, current consumption increases with temperature.

V. CONCLUSION

We have presented design techniques for true ultra-low-voltage analog CMOS circuits. No voltage boosting is used and all nodes in the circuits are within the power rails. The designs were nominally done for a 0.5-V power supply, equal to the threshold voltage of the individual devices. Two OTA design techniques have been shown along with automatic biasing techniques to control the common-mode voltage levels and to maximize signal swings over process, voltage, and temperature. A weak inversion MOS varactor has been analyzed and modeled. Together with gate-input OTAs, such varactors were used in a fully integrated tunable fifth-order active-RC low-pass filter and a matched VCO. The VCO is embedded in a PLL

that is used to tune the frequency response of the filter. The OTAs and the varactors used are generic analog circuit building blocks and can be used in a variety of other designs at similar power supply voltage levels.

APPENDIX
TECHNIQUES TO MODEL THE VARACTOR SERIES RESISTANCE

We define the gate-source transadmittance, Y_{gs}, by I_g/V_s, where V_s is a voltage phasor applied to the source/drain terminal and I_g is a current phasor leaving the gate terminal, with V_B and V_G constant. Distributed analysis techniques, as discussed in [24], show that the effective transadmittance, $Y_{gs}(j\omega)$, (not including overlap capacitance), starting from the model in Fig. 17(d) and letting the number of sections go to infinity, is given by

$$Y_{gs}(j\omega) = j\omega C_{gs}\frac{\tanh\alpha/2}{\alpha/2} \tag{7}$$

where $\alpha = \sqrt{j\omega R_{ds}(C_{gs}+C_{bs})}$. C_{gs}, C_{bs}, and R_{ds} are the lumped gate to source/drain capacitance, body to source/drain capacitance, and source to drain resistance, respectively. The intrinsic transadmittance, Y_{gs}, can now be combined with the overlap capacitance, and then transformed to extract the effective series resistance and series capacitance. The effective gate-source capacitance is now given by

$$C_{\text{eff}} = -\frac{1}{\omega\cdot\text{Im}\{1/[Y_{gs}(j\omega)+2j\omega C_{\text{overlap}}]\}}. \tag{8}$$

The effective series resistance is given by

$$R_{\text{eff}} = \text{Re}\left\{\frac{1}{Y_{gs}(j\omega)+j\omega 2C_{\text{overlap}}}\right\}. \tag{9}$$

If R_{ds}, C_{bs}, or C_{gs} at any bias point are found using a given MOS model, (7), (8), and (9) can be used to extract the effective series resistance and capacitance at the frequency of interest.

The distributed effect can also be quickly simulated using a standard circuit simulator by using channel segmentation [4], as in Fig. 17(d). A long-channel MOS device can be viewed as a series connection of several short intrinsic MOS devices with the drains and sources of adjacent devices connected to each other. If a device of length L μm is broken into N segments, each of the channel segments has length of L/N μm. As the number of segments N becomes larger, this will approach a truly distributed model. It can be shown that for a segmented model, the number of segments N should be such that at the frequency of interest, $\omega R_{ds}(C_{gs}+C_{bs})/2N^2 \ll 1$. Note that for $N=1$, $Y_{gs}(jw)$ is purely imaginary, and the series resistance predicted is zero.

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REFERENCES

[1] The International Technology Roadmap for Semiconductors (2004 Edition) [Online]. Available: http://public.itrs.net
[2] S. Chatterjee, Y. Tsividis, and P. Kinget, "A 0.5-V bulk-input fully differential operational transconductance amplifier," *Proc. 30th ESSCIRC*, pp. 147–150, Sep. 2004.
[3] ——, "A 0.5 V filter with PLL-based tuning in 0.18-μm CMOS technology," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2005, pp. 506–507.
[4] Y. Tsividis, *Operation and Modeling of the MOS transistor*, 2nd ed. New York: Oxford Univ. Press, 1999.
[5] M.-J. Chen, J.-S. Ho, T.-H. Huang, C.-H. Yang, Y.-N. Jou, and T. Wu, "Back-gate forward bias method for low-voltage CMOS digital circuits," *IEEE Trans. Electron Devices*, vol. 43, pp. 904–910, 1996.
[6] S. Narendra, J. Tschanz, J. Hofsheier, B. Bloechel, S. Vangal, Y. Hoskote, S. Tang, D. Somasekhar, A. Keshavarzi, V. Erraguntla, G. Dermer, N. Borkar, S. Borkar, and V. De, "Ultra-low voltage circuits and processor in 180 nm to 90 nm technologies with a swapped-body biasing technique," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2004, pp. 156–157.
[7] J. W. Tschanz, J. T. Kao, S. Narendra, R. Nair, D. Antoniadis, and A. P. Chandrakasan, "Adaptive body bias for reducing impacts of die-to-die and within-die parameter variations on microprocessor frequency and leakage," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1396–1402, Nov. 2002.
[8] V. R. Kaenel, M. D. Pardoen, E. Dijkstra, and E. A. Vittoz, "Automatic adjustment of threshold and supply voltages for minimum power consumption in CMOS digital circuits," in *Proc. IEEE Symp. Low Power Electronics*, 1994, pp. 78–79.
[9] A. Guzinski, M. Bialko, and J. Matheau, "Body driven differential amplifier for application in continuous-time active-C filter," in *Proc. ECCD*, 1987, pp. 315–319.
[10] B. Blalock, P. Allen, and G. Rincon-Mora, "Designing 1-V op-amps using standard digital CMOS technology," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 45, no. 7, pp. 769–780, Jul. 1998.
[11] K. Lasanen, E. Raisanen-Ruotsalainen, and J. Kostamovaara, "A 1-V 5 μW CMOS-opamp with bulk-driven input transistors," in *43rd IEEE Midwest Symp. Circuits and Systems*, 2000, pp. 1038–1041.
[12] T. Lehmann and M. Cassia, "1-V power supply CMOS cascode amplifier," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1082–1086, Jul. 2001.
[13] T. Stockstad and H. Yoshizawa, "A 0.9-V 0.5-μA rail-to-rail CMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. 37, pp. 286–292, 2002.
[14] S. Karthikeyan, S. Mortezapour, A. Tammineedi, and E. Lee, "Low-voltage analog circuit design based on biased inverting opamp configuration," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 3, pp. 176–184, Mar. 2000.
[15] K. Bult, "Analog design in deep sub-micron CMOS," in *Proc. ESSCIRC*, Sep. 2000, pp. 11–17.
[16] H. Huang and E. K. F. Lee, "Design of low-voltage CMOS continuous-time filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1168–1177, Aug. 2001.
[17] A. Baschirotto, F. Rezzi, and R. Castello, "Low-voltage balanced transconductor with high input common-mode rejection," *Electron. Lett.*, vol. 30, no. 20, pp. 1669–1671, Sep. 1994.
[18] F. Rezzi, A. Baschirotto, and R. Castello, "A 3 V 12–55 MHz BiCMOS pseudo-differential continuous-time filter," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 42, no. 11, pp. 896–903, Nov. 1995.
[19] T. Kobayashi and T. Sakurai, "Self-adjusting threshold-voltage scheme (SATS) for low-voltage high-speed operation," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 1994, pp. 271–274.
[20] J. T. Kao, M. Miyazaki, and A. P. Chandrakasan, "A 175-mV multiply-accumulate unit using an adaptive supply voltage and body bias architecture," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1545–1554, Nov. 2002.
[21] G. Ferri and W. Sansen, "A 1.3 V op/amp in standard 0.7 μm CMOS with constant g_m and rail-to-rail input and output stages," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, vol. 478, 1996, pp. 382–383.
[22] V. Peluso, P. Vancorenland, A. M. Marques, M. Steyaert, and W. Sansen, "A 900-mV low-power $\Delta\Sigma$ A/D converter with 77-dB dynamic range," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 1887–1897, Dec. 1998.
[23] S. Chatterjee, T. Musah, Y. Tsividis, and P. Kinget, "Weak inversion MOS varactors for 0.5 V analog integrated filters," in *Proc. Symp. VLSI Circuits*, Jun. 2005, pp. 272–275.

[24] M. S. Ghausi and J. J. Kelly, *Introduction to Distributed-Parameter Networks*. New York: Holt, Rinehart and Winston, 1968.
[25] M. Banu and Y. Tsividis, "An elliptic continuous-time CMOS filter with on-chip automatic tuning," *IEEE J. Solid-State Circuits*, vol. SC-20, no. 12, pp. 1114–1121, Dec. 1985.

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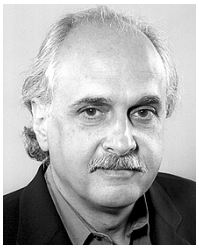

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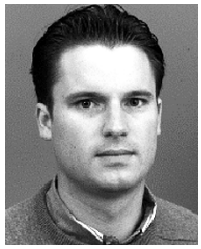

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