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Superjunction Power Transistors With Interface Charges: A Case Study for GaN

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ABSTRACT Recent progress in p-GaN trench-filling epitaxy has shown promise for the demonstration of GaN superjunction (SJ) devices. However, the presence of n-type interface charges at the regrowth interfaces has been widely observed. These interface charges pose great challenges to the design and performance evaluation of SJ devices. This work presents an analytical model for SJ devices with interface charges for the first time. In our model, two approaches are proposed to compensate interface charges, by the modulation of the SJ doping or the SJ geometry. Based on our model, an analytical study is conducted for GaN SJ transistors, revealing the design windows and optimal values of doping concentration and pillar width as a function of interface charge density. Finally, TCAD simulation is performed for vertical GaN SJ transistors, which validated our analytical model. Our results show that, with optimal designs, interface charges would only induce small degradation in the performance of GaN SJ devices. However, with the increased interface charge density, the design windows for pillar width and doping concentration become increasingly narrow and the upper limit in the pillar width window reduces quickly. When the interface charge density exceeds $\sim 3\times 10^{12}$ cm^{-2}, the design window of pillar width completely falls into the sub-micron range, indicating significant difficulties in fabrication. Vertical GaN SJ transistors with interface charges retain great advantages over conventional GaN power transistors, but have narrower design windows and require different design rules compared to ideal GaN SJ devices.

INDEX TERMS Power electronics, power semiconductor devices, superjunction, interface charges, interface impurities, gallium nitride, semiconductor device modeling, device simulation.

I. INTRODUCTION

One of the main objectives in the design of power devices is to obtain a high off-state breakdown voltage (V_B) while keeping a low on-state specific resistance ($R_{on,sp}$). Today's unipolar power devices are limited by a theoretical trade-off that $R_{on,sp}$ increases with the square of V_B [1]. A vertical superjunction (SJ) structure could break this theoretical limit. It utilizes multiple n-type and p-type pillars with relatively high doping to replace the single-conduction-type lowly-doped drift region in unipolar devices. Due to the charge balance in n- and p-pillars, the SJ region can be depleted at relatively low voltages. This allows for the increase in the pillar doping, and therefore a significantly lower $R_{on,sp}$, for the same V_B. As a result, a linear dependence of $R_{on,sp}$ on V_B can be achieved in vertical SJ devices [2]. Since their technological realization in the late 1990s, Si SJ devices have achieved huge commercial success up to 900 V [3].

SJ structures also promise great improvement to today's wide-bandgap power devices. SiC and GaN SJ devices have superior theoretical performance than Si SJ devices. However, the fabrication of SiC and GaN SJ structures remains challenging. Vertical SiC SJ diodes were first demonstrated in 2014 [4], and 1.2 kV SiC SJ MOSFETs were recently announced [5]–[6]. Up to now, no experimental demonstration of vertical SJ devices has

been reported in GaN, due to the challenges in forming multiple n-/p-pillars with precisely controlled doping and charges.

The fabrication technology for SJ devices can be classified into two categories [3]: multi-epitaxy and trench. Multi-epitaxy uses multiple steps of masked implantation and epitaxial growth to make the n- and p-pillars. The trench technology is based on the formation of deep trenches and subsequent epitaxial filling of compensating pillars. For GaN, multi-epitaxy is extremely challenging, as the p-type ion implantation in GaN is very difficult to produce sufficient dopants [7]. In addition, the activated acceptors in the implanted regions will be re-passivated by the hydrogen present in the growth chamber during the following epitaxy. In contrast, selective-area p-GaN trench-filling epitaxy has been recently demonstrated for forming lateral PN junctions by a few groups [8]–[11]. This suggests a good promise to make the GaN SJ based on the trench etch and p-GaN filling epitaxy.

Despite the feasibility of p-GaN trench-filling epitaxy, the presence of n-type interface charges has been widely reported for the p-GaN regrowth on different GaN lattice planes [11]–[14]. The physical origin of this interface charges is often attributed to the impurities (Si, O, C, mainly Si) in the growth chamber or in the environments during the device transfer to the growth chamber [12]–[14]. The donor-type nitrogen vacancies at the etched sidewalls, which have been widely reported in vertical GaN devices [15]–[17], may also contribute to the interface charge. These interface charges impair the charge balance required for the design of SJ devices. New SJ models considering the interface charges are therefore highly desired.

Although various models have been developed for SJ devices with fixed oxide charges [18]–[20], asymmetric doping [21] or charge imbalance [22], there still lacks the SJ models that consider the interfacial impurity dopants which can provide carriers and induce a parasitic leakage path. In addition, most of the previous models focused on the evaluation of charge imbalance to SJ performance (e.g., $R_{\mathrm{on,sp}}$, V_{B}). However, a more urgent need for GaN SJ design is a guideline to quantify the optimal SJ geometry and doping for a given interface charge density. This is because that the interface charges at the PN junction are difficult to completely remove but can be experimentally characterized in GaN.

This work for the first time formulates an analytical model for SJ with interface charges. Two methods were investigated to compensate the interface charge, by the modulation of doping or geometry. Numerical analysis was conducted for GaN SJ transistors, with a careful comparison between two compensation methods. TCAD simulation was then performed for vertical GaN SJ transistors, which validated our analytical models and numerical analysis. The results in this work provide important guidelines for the design and experimental demonstration of vertical GaN SJ devices.

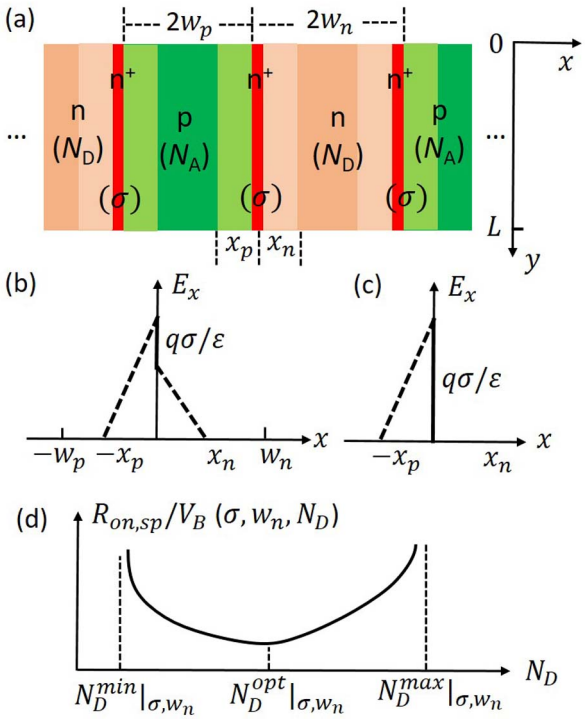

FIGURE 1. (a) Schematics of the SJ with interface charges considered in our analytical models. (b) E_x distribution in the SJ unit-cell at the zero bias. (c) E_x distribution in the situation when the depletion in n-pillars reduces to zero at zero bias. (d) Schematic illustration for seeking the optimal FOM of SJ devices, by iterating the N_D for a given σ and a selected w_n; also shown is the N_D design window for a given σ and a selected w_n.

II. ANALYTICAL MODELS

Fig. 1(a) shows the schematic model of the SJ with interface charges. The width and doping concentration are $2w_n$ and N_D for the n-pillar, and $2w_p$ and N_A for the p-pillar, respectively. In this work, we propose two baseline design methods to compensate the interface charge [with a charge density $\sigma(\mathrm{C}/cm^2)$] by either increasing the doping concentration in p-pillars or increasing the p-pillar width.

A. DOPING MODULATION

In the first approach, we increase the p-pillar doping while keeping $w_n = w_p$. The charge balance gives:

$$N_A = N_D + \sigma/w_n \tag{1}$$

In SJ devices, on-state current only flows in the n-pillars. The calculation of the conduction width requires the consideration of the parasitic junction field-effect transistor (JFET) effect. As first studied by Nassif-Khalil *et al.* [23] and Disney and Dolny [24] and recently studied by Wang *et al.* [20] and Kang and Udrea [25], [26], the JFET effect accounts for the lateral depletion of p-n junctions that narrows the current conduction width in n-pillars.

The JFET effect is more prominent at higher drain voltages (V_{DS}), due to the increased depletion width in the n-pillars (x_n) at higher V_{DS} [25], [26]. This is important for the normal

operation of SJ transistors with interfacial impurity dopants, in that the interfacial dopants are depleted in the forward conduction and forward blocking states and will not induce the parasitic leakage path along the PN junction interfaces.

The minimum $R_{on,sp}$ is achieved when the V_{DS} approaches zero; in this scenario, the x_n is given by the intrinsic built-in potential of p-n junctions [25], [26], and the $R_{on,sp}$ of the SJ region is derived as

$$R_{on,sp} = \frac{1}{qN_D\mu_n}\frac{L}{(w_n - x_n)Z}2w_nZ = \frac{2L}{qN_D\mu_n}\frac{w_n}{w_n - x_n} \quad (2)$$

where Z is the SJ depth, L is the SJ length and μ_n is the electron mobility which is dependent on N_D [23].

For wide-bandgap p-n junctions with sufficient doping concentrations, the built-in potential can be replaced by the potential of the material's bandgap [25], E_g/q. From Fig. 1(b), the following equations can be written based on the built-in potential and the E-field continuity:

$$E_g/q = qN_Dx_n^2/2\varepsilon + qN_Ax_p^2/2\varepsilon \quad (3)$$

$$qN_Ax_p/\varepsilon = q(N_Dx_n + \sigma)/\varepsilon \quad (4)$$

where ε is the material permittivity. The x_n is then solved by combining (1), (3) and (4).

$$x_n = \frac{-\sigma + \sqrt{-\frac{\sigma^3}{N_Dw_n} - \sigma^2 + \frac{2\varepsilon E_g}{q^2N_D}\left(N_D + \frac{\sigma}{w_n}\right)\left(2N_D + \frac{\sigma}{w_n}\right)}}{2N_D + \sigma/w_n} \quad (5)$$

The breakdown of SJ devices occurs when the maximum electric field (E-field) reaches the material critical E-field, E_C. The lateral E-field at the breakdown, E_x, is given by:

$$E_x = \alpha E_C = q(\sigma + N_Dw_n)/\varepsilon \quad (6)$$

Here α is defined as the ratio between E_x and E_C.

The vertical E-field, E_y, and the device breakdown voltage, V_B, are calculated as follows:

$$E_y = \sqrt{E_c^2 - E_x^2} = E_C\sqrt{1-\alpha^2} \quad (7)$$

$$V_B = E_yL = E_CL\sqrt{1 - \left[q(\sigma + N_Dw_n)/\varepsilon E_c\right]^2} \quad (8)$$

Inserting (8) into (2), the $R_{on,sp} \sim V_B$ trade-off for the SJ devices with interface charges can be obtained.

$$\frac{R_{on,sp}}{V_B} = \frac{2/qE_C}{\mu_nN_D\sqrt{1 - \left[q(\sigma + N_Dw_n)/\varepsilon E_c\right]^2}}\frac{w_n}{w_n - x_n} \quad (9)$$

where the $R_{on,sp}/V_B$ is often referred to as the figure of merit (FOM) for SJ power devices. A smaller FOM corresponds to the superior performance of SJ devices. It is worth mentioning that the SJ FOM is different from the Baliga's FOM often used for evaluating conventional unipolar power devices ($V_B^2/R_{on,sp}$), as SJ breaks the conventional $V_B \sim R_{on,sp}$ limits and allows a linear limit as explained in Section I.

It should be noted that if no interface charges ($\sigma = 0$) and JFET effect ($x_n = 0$) are considered, (9) leads to the ideal SJ relations:

$$\left(\frac{R_{on,sp}}{V_B}\right)_{Ideal} = \frac{2w_n}{\alpha\sqrt{1-\alpha^2}\mu_n\varepsilon E_C^2} = \frac{4w_n}{\mu_n\varepsilon E_C^2}\left(\alpha = \frac{1}{\sqrt{2}}\right) \quad (10)$$

For the ideal SJ region, the $R_{on,sp}/V_B$ has the lowest value at $\alpha = 1/\sqrt{2}$ [2], [3]. The ideal model does not contain a theoretical limit, as $R_{on,sp}/V_B$ can be reduced indefinitely by decreasing the w_n and selecting an N_d accordingly to satisfy $\alpha = 1/\sqrt{2}$.

The optimal SJ design corresponds to the lowest value of $R_{on,sp}/V_B$ in (9). There are no easy analytical solutions due to the incorporation of σ. For a given σ, an iteration of all feasible w_n and N_D combinations are needed to find the minimum $R_{on,sp}/V_B$. To simplify the iteration, it is important to define the upper and lower bounds of w_n and N_D, i.e., design windows [see Fig. 1(d)]. For a given σ and a selected w_n, the maximum N_D can be determined from $\alpha < 1$, which gives:

$$N_D^{max}|_{\sigma,w_n} = \varepsilon E_C/qw_n - \sigma/w_n \quad (11)$$

The minimum N_D can be derived from two constraints: (a) $x_n \geq 0$, i.e., interface charges need to be fully depleted at zero bias, otherwise, large interface leakage will be induced at small biases; (b) $x_n \leq w_n$, i.e., n-pillars should not be fully depleted at zero bias, otherwise, no forward conduction is present due to the JFET effect. Based on Fig. 1(c) and equations (1), (3) and (4), the minimum N_D from the first constraint can be obtained.

$$N_{D\_1}^{min}|_{\sigma,\mathrm{w_n}} = q^2\sigma^2/2\varepsilon E_g - \sigma/w_n \quad (12)$$

The minimum N_D based on the second constraint can be obtained based on Fig. 1(b) and equations (3)-(4).

$$N_{D\_2}^{min}|_{\sigma,\mathrm{w_n}} = \varepsilon E_g/q^2w_n^2 - \sigma/2w_n \quad (13)$$

$$N_D^{min}|_{\sigma,\mathrm{w_n}} = max\left\{N_{D\_1}^{min}|_{\sigma,\mathrm{w_n}}, N_{D\_2}^{min}|_{\sigma,\mathrm{w_n}}\right\} \quad (14)$$

From $N_{D\_1}^{min}|_{\sigma,\mathrm{w_n}} < N_D^{max}|_{\sigma,\mathrm{w_n}}$ and $N_{D\_2}^{min}|_{\sigma,\mathrm{w_n}} < N_D^{max}|_{\sigma,\mathrm{w_n}}$, the range for w_n selection can be derived based on (11)-(13).

$$\frac{\varepsilon E_g}{\varepsilon E_c q - \sigma q^2/2} < w_n < \frac{2E_g\varepsilon^2E_C}{q^3\sigma^2} \quad (15)$$

Equations (15) and (12)-(14) provide the design windows for the pillar width and doping concentration, respectively.

B. GEOMETRY MODULATION

In the second approach, we increase the p-pillar width while keeping $N_D = N_A$. The charge balance gives:

$$w_p = w_n + \sigma/N_D \quad (16)$$

The $R_{on,sp}$ of the SJ region in this scenario is derived as

$$R_{on,sp} = \frac{1}{qN_D\mu_n}\frac{L(w_n + w_p)}{(w_n - x_n)Z} = \frac{L}{qN_D\mu_n}\frac{2w_n + \sigma/N_D}{w_n - x_n} \quad (17)$$

The x_n is then solved by inserting (16) into (3) and (4).

$$x_n = -\sigma/2N_D + \sqrt{-4\sigma^2/4N_D^2 + \varepsilon E_g/q^2N_D} \quad (18)$$

The SJ FOM in this scenario can be derived by combining (17), (7) and (8).

$$\frac{R_{on,sp}}{V_B} = \frac{1/qE_C}{\mu_nN_D\sqrt{1 - \left[q(\sigma + N_Dw_n)/\varepsilon E_c\right]^2}}\frac{2w_n + \sigma/N_D}{w_n - x_n} \quad (19)$$

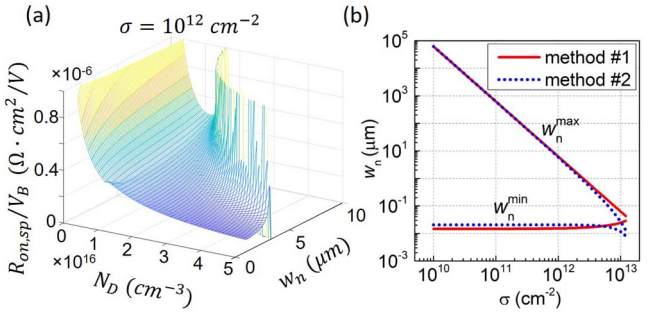

FIGURE 2. **(a) 3-D illustration of the SJ FOM as a function of w_n and N_D, for a σ of 10^{12} cm^{-2}, based on the first design method. (b) The calculated maximum w_n and minimum w_n as a function of σ for two design methods.**

Identical to the first approach, for a given σ and a selected w_n, the maximum N_D is limited by $\alpha < 1$, as given by (11). The minimum N_D is limited by the constraints $x_n \geq 0$ and $x_n \leq w_n$, which gives:

$$N_{D\_1}^{min}|_{\sigma,w_n} = q^2\sigma^2/2\varepsilon E_g \tag{20}$$

$$\left(w_n N_{D\_2}^{min}\right)^2 + \left(w_n N_{D\_2}^{min} - \varepsilon E_g/q^2\right)N_{D\_2}^{min} + \sigma^2/2 > 0 \tag{21}$$

From $N_{D\_1}^{min} < N_D^{max}$ and $N_{D\_2}^{min} < N_D^{max}$, the design window of w_n in the second approach is given by:

$$\frac{2\varepsilon E_g(\varepsilon E_C - \sigma q)}{q^3\sigma^2 - q^2\sigma\varepsilon E_c + q\varepsilon^2 E_C^2} < w_n < \frac{2\varepsilon E_g(\varepsilon E_C - \sigma q)}{q^3\sigma^2} \tag{22}$$

From the comparison of (22) and (15), it can be seen that the design window of w_n is smaller in the second approach compared to the first approach.

III. NUMERICAL ANALYSIS

Numerical analysis was conducted for a GaN SJ region with interface charges, based on the analytical models developed in Section II. The ε, E_g and E_C of GaN are 8.4×10^{-13} (F/m), 3.4 eV and 3.3 MV/cm [27], respectively. The $\mu_n(cm^2/V \cdot s)$ of GaN as a function of doping concentration is used as [27]

$$\mu_n = \left(2 \times 10^{17} + 60N_D^{0.78}\right)/\left(2 \times 10^{14} + N_D^{0.78}\right) \tag{23}$$

Fig. 2(a) shows the numerically calculated FOM of the GaN SJ as a function of w_n and N_D based on the first design approach. For each w_n, the FOM reaches a minimum value at $N_D^{opt}|_{\sigma,w_n}$. This is consistent with our analytical models shown in Fig. 1(d).

From (15) and (22), the maximum and minimum w_n in two design approaches were calculated as a function of σ, as shown in Fig. 2(b). The physical upper limit of σ that allows for the GaN SJ design is calculated to be $\sim 10^{13}$ cm^{-2}, based on (6) when $q\sigma/\varepsilon E_C \to 1$. The design window of w_n is reduced quickly with the increased σ. The SJ design based on the second approach has slightly smaller w_n design window compared to the first approach. In addition, the upper limit of the $w_n$design window reduces quickly with the increased σ. As shown, when the σ is above $\sim 3\times10^{12}$ cm^{-2}, the design window of SJ pillar width ($2w_n$) completely falls into the sub-micron range, indicating great difficulties in device fabrication.

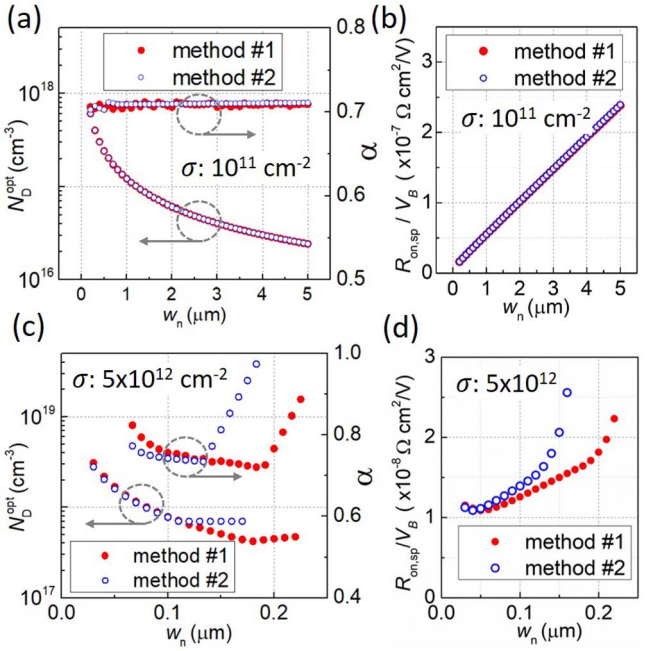

FIGURE 3. **(a) Optimal combinations of w_n and N_D and the corresponding α, as well as (b) the SJ FOM, for a σ of 10^{11} cm^{-2}, for two design methods. (c) Optimal w_n and N_D and the α, as well as (d) the SJ FOM, for a σ of 5×10^{12} cm^{-2}, for two design methods.**

Next, we study the SJ design for two characteristic σ. The σ selection is based on the experimentally reported Si impurity concentration at the regrown PN interface [12]–[14]. The Si peak concentration (N_{peak}) at the regrown p-GaN interface was reported to range from $\sim 10^{17}$ cm^{-3} to $\sim 3\times10^{19}$ cm^{-3} in [12]–[14], and the full width at half maximum (FWHM) concentration is about 20$\sim$30 nm. This corresponds to an interface charge ($\sigma \sim FWHM \times N_{peak}/2$) in the range of 10^{11} cm^{-2} and 5×10^{12} cm^{-2}. This range is also consistent with the interface charge density experimentally characterized at the GaN/dielectric interface [15]–[17], which further supported its practical significance.

The two characteristic σ values of 10^{11} cm^{-2} and 5×10^{12} cm^{-2} have not only practical significance but also physical significance. The former σ is much smaller than $N_D w_n$, indicating the minor disturbance on the charge balance in ideal SJ. The latter σ of comparable to $N_D w_n$ and is close to the physical upper limit of σ, indicating the need for a complete reconstruction of the charge balance in SJ.

The solved N_D^{opt} as a function of w_n for $\sigma = 10^{11}\ cm^{-2}$ is shown in Fig. 3(a). The calculated α almost equals to $1/\sqrt{2}$ in all optimal combinations of w_n and N_D, for two design approaches. This indicates that for a relatively small σ, the design guideline for the SJ with interface charges is similar to the ideal SJ, i.e., $\alpha = 1/\sqrt{2}$. The only difference is the need to account for σ in α, as given by (6). As shown in Fig. 3(b), the FOM is improved at lower w_n. This trend is

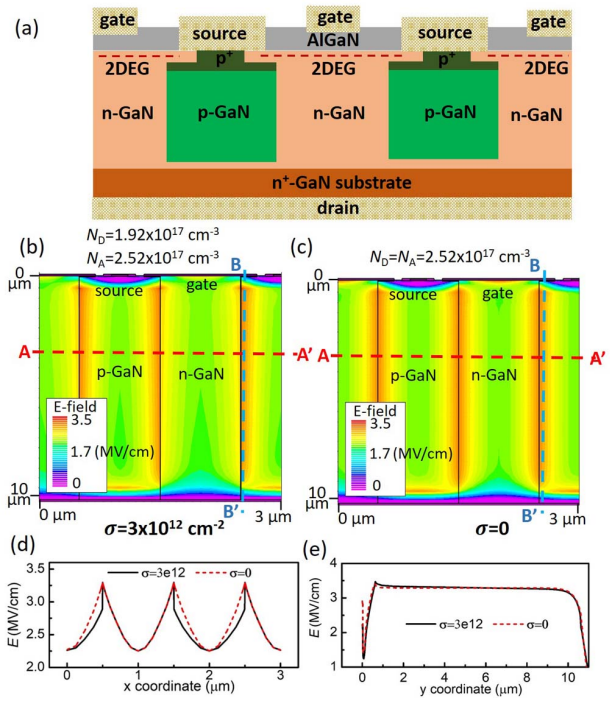

FIGURE 4. (a) Schematics of the simulated GaN SJ-CAVETs. Simulated E-field distribution in GaN SJ-CAVETs optimized for a pillar width of 1 μm, with (b) a σ of 3×10^{12} cm^{-2} and (c) without σ, both at an off-state bias of V_{DS} = 2400 V and V_G = −5 V. Simulated E-field distribution along the cutline (d) A-A′ and (e) B-B′, extracted in (b) and (c).

also similar to the ideal SJ. The two approaches give almost identical FOMs.

When the σ is large, i.e., the σ is comparable to $N_D w_n$, the α for the optimal designs was found to deviate from $1/\sqrt{2}$. Fig. 3(c) shows the derived optimal combinations of w_n and N_D for $\sigma = 5 \times 10^{12}\ cm^{-2}$, for two design approaches. As shown, the α is clearly higher than $1/\sqrt{2}$. This higher α indicates an inferior SJ FOM, as it means a smaller percentage of E_C is attributed to E_y to support the device V_B.

Fig. 3(d) shows the SJ FOMs based on two design approaches. The FOMs based on the first approach is superior to the second approach. This conforms to the higher α for the second approach. Its inferior FOM can be attributed to the enlarged p-pillar width, which reduces the effective percentage of device area for current conduction and therefore increases the $R_{on,sp}$. From Fig. 3(d), it can be seen that the FOM does not decrease indefinitely with the reduced w_n. This is due to the JFET effect, and agrees with the findings in [20], [25].

IV. TCAD SIMULATION

To further validate our analytical model, TCAD simulation was performed for GaN SJ transistors. As the main purpose of our simulation is to validate the physical models on the distribution of E-field and current in the SJ drift region, the selection of gate-modulated channel structures is not critical. Here we simulated a vertical GaN SJ transistor with the lateral two-dimensional-electron-gas (2DEG) channel, i.e., an SJ current aperture vertical electron transistor (SJ-CAVET). The schematic of SJ-CAVET is shown in Fig. 4(a). The source electrode forms Ohmic contact to an n^+-GaN source region and a p^+-GaN current blocking layer. The former is used to provide electrons to 2-DEG channels and the latter to confine the vertical electron conduction in the apertures below the gate electrode. This structure was first studied in [28] and we recently developed TCAD simulation for this structure [29]. However, none of prior studies considered the interface charges in the SJ drift region.

The 2-D TCAD simulations were performed using the Silvaco ATLAS simulator. The device physical models were established based on our previous simulation developed for lateral and vertical GaN power transistors [29]–[33]. The electron/hole continuity equations and Poisson equations were solved self-consistently, taking into account the Shockley-Read-Hall recombination, carrier generation, electron saturation velocity, complete dopant ionization, and impact ionization. The dependence of the electron mobility in bulk GaN on the electric field was adopted as described in [29], [30] and its dependence on doping concentration was adopted as described in (23). The bulk electron mobility in n-GaN at low donor concentration ($\sim10^{15}$ cm^{-3}) was calibrated to be $\sim$1000 cm^2/ V·s, making it consistent with the one extracted from our recent experimental study on vertical GaN transistors [34]. The sheet charge density and mobility of the AlGaN/GaN channel are set as 10^{13} cm^{-2} and 1500 cm^2/V·s, respectively, based on our experimental data on lateral GaN transistors described in [30]. The calibration of the simulation model for the AlGaN/GaN channel with the experimental data has also been illustrated in [30].

Two SJ-CAVETs were designed and simulated, one with a relatively large σ of 3×10^{12} cm^{-2} (i.e., the midpoint of the range $10^{11} \sim 5 \times 10^{12}$ cm^{-2} extracted from the experimental reports, as illustrated in Section III) and the other without interface charges in the SJ drift layer. The design of the SJ drift region with interface charges was based on the first approach in Section II, as the first approach has been revealed as superior to the second approach for compensating the interface charges in Section III. A pillar width was selected as 1 μm, considering the fabrication limit to etch the deep trenches. The optimal doping concentrations in n- and p-pillars were then determined using our analytical models. The thickness of the SJ drift region is 10 μm. While this thickness is not relevant to the focus of our study, recent experimental demonstration of etching high-aspect-ratio GaN deep trenches [15], [35], [36] with submicron width [15], [36] suggests the feasibility to etch the 1-μm-wide and 10-μm-deep trenches. Whereas, we note that p-GaN regrowth in 10 μm trenches is still very challenging, as most of the p-GaN regrowth experimentally demonstrated up to now is limited to 1 μm [8]–[10]. In our simulation, besides adding σ in the SJ drift region, the same amount of σ was added to the lateral p^+/n and p^+/p interfaces in the current aperture regions.

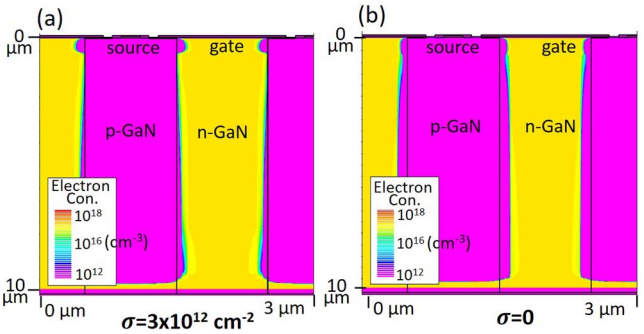

FIGURE 5. **Simulated electron concentration distribution in GaN SJ-CAVETs with (a) a σ of 3×10^{12} cm^{-2} and (b) without σ, both at an on-state bias of V_{DS} = 10 V and V_G = 5 V.**

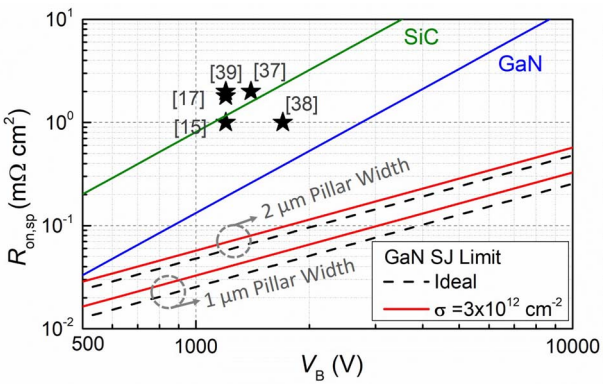

FIGURE 6. **$R_{on,sp} \sim V_B$ trade-offs for the GaN SJ with and without interface charges ($\sigma=3\times10^{12}$ cm^{-2}), for the pillar width of 1 μm and 2 μm, respectively. Theoretical limits for SiC and GaN conventional devices (as the conventional GaN drift region requires low N_D, a constant mobility of 1000 cm^2/Vs is used), and the experimental data for state-of-the-art GaN vertical transistors with conventional drift regions, are also included. An E_C of 2.4 MV/cm is used for SiC when calculating the unipolar SiC limit.**

Fig. 4(b) and (c) show the simulated E-field distribution of GaN SJ-CAVETs with and without interface charges, at a forward-blocking bias. Fig. 4(d) shows the simulated E-field distribution along a lateral cutline. Note the E_y is identical along this lateral cutline; the simulated E-field distribution validates the E_x distribution adopted in our analytical models [see Fig. 1(b)]. Fig. 4(e) shows the E-field distribution along a vertical cutline along the PN-pillar interface in the SJ drift region. The simulated E-field shows a uniform distribution at the SJ interface in the drift region, which validates the SJ design (in contrast to the triangle-shaped E-field distribution in conventional drift regions). This also suggests that interface charges induce no degradation in the E-field of SJ transistors. At a drain bias of 2400 V, an 'average' peak E-field of ~3.3 MV/cm locates at the SJ interface, which is close to the critical E-field of GaN (3.3-3.7 MV/cm).

Fig. 5(a) and (b) show the simulated electron concentration in GaN SJ-CAVETs with and without interface charges, at a forward-conduction bias. The simulated electron concentration distribution well validated the JFET effect considered in our analytical models. From the comparison between Fig. 5(a) and (b), it can be seen that interface charge reduces the depletion width in n-pillars, as it screens the E_x to the n-pillar. As a result, the current conduction path is wider in the SJ-CAVETs with interface charges. However, as revealed in Section III, the $R_{on,sp}$ of SJ-CAVETs with interface charges is still larger than the devices without. This is due to the smaller value of the optimal N_D in the SJ-CAVETs with interface charges.

V. BENCHMARK AND DISCUSSION

Fig. 6 plots the $R_{on,sp} \sim V_B$ trade-offs for the optimized GaN vertical SJ drift region with and without interface charges, for a pillar width of 1 μm and 2 μm, respectively. The theoretical limit for unipolar GaN and SiC devices and the experimental data for state-of-the-art vertical GaN transistors with conventional drift regions [15], [17], [37]–[39] are also included for benchmarking. In vertical GaN power transistors, at least 10-to-100-fold smaller $R_{on,sp}$ can be achieved for the same V_B by adopting the SJ structure in the drift region. These advantages are retained for the SJ with interface charges, as long as optimal designs are adopted based on the design guidelines and analytical model developed in this work.

Finally, we would like to discuss the applicability and limitations of our analytical models presented in this work. Our analytical models work the best for the interface charges originated from the interfacial impurity doping, such as the [Si] or [O] interfacial dopants recently observed in the regrown p-GaN [12]–[14]. If the origin of interface charges is the interface trap with a wide energy distribution within the bandgap, the amount of interface charge would possibly not be fixed but depend on the device working biases. In this case, more complete analytical models are not only needed to study the static parameters (e.g., V_B and $R_{on,sp}$) of SJ transistors but also for their switching performances in consideration of the dynamic responses of interface traps. While these non-ideal factors need to be considered in the future models after the availability of experimental GaN SJ devices, we would like to re-assure the significance of this work that it provides the design guidelines for the experimental demonstration of GaN SJ devices with interface charges and removes the concern that the benefits of SJ devices will no longer be retained in the presence of interface charges.

VI. CONCLUSION

In summary, this work demonstrates an analytical model for SJ devices with interface charges for the first time. This analytical model provides important design guidelines to minimize the adverse impacts induced by interface charges on SJ performance. Two different design guidelines were quantitatively investigated for GaN SJ devices. The doping modulation was identified to be a superior approach to compensate interface charges. The TCAD simulation of vertical GaN SJ transistors validated our analytical model. With the optimal designs, vertical GaN SJ transistors with interface charges retain great advantages over the conventional GaN

power transistors, while their design windows are smaller compared to ideal GaN SJ devices. The results in this work provide important guidelines for the design and experimental demonstration of GaN vertical SJ devices.

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