Analog Integrated Circuits and Signal Processing
https://doi.org/10.1007/s10470-020-01633-w

Push–pull based operational transconductor amplifier topologies for ultra low voltage supplies

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Received: 8 August 2019 / Revised: 18 January 2020 / Accepted: 7 March 2020

Abstract
This work presents an Operation Transconductance Amplifier with improved common mode rejection based in both Nauta's and Vieru's push–pull based OTAs operating at a 0.5 V power supply in the 180 nm CMOS process, with an additional biasing circuit that employs an adaptive body bias technique for calibration of output common mode voltage. Equal size CMOS push–pull pair inverter cells comprised by rectangular and trapezoidal transistor arrays are simulated and compared, showing that trapezoidal arrays designs have a higher DC voltage gain while rectangular arrays are more tolerant to process variability. Two new adaptive body bias circuits for CMOS circuits are proposed, which are used to minimize the inverter cells PVT variability and at the same time control the push–pull based OTAs common mode output voltage and transconductance. A schematic-level simulation of a hybrid Nauta–Vieru OTA prototype was run and achieved as result a differential voltage gain of 58 dB, a CMRR of 108 dB, a total power consumption of 375 nW, unity gain-bandwidth product of 100 kHz for a capacitive load of 10 pF, and a total area of 13,650 μm^2. The same OTA was fabricated and its DC transfer functions were measured, showing a maximum 52 dB voltage gain, 73 dB CMRR and 11μV/A transconductance at a 0.5 V voltage supply.

Keywords Analog integrated circuits · Body bias · Ultra low voltage · Operational transconductance amplifiers · Self-cascode

1 Introduction

The evolution of CMOS technology pursues smaller transistor lengths, which results in higher operating frequencies and higher logic gate densities in integrated circuits. The trade-off of higher transistor densities is an increased power density, so supply and threshold voltages were scaled down to keep power dissipation to practical levels.

New biomedical and sensor applications are being developed using energy harvesting from the environment that provides very limited energy resources and very low supply voltages, much lower than the typical supply voltages for which common digital CMOS processes are designed. Those supply voltages, commonly under 0.5 V, are within the so called ultra low voltage supplies.

Ultra low voltage supplies introduce many challenges to analog design of amplifiers and demand different circuit design strategies. Transistors must be kept operating in saturation for acceptable gains and signal swing, which excludes gain design techniques using cascode configurations and limits the use of differential pairs. Differential pairs are often replaced by pseudo-differential pairs, which lacks a current source transistor and relies on other techniques for common mode input signal and power supply rejection [3].

The gain of amplifiers stages with ultra low voltage supplies are usually lower than needed by its applications and the use of more than two amplifying stages has added complexity for stability compensation. A solution to increase gain is to use series-parallel transistor arrays to achieve higher output resistance [5].

Nauta proposed a OTA [7] based on a push–pull pseudo-differential pair and a circuit which rejects common mode input signals. Vieru proposed another push–pull based OTA [9] which employs a common mode cancellation path

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Published online: 23 March 2020

for common mode rejection. For both push–pull based amplifiers, the common mode output voltage is the quiescent voltage of the push–pull CMOS pair, which is a function of process parameters. Thus, the common mode output voltage is highly dependent of process variability. Also, the power consumption and gain bandwidth product of those topologies are defined by the push–pull pair quiescent current, which is also highly dependent of process variability.

The original Nauta's OTA biasing uses supply voltage regulation, which is impractical for ULV, so independent body-biasing was proposed in [12] to control the OTA transconductance. Also, both original and body-biased OTAs rely on positive feedback to improve its voltage gain. Another work [1] proposed rectangular arrays to improve voltage gain and process variability tolerance without body-biasing, which is useful to reduce transistor mismatch but is not effective against process parameter variability. This work proposes the use of trapezoidal transistor arrays, also know as composite series transistor and self-cascode, as an alternative to voltage gain enhancement. Additionally, this work proposes two entirely analog adaptive biasing circuits useful for both Nauta's and Vieru's OTAs, based in the push–pull body-biasing circuits from [3] and the constant transconductance current reference from [11].

In Sect. 2, the push–pull pair will be analysed for transistors operating in weak inversion and forward-body-bias will be discussed as a method to define its quiescent voltage and quiescent current. Rectangular and trapezoidal arrays will be discussed as methods to improve voltage gain and how they affect the push–pull pair characteristics. Then, two biasing circuits will be proposed: the first one to define only the push–pull quiescent voltage, and the second one to define both quiescent voltage and current.

In Sect. 3, Nauta's and Vieru's push–pull based OTAs will be analysed. A variation of the Nauta's OTA which employs the bulk terminal for common mode rejection, the Bulk Nauta OTA, will be proposed. Later, a hybrid of the proposed Bulk Nauta and Vieru OTA will be proposed. Finally, in Sect. 4, simulation and measurement results will be shown to compare the proposed amplifiers with state-of-art counterparts.

2 Push–Pull analysis, voltage gain enhancement and biasing

2.1 Push–Pull pair analysis

The CMOS push–pull pair, depicted in Fig. 1(a), consists in a PMOS transistor staked on a NMOS transistor, with the input signal connected to both gate terminals. The push–pull quiescent output voltage V_Q, which is the input voltage that results in an equal output voltage, is shown in the transfer function depicted in Fig. 1(b). The quiescent current I_Q is the push–pull DC current while $V_i = V_Q$. The quiescent current I_Q can be calculated accordingly to the UICM model [8] simplified for weak inversion operation, as shown in (1),

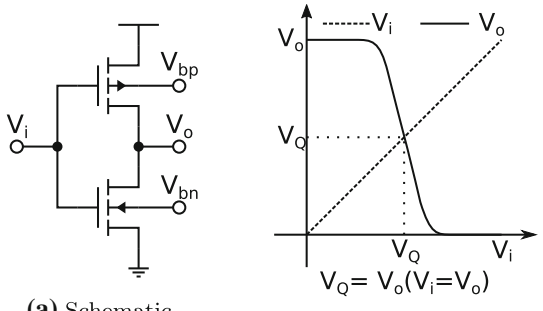
$$I_D = I_S e^1 \exp\left(\frac{V_{GS} + (n-1)V_{BS} - V_T}{n\phi_t}\right) \tag{1a}$$

$$I_Q = I_{S_N} e^1 \exp\left(\frac{V_Q + (n-1)V_{bn} - V_T}{n\phi_t}\right) \tag{1b}$$

$$I_{S_{N(P)}} = \mu C'_{ox} n \frac{\phi_t^2}{2}\frac{W}{L} = I_{SH}\frac{W}{L} \tag{1c}$$

where I_S is the normalization current, which is function of the charge mobility μ, the oxide capacitance per area C'_{ox}, the slope factor n, the thermal voltage ϕ_t and the channel width and length W and L. Considering that V_Q is kept constant, by biasing independently the PMOS and NMOS substrate voltages V_{bp} and V_{bn}, the quiescent current increases exponentially with $(n-1)V_{bn}$.

The push–pull DC transfer function itself can be simplified into a linear voltage amplifier by extrapolating small signal parameters to large signal operation. The transfer function (2) is defined by the small signal voltage gain A_V and this approximation is only valid while both PMOS and NMOS transistors operate in saturation and in weak inversion. The voltage gain A_V is function of the inverter transconductance G_m and output conductance G_o, which are respectively function of the PMOS and NMOS transistors gate-drain small signal transconductance g_{mg} and drain conductance g_{md}, accordingly to the UICM model. Finally, these small signal parameters are function of the slope factor n, the thermal voltage ϕ_t and the Early voltage V_A.



(a) Schematic **(b)** Transfer Function

Fig. 1 CMOS push–pull pair

$$V_o = A_V(V_Q - V_{in}) + V_Q \tag{2a}$$

$$G_m = g_{mg_P} + g_{mg_N} = \frac{I_Q}{\phi_t}\left(\frac{1}{n_P} + \frac{1}{n_N}\right) \approx \frac{2I_Q}{n\phi_t} \tag{2b}$$

$$G_o = g_{md_P} + g_{md_N} = I_Q\left(\frac{1}{V_{A_P}} + \frac{1}{V_{A_N}}\right) \tag{2c}$$

$$A_V = G_m R_o = \frac{G_m}{G_o} \approx \frac{1}{n\phi_t\left(\frac{1}{V_{A_P}} + \frac{1}{V_{A_N}}\right)} \tag{2d}$$

The quiescent output voltage V_Q can be controlled by body biasing, since V_Q varies almost proportionally with the bulk terminal voltages V_{bp} and V_{bn}, as shown by (3). Fig. 2(a) and (b) shows the circuits used to extract V_Q and the initial quiescent voltage V_{Q0}. Considering operation in weak inversion, the initial quiescent voltage V_{Q0} is defined by (3b), obtained for $V_{in} = V_{out} = V_{bp} = V_{bn}$, as derived in [6]. Also, as inferred from (3b), V_{Q0} is sensitive to process and temperature variations.

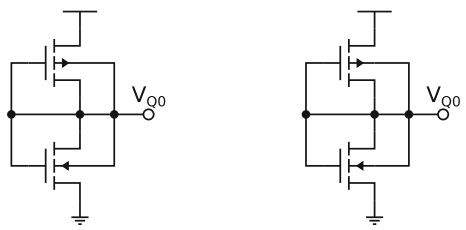
$$\begin{aligned} V_Q &\approx V_{Q0} + \frac{G_{mb}}{G_m + G_o}\left(V_{Q0} - \frac{V_{bp} + V_{bn}}{2}\right) \\ &\approx V_{Q0} + (n-1)\left(V_{Q0} - \frac{V_{bp} + V_{bn}}{2}\right) \end{aligned} \tag{3a}$$

$$V_{Q0} \approx \frac{V_{DD}}{2} + \frac{V_{T_P} + V_{T_N}}{2n} - \frac{\phi_t}{2}\ln\left(\frac{I_{S_P}}{I_{S_N}}\right) \tag{3b}$$

2.2 Voltage gain enhancement

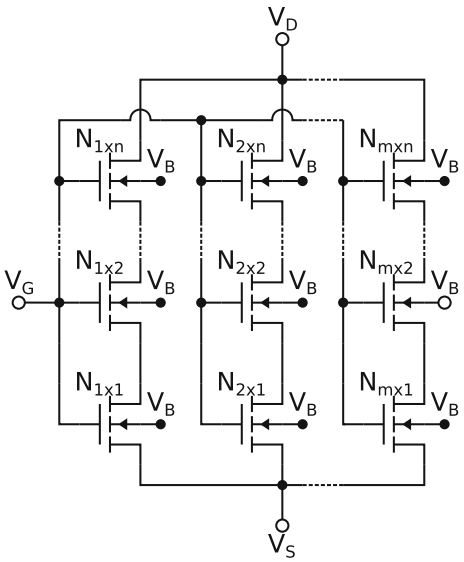
Since the traditional cascode amplifier configuration must be avoided in order to improve output voltage signal swing, another technique must be used to improve gain. Rectangular transistor arrays [5] are equivalent to a single transistor with a large output impedance, which improves gain.

The rectangular array, shown in Fig. 3(a), is a m by n matrix of single transistors composed by m parallel columns of n series single transistors. The rectangular equivalent transistor aspect ratio S_{eq-R} is a function of the single transistor aspect ratio S_u, as shown in (4). The rectangular array total gate area $A_R = (mn)A_u$, where A_u is the single transistor area.

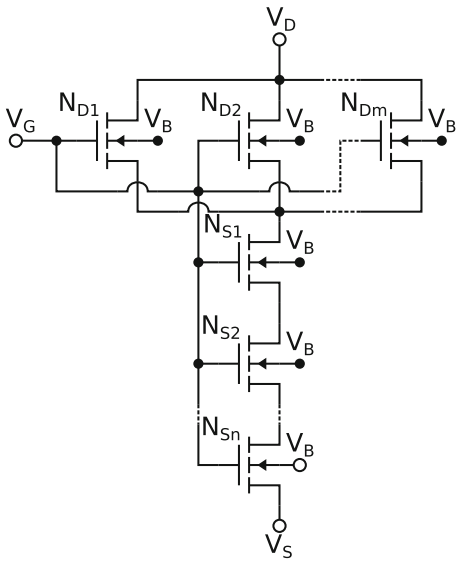


(a) Quiescent Voltage **(b)** Initial Quiescent Voltage

Fig. 2 Quiescent voltage extraction circuits



(a) Rectangular $1 \times m : n$



(b) Trapeizodal $1 \times m : n$

Fig. 3 Transistor arrays

$$S_{eq-R} = \frac{W_{eq}}{L_{eq}} = \frac{mW_u}{nL_u} = \frac{m}{n}S_u \tag{4}$$

The trapezoidal array, shown in Fig. 3(b), is composed by two separate arrays N_D, composed of m parallel single transistors, and N_S, composed of n series single transistors. The trapezoidal equivalent transistor aspect ratio S_{eq-T} is a function of the single transistor aspect ratio S_u, as shown in (5). The trapezoidal array total gate area $A_T = (m+n)A_u$.

$$S_{eq-T} = \frac{W_{eq}}{L_{eq}} = \frac{mW_u}{(1+mn)L_u} = \frac{m}{1+mn}S_u \tag{5}$$

Previous works [2, 4] used rectangular transistor arrays. The trapezoidal array configuration will be used in this work instead, since it is more area efficient.

2.3 Push–pull biasing

Both push–pull quiescent voltage and current are sensitive to process, supply voltage and temperature variations, as previously mentioned. Adaptive body biasing circuits [3, 9, 12, 13] can be used to correct those unwanted variations by using the transistor body-bias effect. However, forward-body-biasing is limited to small voltages, usually lower than 0.5 V, in order to prevent latch-up and excess power consumption.

The circuit shown in Fig. 4(a) is a simplified and inherently stable version of the circuit proposed in [3]. The circuit shown in Fig. 4(b) is a improved version of the previous circuit which use of trapezoidal arrays for gain enhancement ($N_{1A,B}$ and $P_{1A,B}$ are arrays of parallel transistors, as illustrated in Fig. 3(b)) and the protection transistors P_2 and N_2 in diode configuration. Those protection transistors limit the bulk current as they work as a very large resistance between the push–pull output and transistor bulk terminals.

The circuit show in Fig. 5 is a transistor based voltage divider which outputs a reference voltage V_{REF} equal to

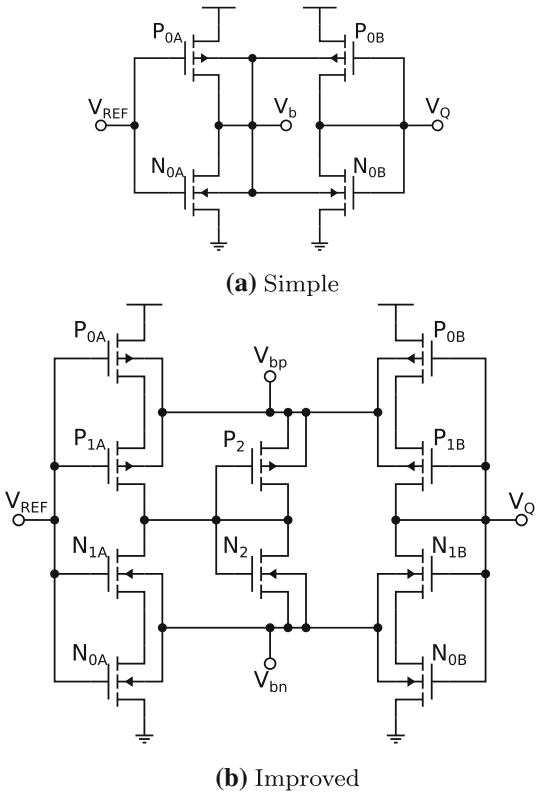


Fig. 4 V_Q only biasing circuit

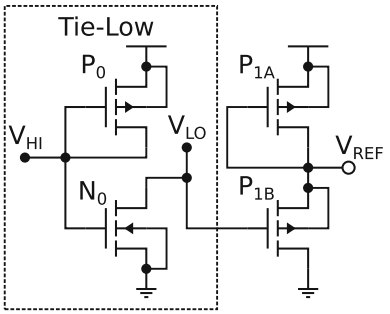


Fig. 5 Voltage reference

half supply voltage V_{DD}, since P_{1A} and P_{1B} are identical. A tie-low circuit is used to avoid connecting the PMOS gate terminal to ground, which would cause antenna layout rule violations.

The previous biasing circuit can only correct push–pull quiescent voltage V_Q process variations. In order to also correct the push pull quiescent current I_Q process variations, the biasing circuit depicted in Fig. 6 is proposed. This circuit is a variation of the former biasing circuit using the same principle of the constant transconductance self biased current reference from [11]. This circuit outputs a constant quiescent current by forcing $V_x = V_y$.

Considering a desired I_Q, V_{Q0} must be equal to V_{REF} at the initial supply voltage V_{DD0}, the resistance R_{REF} must be equal to V_{x0}/I_{Q0}, as extracted from the circuit shown in Fig. 7. This circuit is a variation of the initial quiescent voltage extractor shown in Fig. 2(b), which is also used in [6].

3 Push–pull based OTA topologies

Push–pull based amplifier topologies are well suited to low supply voltages since the push–pull pair has only two stacked transistors. In comparison with the common source

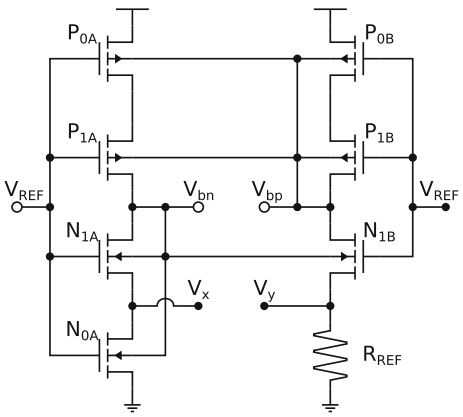


Fig. 6 Push–pull V_Q and I_Q biasing

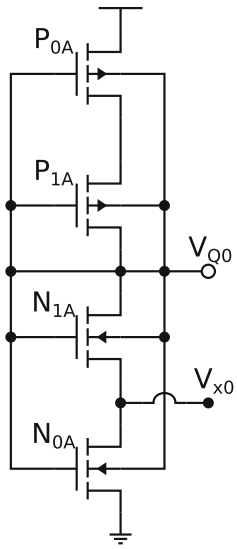


Fig. 7 Push–pull forward-body-biasing

amplifier with active load with similar dimensions and biasing, the push–pull pair has a higher transconductance G_m and voltage gain A_V. However, since both NMOS and PMOS gate terminals are used as input signal terminals, common mode rejection must be performed by additional circuits.

Nauta [7] proposed a push–pull based pseudo differential transconductor, shown in Fig. 8(a), which employs an attenuated positive feedback loop to improve common mode rejection. Another push–pull based pseudo differential transconductor was proposed by Vieru [9], shown in Fig. 8(b), which employs a common mode feedforward cancellation path for common mode rejection instead.

The transistor body effect can be used to both define the differential OTA common mode output voltage and transconductance [12], but also could be used for common mode rejection, as shown in Fig. 9. This OTA is a variation of the Nauta OTA which replaces the discrete inverters in the positive feedback loop and attenuators with a self bulk biasing circuit. This circuit is very power efficient, since it does not use the extra inverter cells. However, since the push–pull bulk transconductance G_{mb} is a fraction of its gate transconductance G_m, common mode rejection is very limited. Also, adaptive body biasing cannot be used to define V_Q or I_Q.

Figure 10 is an improved version of this OTA using the same techniques from the biasing circuit shown in Fig. 4(b). This OTA uses trapezoidal arrays to enhance DC voltage gain and the transistors P_{2A-B} and N_{2A-B} as pseudo-resistors to allow this circuit to operate with higher supply voltages.

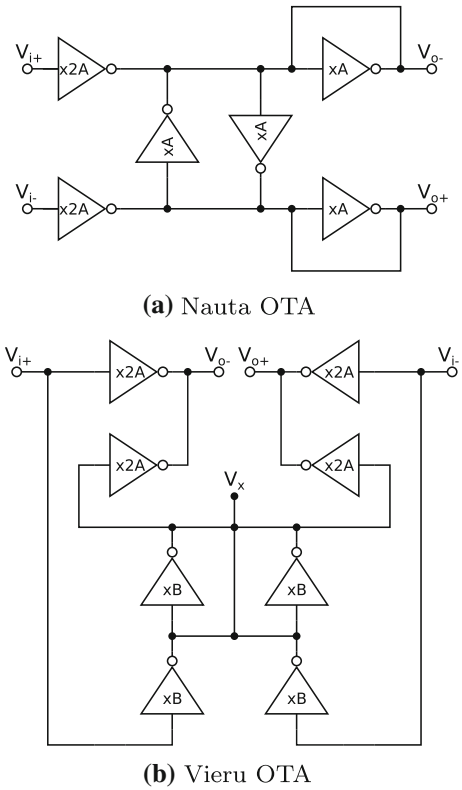


Fig. 8 Push pull based OTAs

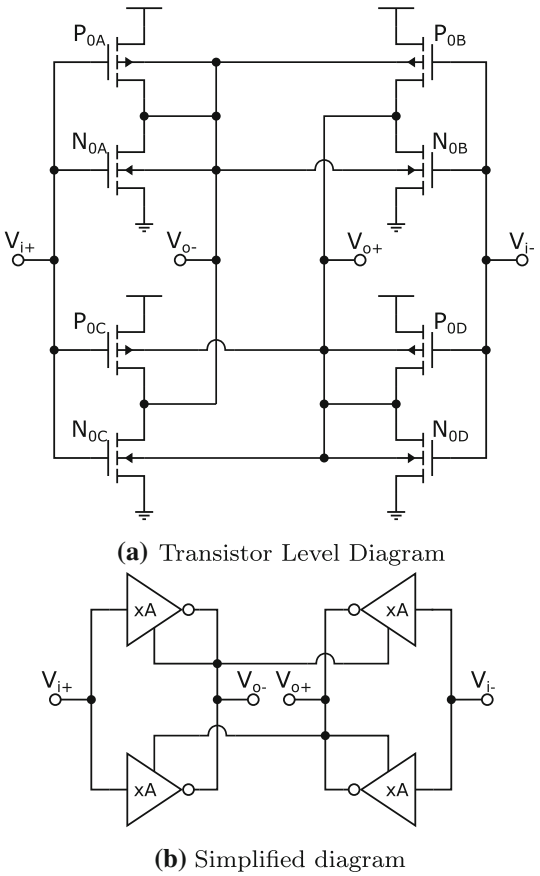


Fig. 9 Proposed bulk Nauta OTA

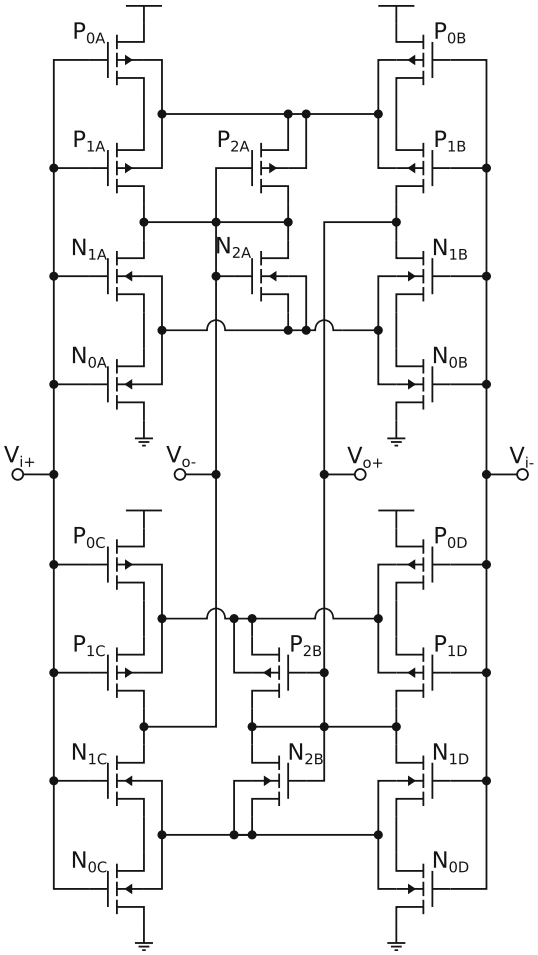


Fig. 10 Proposed improved bulk Nauta OTA

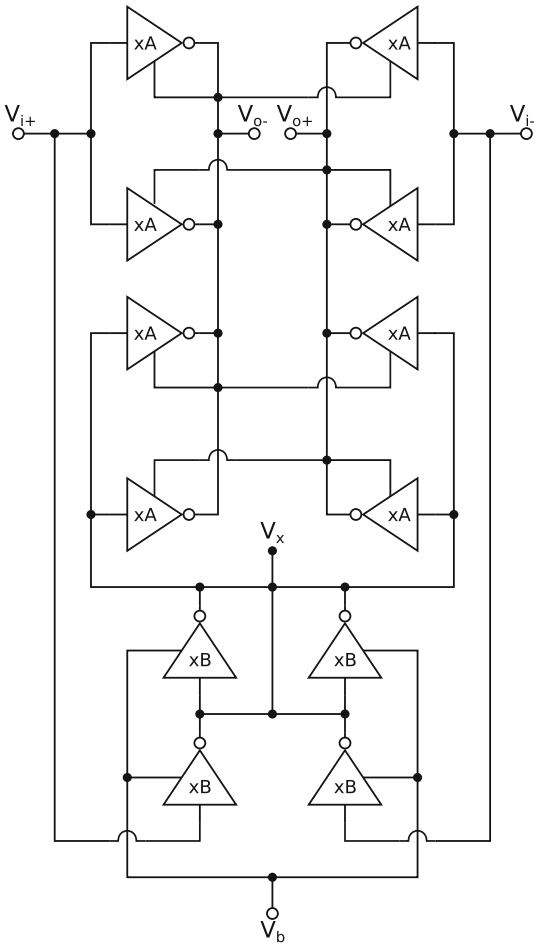


Fig. 11 Proposed hybrid Vieru-Bulk Nauta OTA

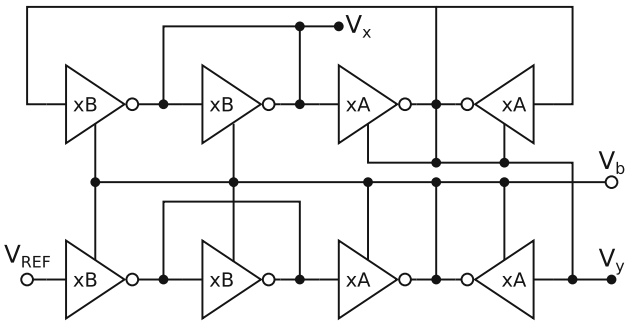


Fig. 12 Hybrid Vieru-Bulk Nauta OTA biasing circuit

In order to further improve common mode rejection and use adaptive body biasing, a hybrid Vieru-Nauta OTA is proposed. This circuit, shown in Fig. 11, replaces the inverters connected to the Vieru OTA output terminals with the previously proposed Bulk Nauta OTA variation. The common mode output voltage is defined by biasing the feedforward cancellation path inverters. The biasing circuit, shown in Fig. 12, is more complex than just biasing all inverters with the same voltages with the previous biasing circuit shown in Fig. 4. This biasing circuit corrects the OTA common mode output voltage by biasing the feedforward inverters, since the output inverter cells of the Vieru OTA topology are replaced by the Bulk Nauta OTA and its bulk terminals are already used to improve common mode signals.

Considering that the previous OTAs use as building block the same push–pull pair, their small signal parameters can be approximately described by the push–pull small signal parameters (G_m, G_o, G_{mb}, I_Q, A_V), as shown in Fig. 13. Table 1 shows their performance comparison based in the inverter factors A and B, which are the number of identical parallel push–pull pairs in each inverter. Considering that they are identically biased and A is the same for every OTA, they are expected to show the same transconductance. Nauta and Vieru OTAs have almost identical characteristics. However, the Vieru OTA has a larger total current consumption. The proposed Nauta OTA variation has a larger differential voltage gain and less total current consumption, however, it has a common mode voltage gain greater than one. The proposed Hybrid Vieru–

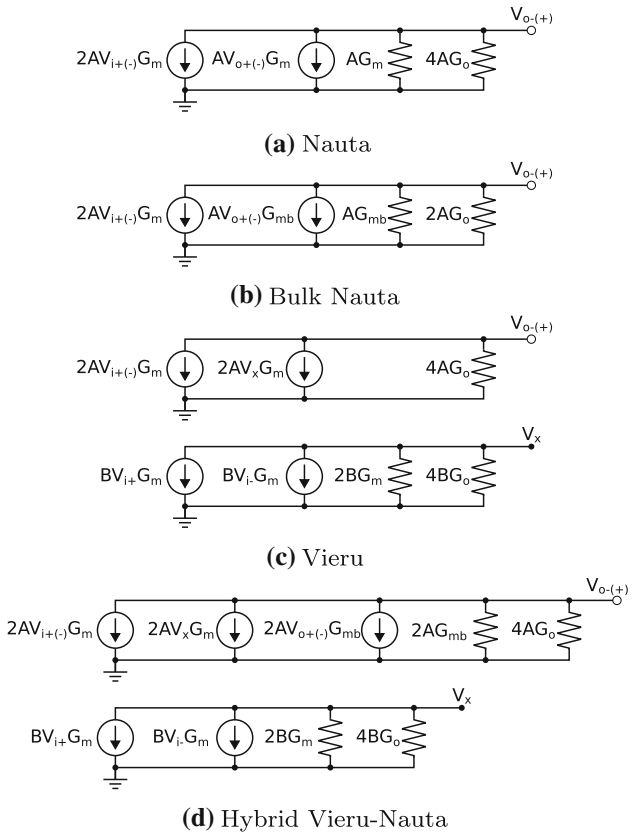


Fig. 13 Small signal diagrams

Nauta OTA uses as much total current as the Vieru OTA and has a very low common mode voltage gain.

4 Simulation and measurement results

4.1 CMOS inverter transistor array configurations

In order to compare the rectangular and trapezoidal transistor array configurations, several inverter cells were designed for a 180 nm CMOS process and simulated at 27°C with a 500 mV power supply. All inverter cells were designed using the same base single transistors, with a PMOS transistor with a 3µm width and 0.5µm length with a NMOS transistor with a 1µm width and 0.5µm length. Additionally, all transistor arrays have the same gate area.

Table 2 shows the result of mismatch only 1000 Monte Carlo simulations of inverter cells composed by rectangular (R m : n) and trapezoidal arrays (T m : n). The first conclusion is that the inverter quiescent current I_Q is proportional to equivalent aspect ratio S_{eq}. The second conclusion is that the rectangular arrays have a greater gate area than the single transistor and the quiescent current I_Q and voltage V_Q variance per average ratio μ/σ decreases accordingly. The trapezoidal array T 8:1 has a greater gate area than the single transistor, yet, they exhibit approximately the same mismatch. The transistor array T 4:5 mismatch is between the single transistor and the rectangular arrays. Although they use the same area, the trapezoidal inverters shows a much higher voltage gain than the rectangular ones.

Figure 14 (a) and (b) shows the rectangular (R) and trapezoidal (T) inverter cells DC transfer functions. It can be noticed that transistor arrays do not reduce output voltage swing.

4.2 Push–pull biasing

Three biasing circuits were designed: the V_{Q0} and I_{Q0} extractor shown in Fig. 7, the V_Q Biasing Only circuit shown in Fig. 4 and the V_Q and I_Q biasing circuit shown in Fig. 6. Transistor dimensions are shown in Table 3.

Figure 15 shows the output of simulated voltages and currents from the biasing circuit depicted in Fig. 4. As shown in Fig. 15(a), the PMOS and NMOS transistors bulk-source diodes are forward biased, as the body terminal voltages V_{bp} and V_{bn} show, while the quiescent voltage V_Q follows the reference voltage V_{REF}, which is half of the supply voltage V_{DD}. Yet, the current through the bulk terminal I_B of the transistor N_0 is orders of magnitude less than the quiescent current of I_Q, as shown in Fig. 15(b), even for the process technology nominal supply voltage of 1.8 V.

Figure 16 shows the biasing voltages and output current of the V_Q and I_Q biasing circuit. As can be seen in Fig. 16(a), the bulk biasing voltages V_{bp} and V_{bn} cross each other at a supply voltage about 600 mV, as they were designed. The output quiescent current is stable at supply voltages from 500 mV too 750 mV at typical process parameters and room temperature.

Figure 17 shows the biasing circuits temperature dependence. As expected, the non-biasing and V_Q biasing only circuits outputs almost exponential quiescent currents with temperature at a 600 mV supply voltage. The V_Q and I_Q biasing circuit outputs a PTAT quiescent current with an almost constant temperature coefficient.

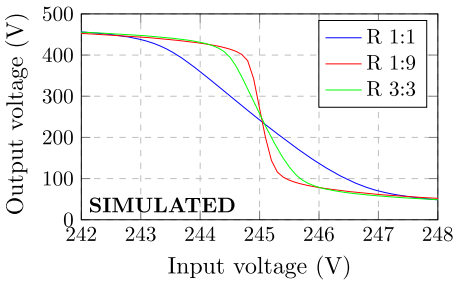
Table 4 shows the results of the biasing circuits monte carlo simulations. Quiescent voltage V_Q biasing is mostly limited by mismatch while I_Q biasing is mostly limited by process variability, more exactly by the reference transistor process variability. Quiescent current I_Q variance is still less than half of the non biased circuits, including mismatch and process variability. Better results could be

Table 1 OTA comparison

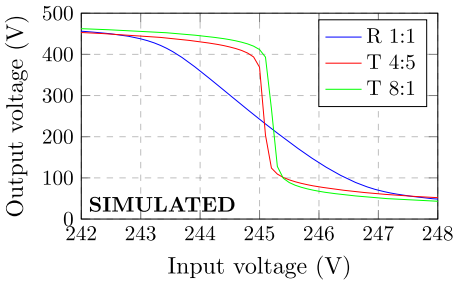
	Nauta	Vieru	B. Nauta	Hybrid
Tranconductance (G_m)	$2A$	$2A$	$2A$	$2A$
Total current (I_Q)	$8A$	$8A + 4B$	$4A$	$8A + 4B$
Diff. voltage gain (A_V)	0.5	0.5	1.0	0.5
C. M. voltage gain	$\frac{G_m}{G_m+G_o} \approx 1$	$\frac{G_m G_o}{(G_m+G_o)G_o} \approx 1$	$\frac{G_m}{G_{mb}+G_o} \approx \frac{1}{n-1}$	$\frac{G_m G_o}{(G_m+G_o)(G_{mb}+G_o)} \approx \frac{1}{(n-1)A_V}$

Table 2 Inverter comparison

	S_{eq}	I_Q		V_Q		A_V
	S_u	$\mu\,(I_{Qu} = 2.67nA)$	$\sigma/\mu\,(\%)$	$\mu\,(V_{Qu} = 245\text{mV})$	$\sigma/\mu\,(\%)$	$\mu\,(A_{Vu} = 118$ V/V)
R 1 : 1	1.00	1.00	6.64	1.00	0.96	1.00
R 9 : 1	9.00	8.98	2.24	1.00	0.32	1.00
R 1 : 9	0.11	0.12	2.23	1.00	0.32	6.11
R 3 : 3	1.00	1.08	2.22	1.00	0.93	2.58
T 8 : 1	0.89	0.92	6.23	1.00	0.92	11.9
T 4 : 5	0.19	0.21	2.89	1.00	0.40	14.0

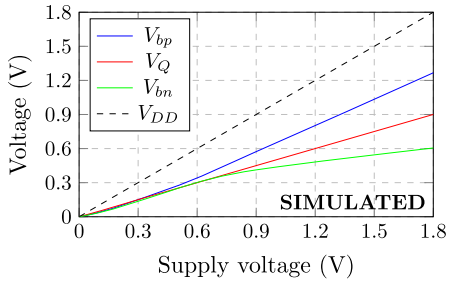


(a) Rectangular Array

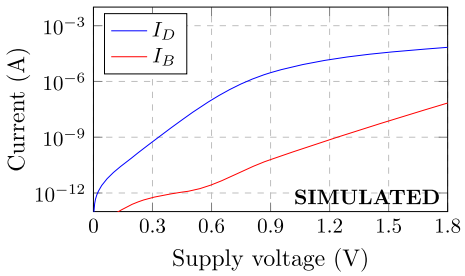


(b) Trapezoidal Array

Fig. 14 CMOS inverter DC transfer functions



(a) Biasing Voltages



(b) Biasing Currents

Fig. 15 V_Q biasing circuit

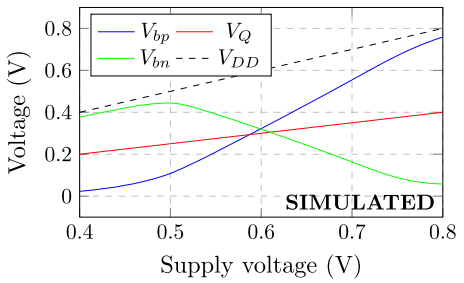
Table 3 Biasing circuit transistor dimensions

	P_0	N_0	P_1	N_1	P_2	N_2
m	8	8	64	64	8	8
W (μm)	3.0	1.0	3.0	1.0	3.0	1.0
L (μm)	0.5	0.5	0.5	0.5	0.5	0.5

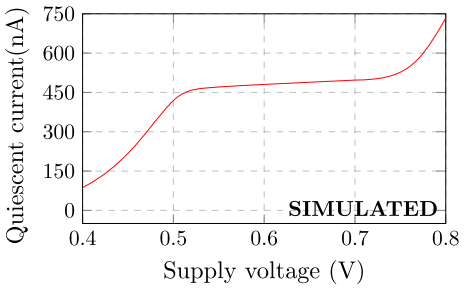
achieved with circuit calibration or an off-chip reference resistor.

4.3 OTA topologies

For proof of concept, four OTAs were designed for a 180 nm CMOS process, as examples of the push–pull based OTA topologies: Nauta, Vieru, proposed Bulk Nauta variation and Vieru–Nauta Hybrid. Transistor geometries



(a) Biasing Voltages



(b) Quiescent Current

Fig. 16 $V_Q + I_Q$ biasing circuit

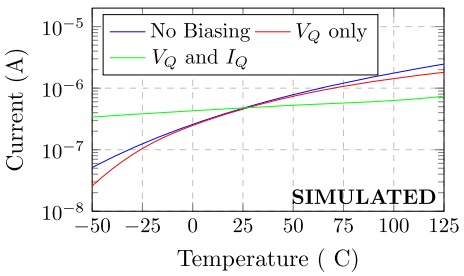


Fig. 17 Biasing circuits temperature dependence

for the designed amplifiers are detailed in Table 5. The inverter factors A and B are equal to 2 for every OTA. All OTAs were simulated at 27°C with a 500 mV power supply and typical process parameters.

4.4 Simulation results

Figure 19(a) and (b) show the DC transfer functions for differential and common mode signals respectively using the testbench shown in Fig. 18(a). Vieru and the Vieru-Bulk Nauta Hybrid show almost equal differential transfer functions, as expected. The Bulk Nauta OTA also shows a greater DC voltage gain. The Nauta OTA, although it has the same small signal differential voltage gain, has a decreased signal output voltage swing. Also, Nauta and Vieru OTAs have identical common mode transfer functions. The Bulk-Nauta OTA has a DC common mode voltage gain greater than unity, as expected, since the slope factor n is lower than two for this technology at the operation conditions. The Hybrid Vieru-Bulk Nauta OTA has a common mode voltage gain less than unity, as it combines the feedforward common mode cancellation from the Vieru OTA topology and the common mode attenuation from the Bulk Nauta OTA topology.

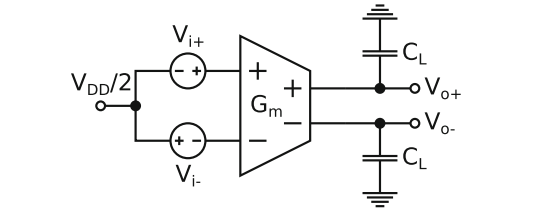
Figure 20 (a) and (b) show the open loop AC transfer function for differential and common mode rejection rate respectively. It was expected the same gain-bandwidth product for identical inverters and the same A factor, but body-biasing was different for each OTA. Although the same biasing circuit was used for both Nauta and Vieru

Table 4 Biasing circuit comparison

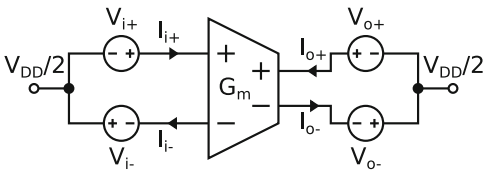
		Mismatch Only			Process Only			Mismatch + Process		
		μ (mV)	σ (mV)	σ/μ (%)	μ (mV)	σ (mV)	σ/μ (%)	μ (mV)	σ (mV)	σ/μ(%)
V_Q	V_{Q0}	306	0.02	0.01	306	6.65	2.18	306	6.70	2.19
	V_Q Biasing	300	1.41	0.47	300	0.01	0.00	300	1.57	0.52
	V_Q and I_Q Biasing	300	1.60	0.53	300	0.02	0.01	300	1.74	0.58
		Mismatch Only			Process Only			Mismatch + Process		
		μ (nA)	σ (nA)	σ/μ(%)	μ (nA)	σ (nA)	σ/μ(%)	μ (nA)	σ (nA)	σ/μ(%)
I_Q	I_{Q0}	500	14.0	2.85	500	113	22.65	500	115	23
	V_Q Biasing	481	12.8	2.67	481	112	23.3	481	115	24.0
	V_Q and I_Q Biasing	481	36.9	7.64	481	25.3	5.26	481	46.0	9.51

Table 5 Inverter Transistor dimensions

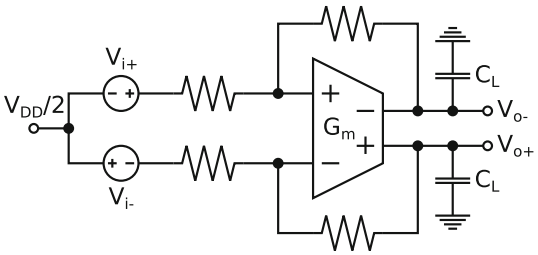
	P_0	N_0	P_1	N_1	P_2	N_2
m	2	2	16	16	2	2
W (μm)	3.0	1.0	3.0	1.0	3.0	1.0
L (μm)	0.5	0.5	0.5	0.5	0.5	0.5



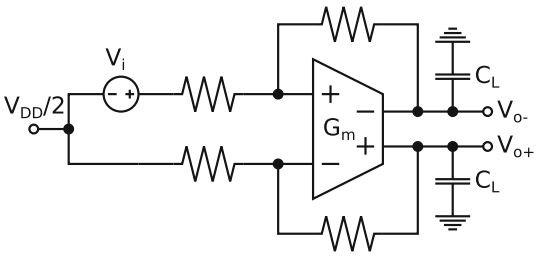
(a) Open loop



(b) Transconductance

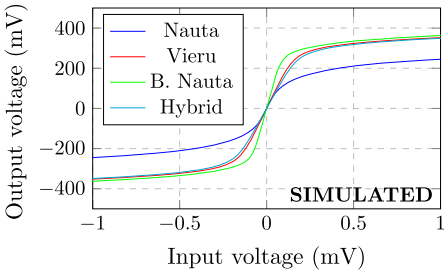


(c) Differential input unit gain buffer

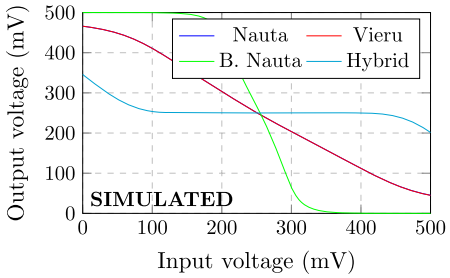


(d) Single input unit gain buffer

Fig. 18 Testbench diagrams

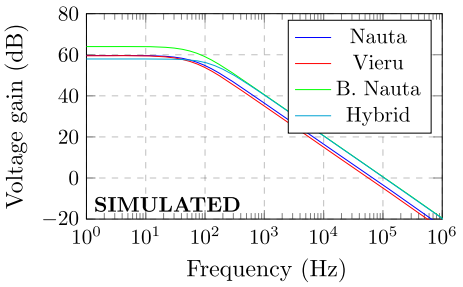


(a) Differential

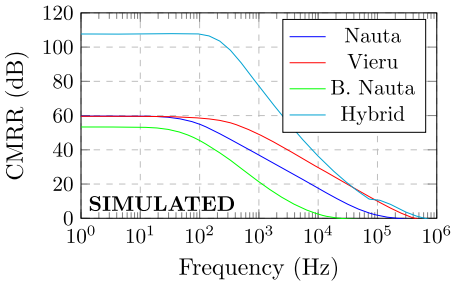


(b) Common Mode

Fig. 19 DC transfer functions



(a) Differential

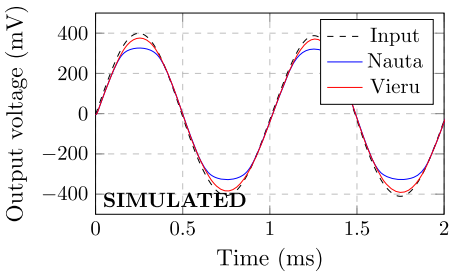


(b) CMRR

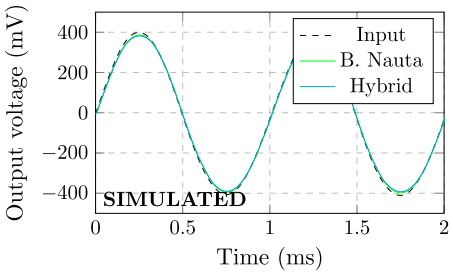
Fig. 20 AC Transfer Functions

OTAs, Vieru OTA has a larger area and, consequently, a larger forward biased diode between the source and bulk transistor terminals.

Figure 21 (a) and (b) show the transient differential response of Nauta, Vieru, Bulk Nauta and Hybrid Vieru-Bulk Nauta OTAs in a closed loop configuration as the one used in the testbench 18c. A 1 kHz 400 mV peak-to-peak input signal and 10 MOhm resistors were used. It can be shown, as expected from their respective DC differential transfer functions, that the Vieru OTA has a better output swing range. The Bulk Nauta and Hybrid Vieru-Bulk Nauta OTAs have a similar output response to the Vieru OTA, as they have similar DC transfer functions, as shown in Fig. 19(a).



(a) Nauta and Vieru



(b) Bulk Nauta and Hybrid Vieru-Nauta

Fig. 21 Transient simulations

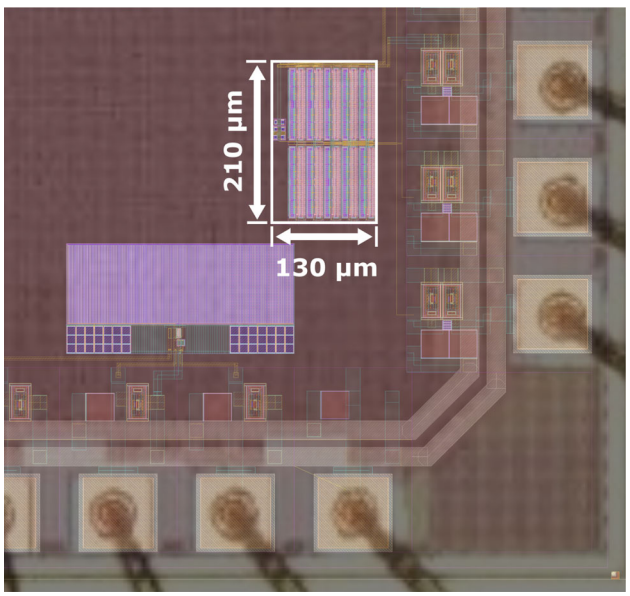


Fig. 22 Fabricated chip micrograph with layout overlay

4.5 Measured results

A prototype of the Hybrid Vieru-Bulk Nauta OTA was fabricated using the TSMC 0.18u MS/RF technology. Figure 22 shows the fabricated chip micrograph with a layout overlay. The OTA and its respective biasing circuit use a total area of 27300µm^2(210µmX130µm), and half of it is used for the OTA, as shown in Fig. 23.

Figure 24(a) and (b) show the open loop DC transfer functions for differential and common mode signals

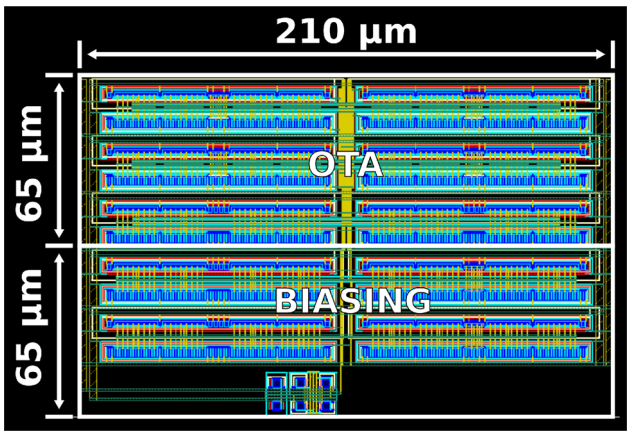
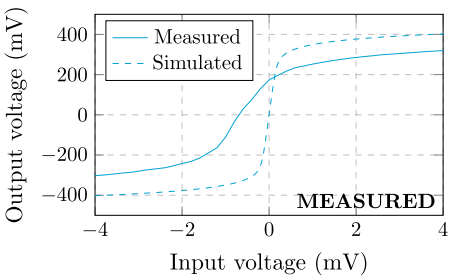
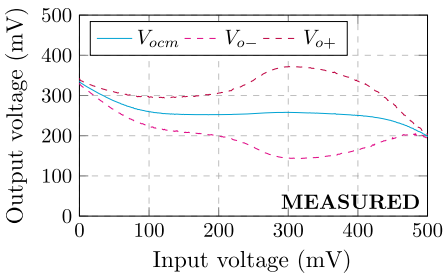


Fig. 23 Hybrid Vieru–Nauta OTA layout



(a) Differential

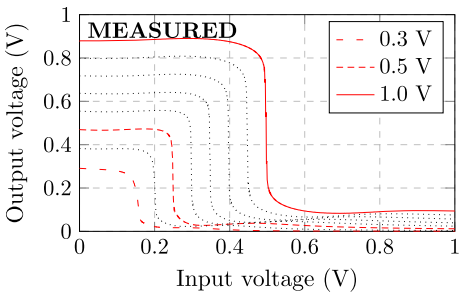


(b) Common Mode

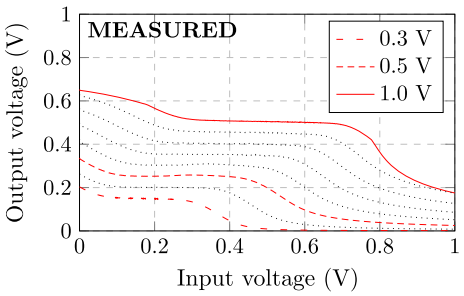
Fig. 24 Measured hybrid OTA open loop DC transfer functions

respectively for a 500 mV supply voltage. As it can be seen, there is a large output offset voltage which varies with the common mode input voltage. The maximum measured DC differential output gain is about 52 dB, which is lower than expected from simulation results. The output voltage range is also reduced.

Figures 25(a) and (b) show the open loop DC transfer functions for differential and common mode signals respectively for supply voltages ranging from 300 mV to 1 V in 100 mV steps. The differential input transfer function, shown in Fig. 25(a), shows the inverting output only. The common mode input transfer function, shown in Fig. 25(b), shows average of the non-inverting and inverting outputs. As can be noticed, for supply voltages greater than 500 mV, the output signal swing is degraded



(a) Differential



(b) Common Mode

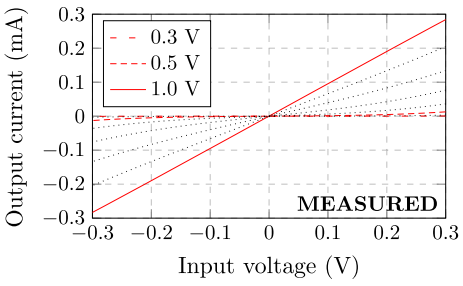
Fig. 25 Measured hybrid OTA open loop DC transfer functions

and never reaches full output swing, due to the parasitic current to substrate introduced by the Bulk Nauta OTA configuration. However, the output swing is still close to the voltage supply rails, the voltage gain is not considerably degraded and the output common mode voltage gain is still lower than unity.

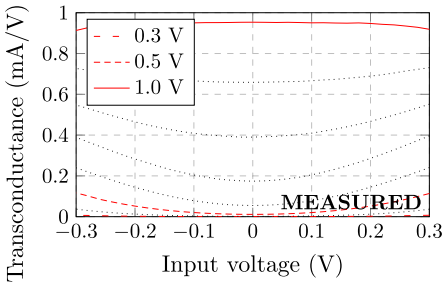
Figure 26(a), (b) and (c) show the measured differential output current, differential output transconductance and normalized output transconductance error results respectively. Since there is no quiescent current biasing for the fabricated Hybrid Vieru-Bulk Nauta OTA, the output transconductance increases as the supply voltage increases. Also, the linearity greatly improves with voltage supply, as the the transistors operates in higher inversion levels.

Table 6 summarizes the fabricated OTA measurements results. As can be seem, the differential voltage gain keeps almost constant for supply voltages greater than 500 mV. Below 400 mV, the differential voltage gain is greatly reduced, as the reverse transistor current is considerable and the transistor start to operate in the linear region and the trapezoidal transistor association output impedance improvement technique is no longer useful. The total current, including the biasing circuit was also measured as they shared the same voltage supply pin.

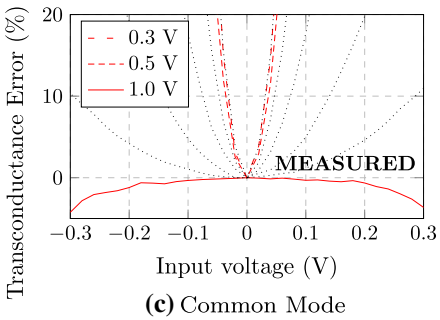
Figure 27 shows the measured output of the Hybrid Nauta OTA with a single 400 mV peak-to-peak square-wave input using the testbench from Fig. 18(d). This figure shows only the OTA negative output, which is about half the amplitude of the input signal. The differential output, however, is about the same of the differential input signal, considering that the negative input is held at a constant voltage of $V_{DD}/2$.



(a) Differential



(b) Common Mode



(c) Common Mode

Fig. 26 Measured hybrid OTA transconductance

Table 6 Hybrid Vieru–Nauta OTA Measurement Results Summary

V_{DD} (V)	A_V (dB)	A_{CM} (dB)	G_m (μA/V)	I_{DD} (μA)
0.3	36	−24	0.27	0.05
0.4	46	−40	1.82	0.33
0.5	52	−21	11.26	2.09
0.6	53	−18	54.79	11.22
0.7	52	−30	173.99	42.26
0.8	54	−33	390.08	127.68
0.9	52	−54	658.73	278.82
1.0	49	−22	953.46	507.71

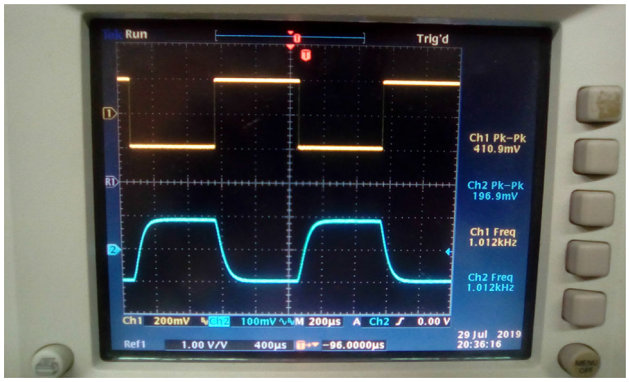


Fig. 27 Closed loop buffer OTA configuration transient measurement

4.6 Performance comparison

The performance achieved by the designed amplifiers and state-of-art counterparts is summarized in Table 7. Amplifiers [3, 10] and [12] are differential amplifiers with positive feedback for voltage gain enhancement. OTAs [9] and [12] are Vieru and Nauta OTAs respectively and they were designed for different processes with transistor parameters and geometries. For this reason, direct comparisons of those OTAs are impossible.

The original Vieru OTA [10] has a Figure of Merit for power efficiency much higher than its version simulated in this work. It has a different voltage gain from CMRR. Also, it uses positive feedback increase voltage gain. The Bulk Nauta OTA is the most efficient of the presented OTAs, but the higher efficiency is a trade-off with CMRR and current consumption and output common mode biasing. The Hybrid Vieru-B. Nauta OTA is as efficient as the simulated Vieru OTA and has a increased CMRR.

The OTA proposed in [3] uses two-gain stages and positive-feedback and its measured voltage gain is 10 dB greater than the proposed Hybrid OTA. Both use a similar area. Although they are equally efficient, the proposed OTA gain-bandwidth-product is three orders of magnitude lower.

The Nauta OTA proposed in [12] is a single-stage OTA with positive feedback to increase voltage gain. The Nauta OTA proposed in [1] is a single-stage OTA with rectangular arrays to increase gain. This work Nauta OTA has a much larger voltage gain using trapezoidal arrays alone, but it was designed for a different process and its voltage supply is twice as high than the one presented in [1].

5 Conclusion

Push–pull based amplifiers are very efficient and their common mode output voltage and quiescent current can be made more tolerant to process variability by using adaptive body-biasing. The proposed biasing circuits enabled forward-body-biasing for supply voltages above the ultra-low-voltage range up to nominal supply voltages by using pseudo-resistors to limit parasitic bulk current.

Rectangular and trapezoidal arrays can be used to improve voltage gain. CMOS inverters composed by trapezoidal arrays have a higher voltage gain per area ratio than rectangular array ones, however, they are more sensitive to mismatch.

Common mode rejection for differential amplifiers can be achieved by positive feedback, as in the Nauta OTA, or common mode feedforward, as in the Vieru OTA. The Nauta OTA is more power efficient than the equivalent

Table 7 Performance Comparison

	[3]*	[10]	[12]	[1]*	This work			
OTA topology	Other	Vieru	Nauta	Nauta	Nauta	Vieru	B. Nauta	Hybrid
Process (nm)	180	180	130	130	180	180	180	180
VDD (V)	0.5	0.6	0.5	0.25	0.5	0.5	0.5	0.5
DC Gain (dB)	62	64	37	25	60	60	64	58/52*
CMRR (dB)	75	31	31	43	60	60	54	108/73*
PSRR (dB)	82	-	90	47	60	61	51	64
GBW (MHz)	10.0	8.1	530	0.0072	0.07	0.06	0.10	0.10
Current (µA)	150.00	37.42	0.12	0.22	0.36	0.45	0.27	0.75
Load (pF)	20	10	-	30	10	10	10	10
PM (°)	60	90	90	90	90	90	90	90
Power (μW)	75	22.45	-	0.055	0.18	0.23	0.14	0.38
FoM**	133	216	-	98	194	133	370	133
Area (mm x mm)	0.017	-	-	0.052	-	-	-	0.014

* Measured results, ** $FoM = 100 \times UGBW \times C_L/I$

Vieru OTA using the same CMOS inverter cells, while designed to have the same differential and common mode voltage gain. However, the Vieru OTA has a larger output voltage excursion.

The proposed Bulk Nauta OTA use forward-body-biasing to implement common mode rejection, achieving a higher power efficiency than a similar Nauta OTA, at the cost of CMRR and biasing options. The proposed Hybrid Vieru-Bulk Nauta OTA further enhance common mode rejection of the Vieru OTA at the cost of more area usage and more complex biasing circuits.

Acknowledgements The author is grateful to FEESC, CAPES, CNPq, IC-BRAZIL program and to MOSIS Educational Program for the financial support, PDK licensing and fabrication.

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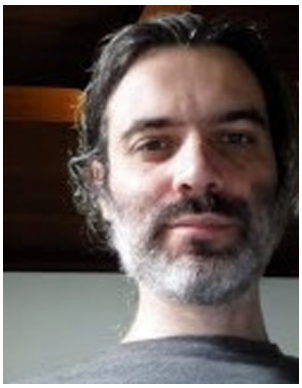

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