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ORIGINAL PAPER

Design of efficient 22 nm, 20-FinFET full adder for low-power and high-speed arithmetic units

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Abstract

The design of a 20-FinFET novel full adder (NFA) with a new architecture employing Double Gate-FinFETs is presented in this work. The feature of new topology is, the input carry of full adder has to traverse through single transistor, by which the speed of full adder is enhanced. Carry propagation is a critical factor in determining the speed of multi-bit adders like carry choose adders, carry save adders, and ripple carry adders, hence input carry is chosen above the other two inputs. The proposed NFA eliminates the complex XOR/XNOR functions for the generation of sum and output carry. The power factor is also addressed in the design, which is reduced by employing a NOR topology in the first stage of the complete adder and designing it using FinFETs at 22 nm and low supply voltage. The circuit's different topology is designed so that the number of 'n' and 'p' type FinFETs is balanced. The proposed NFA is designed and extensively simulated at 22 nm by testing its performance with various supply voltages like 0.6 V, 1 V, 1.2 V and 1.5 V using Cadence Virtuoso, ADE, ADEXL design suite. The NFA outperforms the existing full adders by reducing the delay and power dissipation by 23%- 31% and 15%—23% respectively.

Keywords Digital VLSI · Full adder · Carry propagate · DG-FinFET · Cadence

1 Introduction

Carry propagation in most of the multi-bit adders is a challenging task for the designer when speed is the major specification. If the carry of full adder (FA) is produced at faster rate, the speed of addition can be enhanced to some extent. The design of full adder based on transmission gates, simple MOSFETs and complementary logic in which the charging and discharging may be the major concern as per [18]. The work of [7] focuses on the design of full adder using three separate modules, by improving the performance of each module using transmission gates and pass transistors. But if the technology is below 45 nm, its irregular structure may not produce intended output for low-threshold transistors like FinFETs [28]. Few of the previous works on full adder design targets to minimize the transistor count using simple pass transistor logic with compromise in full logic swing [2]. The circuit design using double-pass transistors and simple pass transistors suffer from threshold drop, and is not preferable at lower technology nodes, by which the output voltage swing may be reduced [1]. The hybrid full adder designs uses various logic styles for improving the performance of modern day central processing units [4, 8, 29]. As the technology scales down, the circuit topology and logic style becomes significant in deciding the proper operation of the circuits [26]. The choice of logic style also has possible impact on full adder circuits as studied in [21] and [9]. Elimination of XOR gates and replacing them with CMOS NOT, NOR, NAND and Majority-NOT gates also improves the performance of the full adders [20]. Therefore, the efficiency of full adders may be improved by changing the logic gates. The applications of full adder has been extended to the field of image processing as given in [23].

Initially, full adders are incorporated in design of multipliers and then in multiplier–accumulator units for image processing applications. The CNTFET technology is also considered for the design of various topologies of full adder circuits, and are being proved as most robust [16]. Finally the sub-blocks required for full adders can also be designed using FinFETs. Few of the basic gates are implemented using FinFETs at lower technology nodes as shown in [19,

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28] and [14]. The era of FinFETs has mushrooming applications in the future VLSI design [24], therefore authors proposed a distinct architecture for the design of full adder using FinFETs. FinFET based circuits are best suitable for low-power design in current scenario of VLSI without compromise in speed [10, 17], and [11].

2 Existing Hybrid Full Adders (HFA)

The proposed HFA is compared with existing HFAs; the existing designs considered are [1, 3, 15], and [13]. The [1] design internally has four modules to generate complex XOR/XNOR, AND/OR functions and two multiplexers are used in second stage for the generation of FA SUM and output carry as shown in Fig. 1(a).

The design [15] is the modified design of [1] by replacing AND/OR logic module with NAND/NOR module as shown in Fig. 1(b). Both [15] and [13] designs improved the performance using three internal modules as shown in Fig. 1(c). The proposed NFA design has three modules which do not use pass transistors and XOR/XNOR logic to obtain the FA_SUM and output carry(FA _COUT) of FinFET based full adder circuit.

The module I of [15] and [13] is constructed using 8 T and 10 T respectively. The performance was improved in both cases. The suggested 1-bit adder's CBSC is compared to existing designs' module I such as [3, 12, 22] and [13] as shown in Fig. 2 (a-d). All the existing designs for Module

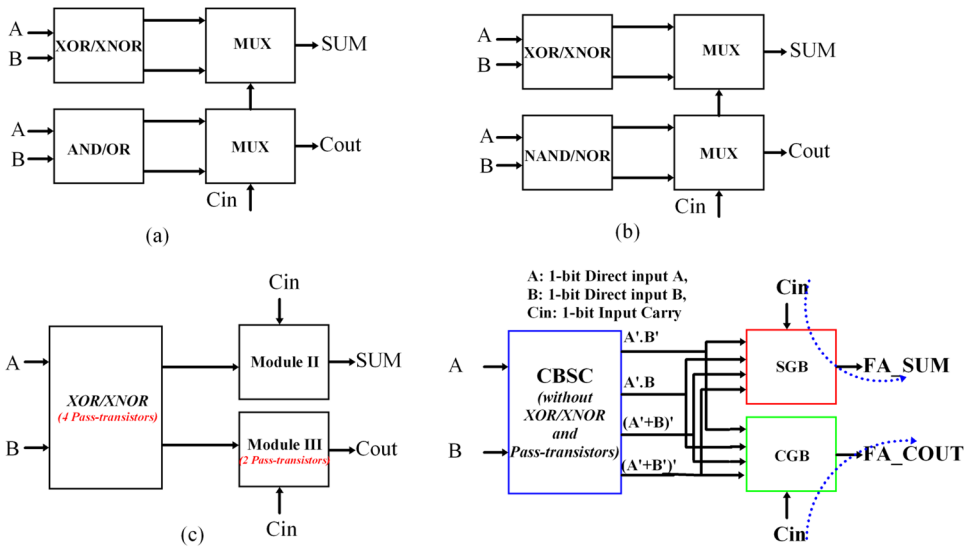

Fig. 1 Design by (a). [1] (b). [15] (c). [13] (d). Block diagram of proposed NFA

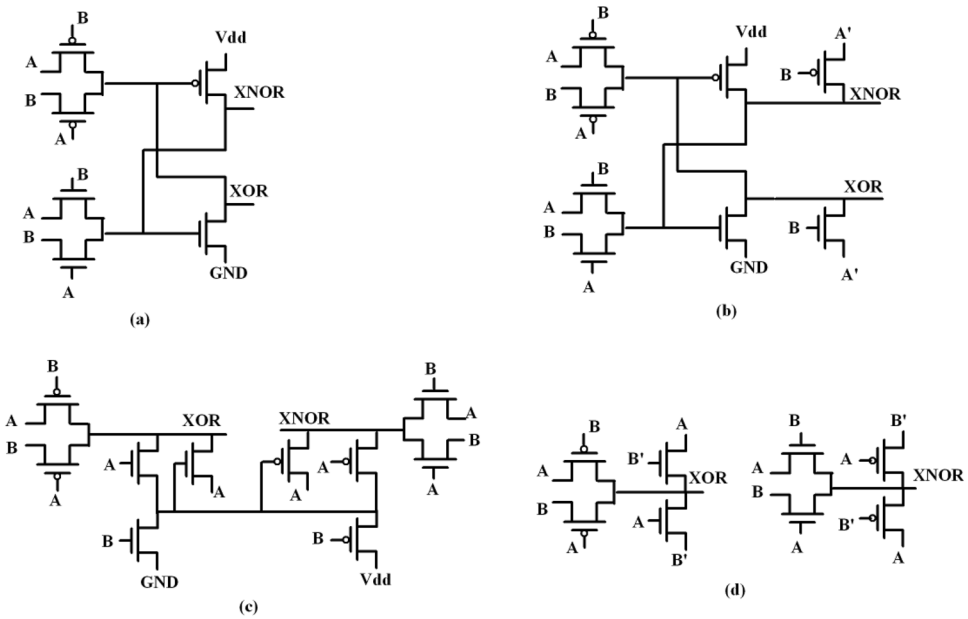

Fig. 2 Module I design of full adder designed by (a). [22], (b). [3], (c). [12] and (d). [13]

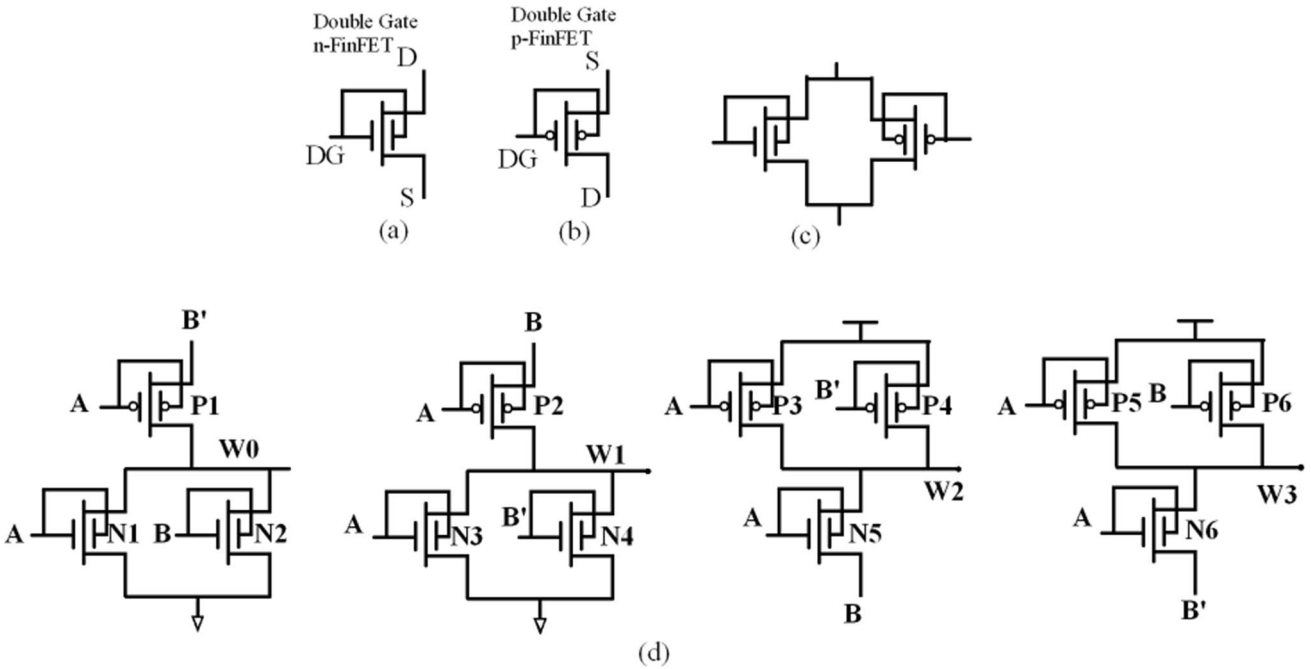

Fig. 3 CBSC design of proposed full adder

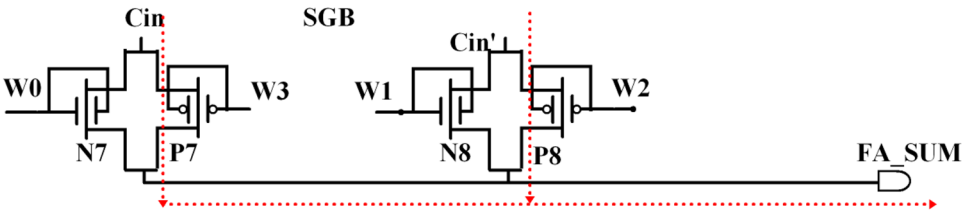

Fig. 4 SGB design of proposed full adder

I enhanced the performance by implementing the complex XOR/XNOR functions. The module III of [13] uses n-type transistors for both pull-up and pull-down, which is not suggested at lower technology nodes. But the direct inputs A and B of full adder are given to n and p-type pass-transistors. The threshold drop of these pass-transistors lowers the output voltage swing and would be a major concern at lower technology nodes.

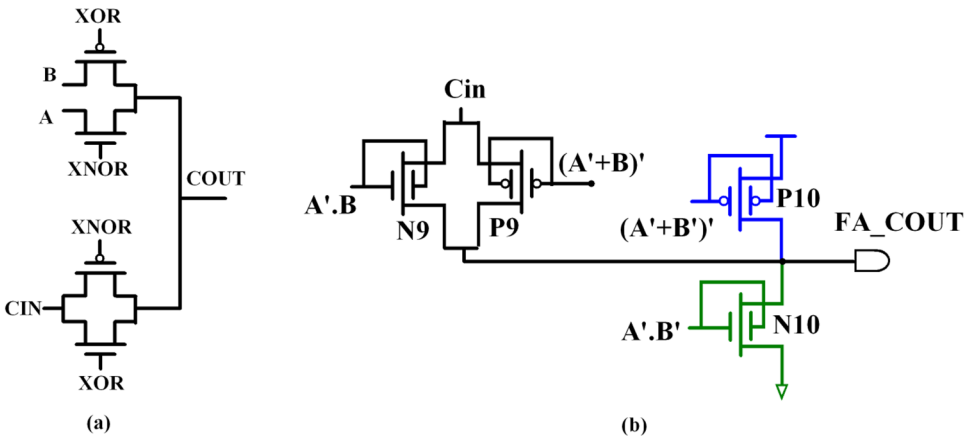

Fig. 5 Comparison of (a) Module III of [13] with (b) proposed CGB module

Table 1 Description table for FA COUT Generation

A	B	FA_COUT generation
0	0	1; Pulled-down to 0 through N10 without waiting for Cin0
0	1	depends on Cin; propagated through single TG
1	0	depends on Cin; propagated through single TG
1	1	1; Pulled-up to 1 through P10 without waiting for Cin

3 Proposed Novel Full Adder (NFA)

The proposed NFA design has three modules which do not use simple pass transistors and XOR/XNOR logic to obtain the FA SUM and FA COUT of FinFET based full adder circuit. The design uses FinFETs which results in low power dissipation at lower technology nodes [10]. The type of logic style, topology, and selectively using transmission gates improves the performance of a circuit [9]. The proposed design also uses mixed logic style to improve the performance. Figure 1(d) depicts a block diagram of the proposed NFA. The Common Block for Sum and Carry (CBSC) generates the terms such as (A'.B'), (A'.B), (A' + B') and (A' + B). These outputs are given to Sum Generation Block(SGB) and Carry Generation Block(CGB). The propagation delay of carry is reduced by passing input carry (Cin) through single transmission gate of each block as shown in Fig. 1(d).

3.1 Common Block for Sum and Carry (CBSC)

The symbols used in this paper for Double Gate-FinFET n-type, p-type and transmission gate are shown in Fig. 3(a-c). The authors of the paper made an effort to eliminate pass-transistors and complex XOR/ XNOR functions in the module; this module is designed distinctly similar to CMOS topology targeting to attain maximum logic swing at low voltages, and is shown in Fig. 3(d). The direct inputs A and B of proposed NFA are given to CBSC; therefore, this module outputs do not rely on input carry. It produces four outputs W0, W1, W2 and W3. The expressions of the four outputs are given below.

$$W0 = A'.B' \tag{1}$$

$$W1 = A'.B \tag{2}$$

$$W2 = (A' + B)' \tag{3}$$

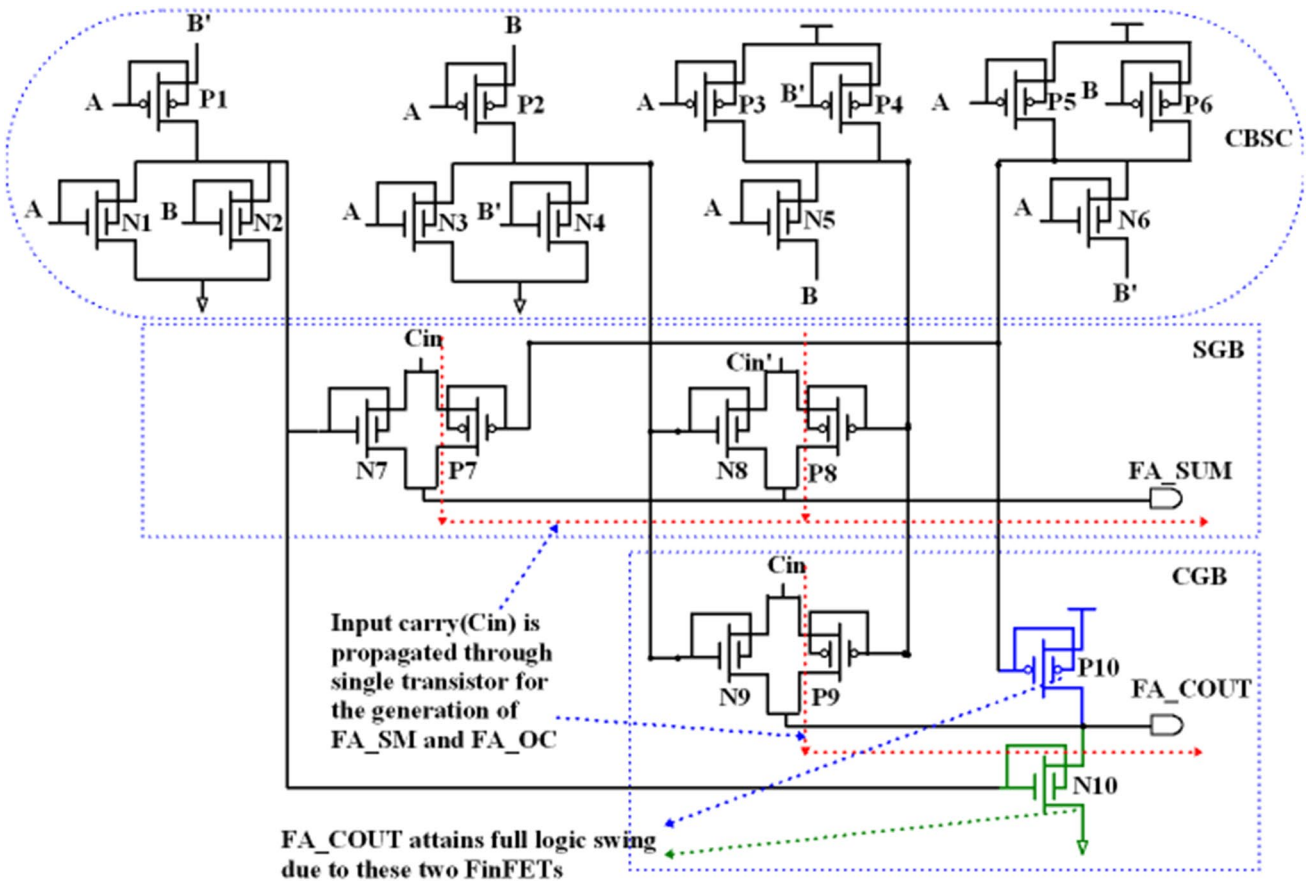

Fig. 6 Complete circuit of proposed Novel Full Adder (NFA)

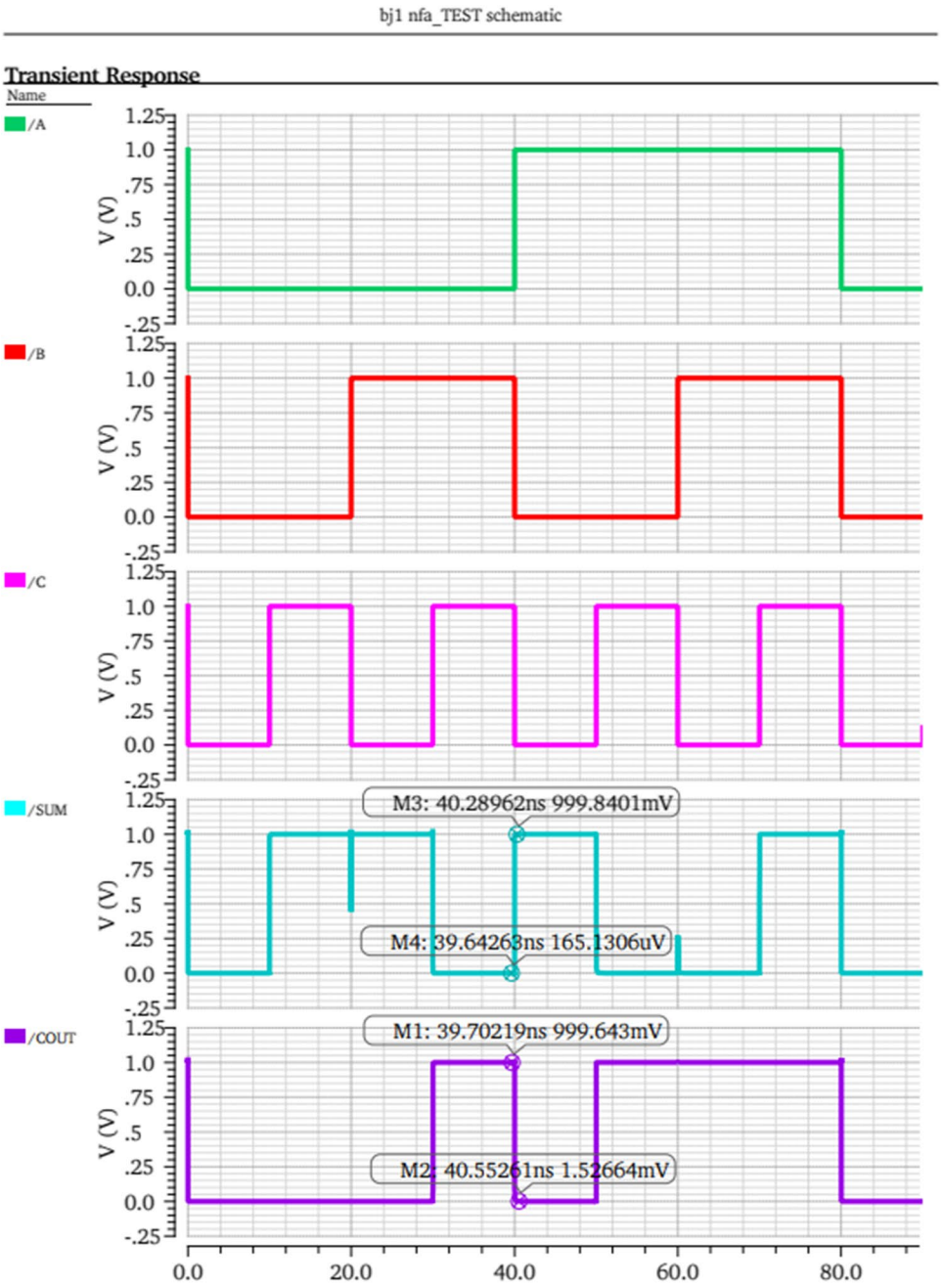

Fig. 7 Transient response of proposed NFA design

$$W3 = (A' + B')' \tag{4}$$

$$FA\_SUM = W0.Cin + W3'.Cin + W1.Cin' + W2.Cin' \tag{5}$$

$$FA\_COUT = W1.Cin + W2.Cin + (A.B) \tag{6}$$

3.2 Sum Generation Block (SGB)

The SGB of proposed FA is designed using only two transmission gates (TG) for the generation of FA SUM, and is shown in Fig. 4. The expression of the FA SUM and FA COUT for eliminating XOR/XNOR and pass transistors is shown in Eqs. (5) and (6). The input carry (Cin) is not given to CBSC, and is fed to SGB and CGB. The Cin has to propagate through only single TG in this module for the generation FA SUM. The carry propagation time is reduced in the proposed SGB.

3.3 Carry Generation Block(CGB)

The CGB of the proposed FA is compared with module III of [13]; it uses pass transistors for the generation of COUT

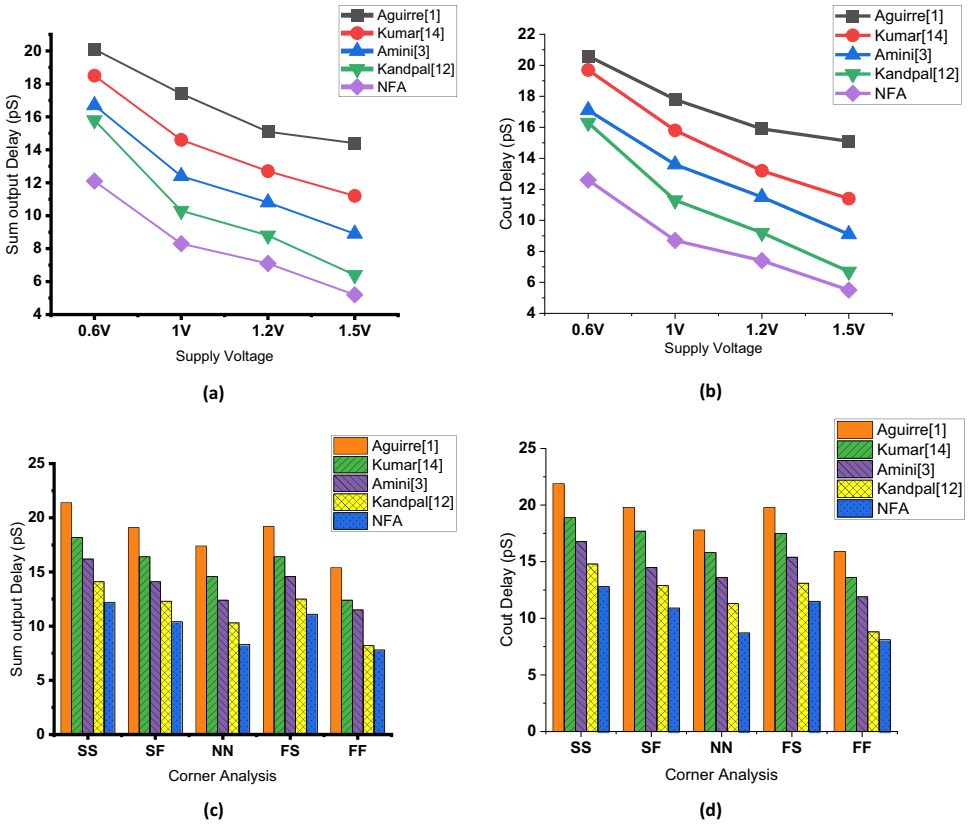

Fig. 8 Delay comparison for producing the (a). FA_SUM output (b). FA_COUT (c). Corner analysis of Delay comparison for producing the FA_SUM output (d). Corner analysis for producing the FA_COUT

which leads to the degradation of output voltage as shown in Fig. 5(a). The rearranged expression of the FA COUT for eliminating XOR/XNOR and pass transistors is shown in Eq. 6.

The proposed CGB is better in terms of voltage swing and noise margin at lower supply voltages. The module III constructed with single TG, p-FinFET connected to supply voltage, and n-FinFET connected to ground as shown in Fig. 5(b). This topology produces maximum voltage swing for FA COUT (FA OC). The inputs for p-FinFET and n-FinFET are taken from w3 and w4 of CBSC respectively. The FA OC is produced at a faster rate as input carry has to propagate through the signal transmission gate, which require less time for carry propagation. The details of the FA COUT generation is shown in the Table1.

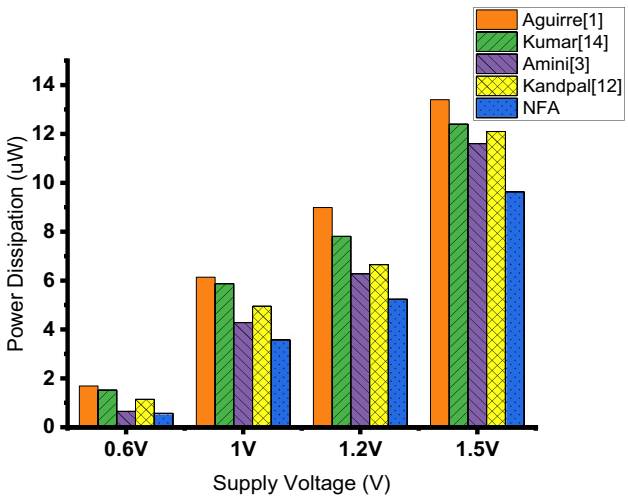

Fig. 9 Power dissipation comparison results

3.4 Features of proposed NFA

The complete circuit of NFA with three modules using 20 T is shown in Fig. 6.The CBSC is constructed and designed using 12 T. The design of SGB and CGB uses 4 T each. The main advantages of the proposed NFA are listed below,

- Pass-transistors are completely removed to improve the voltage swing.
- Complex XOR/XNOR modules are not used for the generation of the FA SUM and FA COUT of proposed NFA.
- The FA COUT is produced at faster rate as there exists single TG in the path from input carry.
- The design has equal number of p and n type transistors; 10 T of each type to maintain uniformity and high package density similar to CMOS.

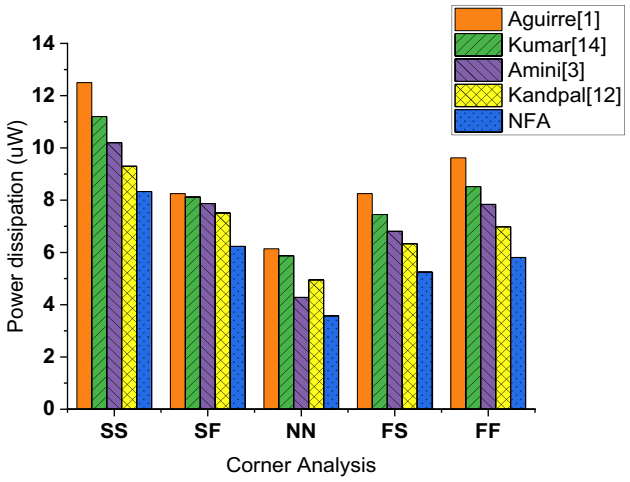

Fig. 10 Corner analysis of Power dissipation comparison results

- Appropriately uses p-type transistors above the output node and n-type transistors below the same node.
- Robust to supply voltages and for lower technology nodes as it exhibits similar attributes of CMOS.
- It consumes less power due to new architecture module I of proposed NFA.
- It exhibits less propagation delay as 12 T module I relies only on the direct inputs but not on the input carry which is normally taken from previous FA in cascaded structure.

4 Analysis and Results comparison

4.1 Simulation set-up

The Virtuoso schematic and Analog Design Environment of Cadence are used for the design, simulation, power and delay analysis [6]. The model libraries of 22 nm High Performance-FinFET technology are collected from [30] and [5].

The model files of both n and p type FinFETs are included to spectre working directory of all the designs during extensive simulations. The stimulus bit patterns such as "00,001,111", "00,110,011", and "01,010,101" are chosen for A, B, and Cin inputs of proposed FA, respectively. The logic '0' value for all the inputs is given as 0 V. The logic'1' value is varied as 0.6 V, 1 V, 1.2 V, and 1.5 V according to different supply voltages to test the robustness of the circuits. The 22 nm model library of DG-FinFET is attached to the Virtuoso ADE while performing simulations. The 1fF of capacitance is connected as load for all the full adders. The ADEXL of Virtuoso [27]is used for Montecarlo analysis for all the designs. The particular model files such as NN, SS, SF, FF, and FS are properly selected for corner analysis as per [25].

The mean of power and delay for 500 simulations each are considered in Montecarlo analysis. The proposed NFA and all the existing designs are simulated at various frequencies ranging from 500 MHz to 4 GHz, to test the range of frequency with which the proposed NFA produces a valid

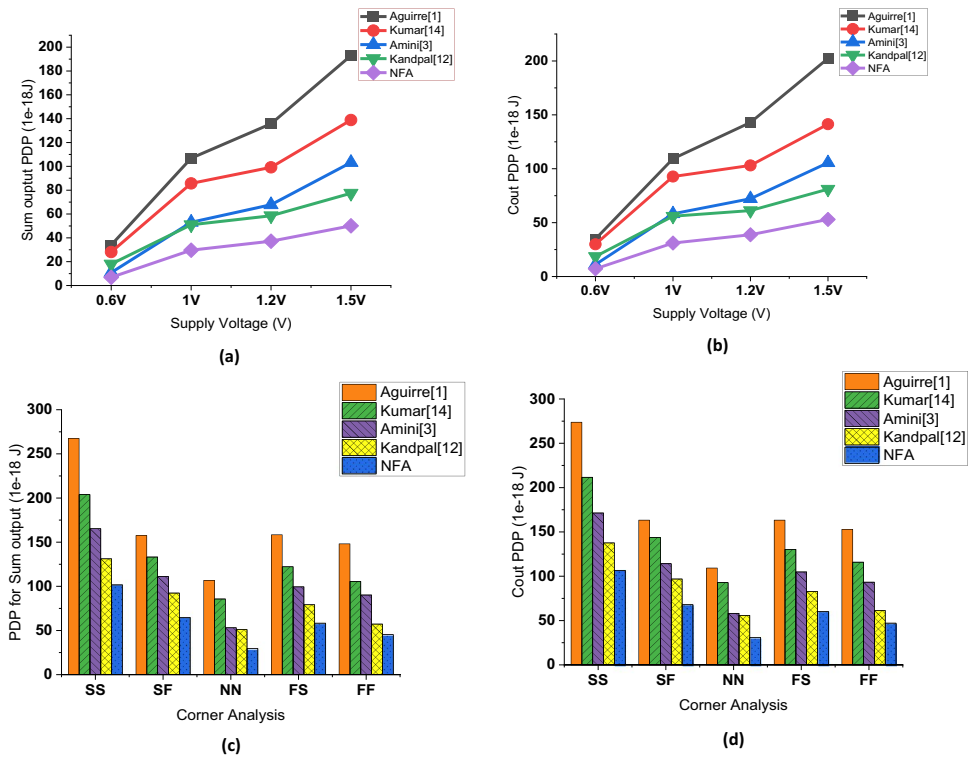

Fig. 11 (a). PDP comparison results for the FA SUM generation (b). Corner analysis of PDP results for the FA_SUM generation (c). PDP comparison results for the FA_COUT generation (d). Corner analysis of PDP results for the FA_COUT generation

Table 2 Description table of Transistors count

Design	Pass Transistors		Pull-up	Pull-down	Transmission Gates (n + p)	Total Count
	P	N	P	N		
Aguirre[1]	7	7	3	3	4(8)	28
Kumar [14]	6	7	3	3	4(8)	27
Amini [3]	6	6	-	-	3(6)	18
Kandpal [12]	5	5	2	2	3(6)	20
Proposed	-	-	7	7	3(6)	20

output voltage. All the designs are simulated and verified with -50 degree to + 50 degree centigrade temperature range.

4.2 Delay analysis

At 1 GHz input frequency, the proposed 1-bit FA is simulated for transient and power analysis for 0.6 V, 1 V, 1.2 V, and 1.5 V. The full swing transient response of the proposed NFA is shown in Fig. 7. The time period of the inputs A, B, and Cin is chosen as 80 ns, 40 ns and 20 ns respectively for the transient analysis. For best result analysis and comparison, all the existing designs are simulated with same time periods. The outputs of NFA such as FA SUM and FA COUT signals transition is compared with input carry signal (Cin); as Cin has more number of transitions. Specifically, the delay is measured during the input (A, B and Cin) transition from"011″ to"100″; as every input bit changes its state. This transition is considered for the worst case delay calculation. As the proposed design targets to reduce carry propagation time; therefore, the delay is minimized by 23–31% compared to [13], as it offers lower delay among the existing designs which are considered for analysis. Figures 8(a) and 8(b) demonstrate the delay comparison of the FA SUM and FA COUT outputs for proposed and current designs, respectively. The FA SUM and FA COUT delay corner analysis (SS, SF, NN, FS, FF) of NFA for 500 iterations are shown in Fig. 8 (c-d).

4.3 Power and PDP analysis

Few of the previous FAs have not produced full swing output for certain low supply voltages due to threshold drop across pass-transistors; mainly at supply voltages 0.6 V and 1 V. The power comparison is carried out using Virtuoso ADEL through DC analysis. The total power is calculated using the tools of Cadence Virtuoso ADEL. The power is carried out for existing and proposed FAs by varying the supply voltages; the proposed FA consumes 15–23% less power than existing designs. The power comparison results are shown in Fig. 9.

The power corner analysis for 1 V (SS, SF, NN, FS, FF) of NFA for 500 iterations is carried out using Cadence Virtuoso ADEXL, and is shown in Fig. 10. At the outset, proposed FA is proved to be optimized as it's PDP is reduced by 38–54% over existing designs. The PDP comparison results for both FA SUM and FA COUT outputs are shown in Fig. 11(a) and 11(b). Figure 11(c) and 11(d) illustrate the PDP corner analysis (SS, SF, NN, FS, FF) of NFA for 500 iterations, respectively.

4.4 Transistors count analysis

The proposed full adder requires 20 FinFETs, and the count of n-FinFETs & p-FinFETs is same i.e. 10. The proposed NFA completely eliminates p- and n-type pass transistors. It is constructed to obtain full output swing, in which p-FinFET are placed at pull-up side, n-FinFETs are placed at pull-down side. In the previous works such as [1, 3, 15] and [13] uses simple pass transistors in their design, which may degrade the output voltage level at lower technology nodes. The previous design such as [3] uses only 18 T but has pass transistors.

Therefore, the proposed NFA uses 20 T by completely eliminating pass transistors, which is best suitable for FinFET technology. The transistor count details of proposed and existing designs, and pass transistors' elimination in proposed design are shown in Table2.

5 Conclusion

The circuit design, modelling, and Monte Carlo analysis of a novel full adder employing 20 T are presented in this paper. The proposed work describes the design of novel full adder using Double Gate FinFETs without pass transistors. A new topology of hybrid full adder reduces the delay due to carry propagation from input to output node. The design process and functional verification of NFA is done at 22 nm technology using Cadence Virtuoso, ADE and ADEXL. The NFA is simulated and tested at various supply voltages. The corner analysis of the proposed adder is carried out by doing Montecarlo simulation using Cadence ADEXL. In terms of power dissipation and time, the suggested NFA outperforms previous designs; the reduction in power dissipation and delay is 15%-23% and 23%-31%, respectively,

when compared to conventional full adder circuits. The suggested NFA is also better than existing hybrid full adders, according to the Montecarlo study.

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Authors' contributions All authors contributed to the study conception and design. Material preparation, data collection and analysis were performed by [B. Jeevan] and [K. Sivani]. The first draft of the manuscript was written by [B. Jeevan] and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

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Data availability The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

Declarations

Ethics approval Not Applicable (as the results of studies does not involve any human or animal).

Consent to participate Not Applicable (as the results of studies does not involve any human or animal).

Consent for publication All authors approve the final manuscript.

Conflict of interests/ Competing interests The authors declare that they have 'no known conflict of interests or personal relationships' that could have appeared to influence the work reported in this paper.

Research involving human participants and/or animals Not Applicable (as the results of studies does not involve any human or animal).

Informed consent All authors read and approved the final manuscript.

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