IET Renewable Power Generation

Research Article

IET Journals
The Institution of Engineering and Technology

Differential current-based fault protection with adaptive threshold for multiple PV-based DC microgrid

ISSN 1752-1416
Received on 14th June 2016
Revised 23rd December 2016
Accepted on 8th February 2017
E-First on 11th April 2017
doi: 10.1049/iet-rpg.2016.0577
www.ietdl.org

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Abstract: A new differential current-based fast fault detection and accurate fault distance calculation is proposed for photovoltaic (PV)-based DC microgrid. A multiterminal direct current (MTDC) distribution network is studied as an adequate solution for present low-voltage utility grid scenario, where local distributed generators (DGs) are incorporated primarily by power electronics based DC–DC converters, DC–AC voltage-source converters (VSCs). PV and diesel generator (as auxiliary source) are considered for cascaded common DC bus, and AC utility bus integration is achieved by VSC unit for the proposed MTDC network. DC microgrid protection is quite significant research focus due to the absence of well-defined standards. Pole-to-pole, pole-to-ground, PV-side DC series and ground arc faults are basically considered as DC distribution network hazards. A discrete model differential current solution is considered to detect, classify and locate the faults by modified cumulative sum average approach. A comprehensive case study is presented with different DC loadings, to deliberate effectiveness of the proposed protection scheme in terms of percentage error and trip time (*Ts*). The result verification is conducted in MATLAB environment as well as *TMS320C6713 digital signal processor*-based test bench with the proposed multiple DGs based DC microgrid.

1 Introduction

Challenges associated with DC microgrid protection are due to lack of well-defined protection standards [1]. AC breakers are cost effective as compared with fast-acting DC switches [2]. The primary focus associated with DC distribution protection is fast detection of fault occurrence and disconnection of power converter units [voltage-source converter (VSCs), DC–DC converters, AC–DC rectifiers etc.] to provide protection from high-fault current surge. Most possible faults to the DC systems are: *pole-to-pole* (PP) and *pole-to-ground* (PG) faults. Fault path between positive and negative lines are responsible for PP fault, whereas fault path between positive/negative line to ground is the cause of *PG* faults [3]. Though PP faults are most general protection hazard condition, *PG* faults are complex to determine. However, while connecting with photovoltaic (PV) system, there is a contingency of DC arc fault [3]. PV configurations are more prone to DC arc faults, while they are constructed in both series, and parallel manner (i.e. modules, panels and arrays) for a larger system [4]. A PV system higher than 80 V (rated) penetrating local/utility network is suggested to incorporate arc fault circuit interrupter (AFCI) device as protection measure, according to the Article 690.11 of National Electrical Code (NEC), 2011 [5]. Earth capacitance measurement and time-domain reflectometry are considered for location identification of PV arc faults [6]. Series, intra-string parallel, cross-string and arcing ground faults (GFs) are introduced as possible crisis for any PV configuration [6]. To design fault protection scheme, Underwriters Laboratory (UL) 1699B, 'Photovoltaic DC Arc Fault Circuit Protection', standard technical panel are followed. In this paper, DC series and ground arc faults [7] are emphasised. These types of faults occurred during high-resistive arc-gap path or no proper grounding of PV arrays. These types of faults are complex to identify because of their low-surge fault current.

Owing to the presence of power electronics converter controls fast fault detection and location estimation is facing difficulties, especially for DC microgrid applications. The accuracy of travelling-wave-based fault detection, proposed for DC network is dependent on accurate detection time calculation and requires high-performance data acquisition tools [8]. Reflected wave-based detection and identification are studied. Inaccuracy of these methods is found due to short-distance DC cables. Active impedance estimation-based fault protection is proposed for marine DC networks [9]. A probe power unit (PPU)-based non-iterative fault location is proposed for low-voltage DC microgrid [10]. This method uses an extra equipment to measure the DC fault location. Line differential current-based fault estimation is listed [11], where iterative solution with complex pole calculation of line current is proposed. A new differential current-based fast detection and accurate fault location is proposed in this paper. The fault detection thresholds for various fault resistance are volatile in nature when primary distributed generators (DGs) are renewable, and thus minimum and maximum permissible fault resistance detection threshold is calculated adaptively using piecewise cubic hermite polynomial (PCHP) interpolation [12]. Differential current-based solutions are mainly considered for fault detection and relaying operation in the existing literature. Fault distance calculation by means of line impedance calculation is included as a separate solution in the literature. These calculations are performed through numerical solutions (i.e. travelling-wave theory, wavelet transform, principal component analysis etc.) using voltage and current expressions during faults. A fast and simple fault detection as well as distance measurement scheme is presented in this paper, where non-iterative calculation is focused to ensure fast computation. Furthermore, the proposed fault detection scheme is effectively designed to detect PV arc faults (series, ground) for PV-based DGs. Non-iterative fault detection and fault distance calculation for PV-based DC microgrids are the key features of the proposed differential current-based protection scheme.

After a brief introduction to the motivation and recent trends of DC microgrid protection in Section 1, utility grid interactive multiterminal direct current (MTDC) distribution network is discussed in Section 2. Sections 3 and 4 provide the fault detection and location methods, respectively, while several fault case studies with or without DC loads are considered in Section 5. Concluding remarks are given in Section 6.

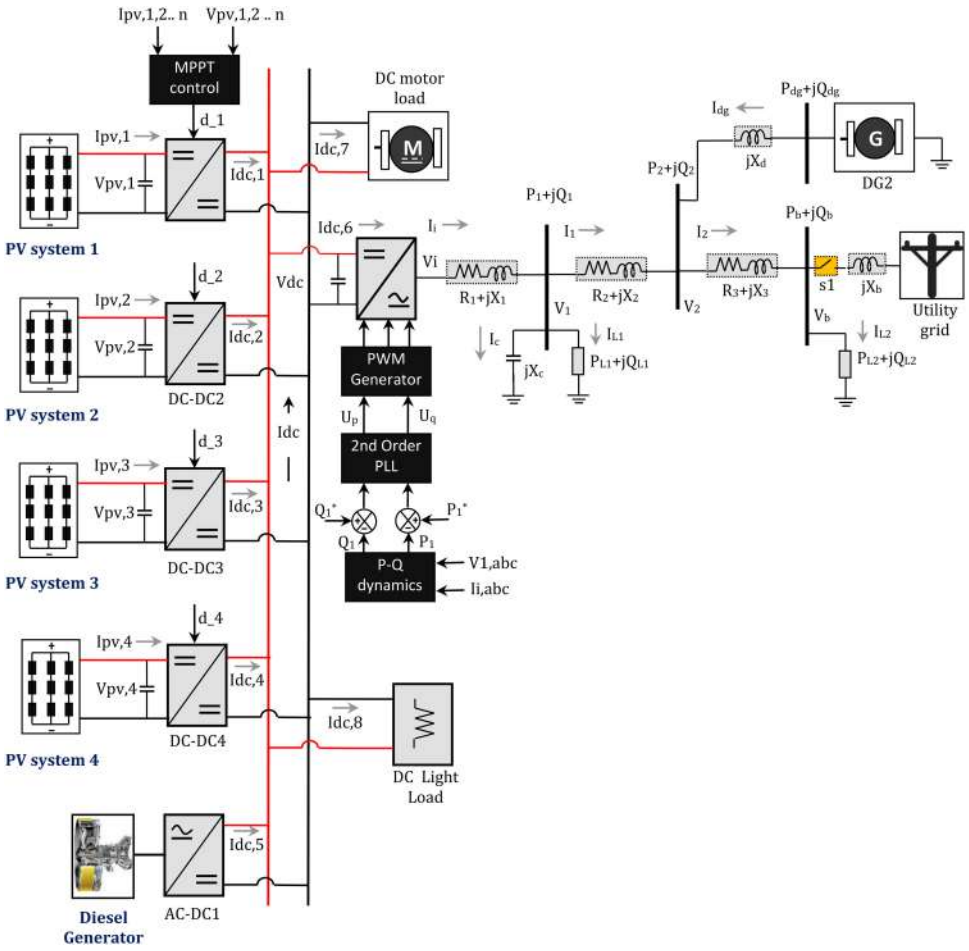

Fig. 1 *Schematic representation of multiple DGs based DC microgrid integrated with utility (AC) bus*

Table 1 Proposed network parameters with generation unit

	PV-based DC bus parameters
PV system power rated (kW)	4 × 100 kW (individual) = 400 kW
DC converter (buck type) rated	4 × 108 kW (+ 8% IEC 6210); 470 V (DC)
DC bus rated	500 V; R_{dc}→121 mΩ/km; L_{dc}→0.97 mH/km; C_{dc}→12.1→nF/km; R_{ground}→0.5 Ω
	VSC parameters
voltage converter parameters	operational frequency→ 60 Hz; 400 kW, 260 V (AC) to step-up. DC-link capacitor→100 μF
VSC PLL control (second order)	*switching frequency*→5 kHz; proportional (K_p) gains 7, 9.8; integral (K_i) gains 32, 20
line parameters	*line voltage(L–L)*→25 kV (AC) after step-up; R_1, X_1 (2.5 km)→0.074 Ω, 2.61 mH; R_2, X_2 (3.2 km)→0.0947 Ω, 3.34 mH; R_3, X_3 (2 km) →0.0592 Ω, 2.08 mH
	Load parameters
DC lamp load	$P_{L,dc}$→50 kW; 450 V
DC motor load	$P_{L2,dc}$→20 kW, 450 V
PV (DER1) local load (load 1)	P_{L1}→100 kW; Q_{L1}→5 kVAR
grid-side non-linear load (load 2)	$P_{L2,0}$→275 kW; $Q_{L2,0}$→25 kVAR
diesel generator (DG2) parameters	$V_{dg2,rated}$→480 V; DG rated revolution 750 rpm
DG2 governor control gains	$K_{1,dg2}$→1.85; $K_{1,dg2}$→2.6; $K_{1,dg2}$→0.85

2 Multiple PV-based utility interactive DC microgrid

An MTDC network incorporated with multiple-shunt-connected PV systems (PV with DC–DC converters), diesel generator (with AC–DC rectifier unit), various DC loads and AC utility interfacing VSC unit is proposed for present microgrid configuration as shown in Fig. 1. VSC is integrated with high-frequency pulse-width modulation (i.e. 10 kHz) switching with grid phase locked loop (PLL) control. Thus, an intermittent fault tolerance is exhibited by the VSC unit by limiting current surges during DC bus faults. Similar high-frequency duty cycle (d) calculation of DC–DC units contributes to their intermittent fault tolerance. The parameters considered for the proposed utility integrated MTDC system are mentioned in Table 1.

DC cables are generally resistive in nature during steady-state power flow solution. However, during sudden fault at any DC cable a transient nature of cable is expressed in terms of series inductive reactance (x_L) and shunt capacitive reactance (x). This shunt capacitive reactance (x) is important during PG fault calculation, especially during high reactance path of DC arc fault. The DC cable parameters considered for present discussion (Fig. 2) are shown in Table 2. This multiple DGs based DC distribution network is designed with proper unit protection by fast-acting DC semiconductor-based switches. The differential current characteristic is explained for DC cables in Section 3.

3 Proposed differential current-based fault detection

A DC network with fast-response DC switches at both sides of unit protection zone and AC circuit breakers at AC side of DGs (i.e. for diesel generator-based DG and AC coupling VSC) is implemented as shown in Fig. 2. The protection switching will be based on measured differential current during fault and present fault

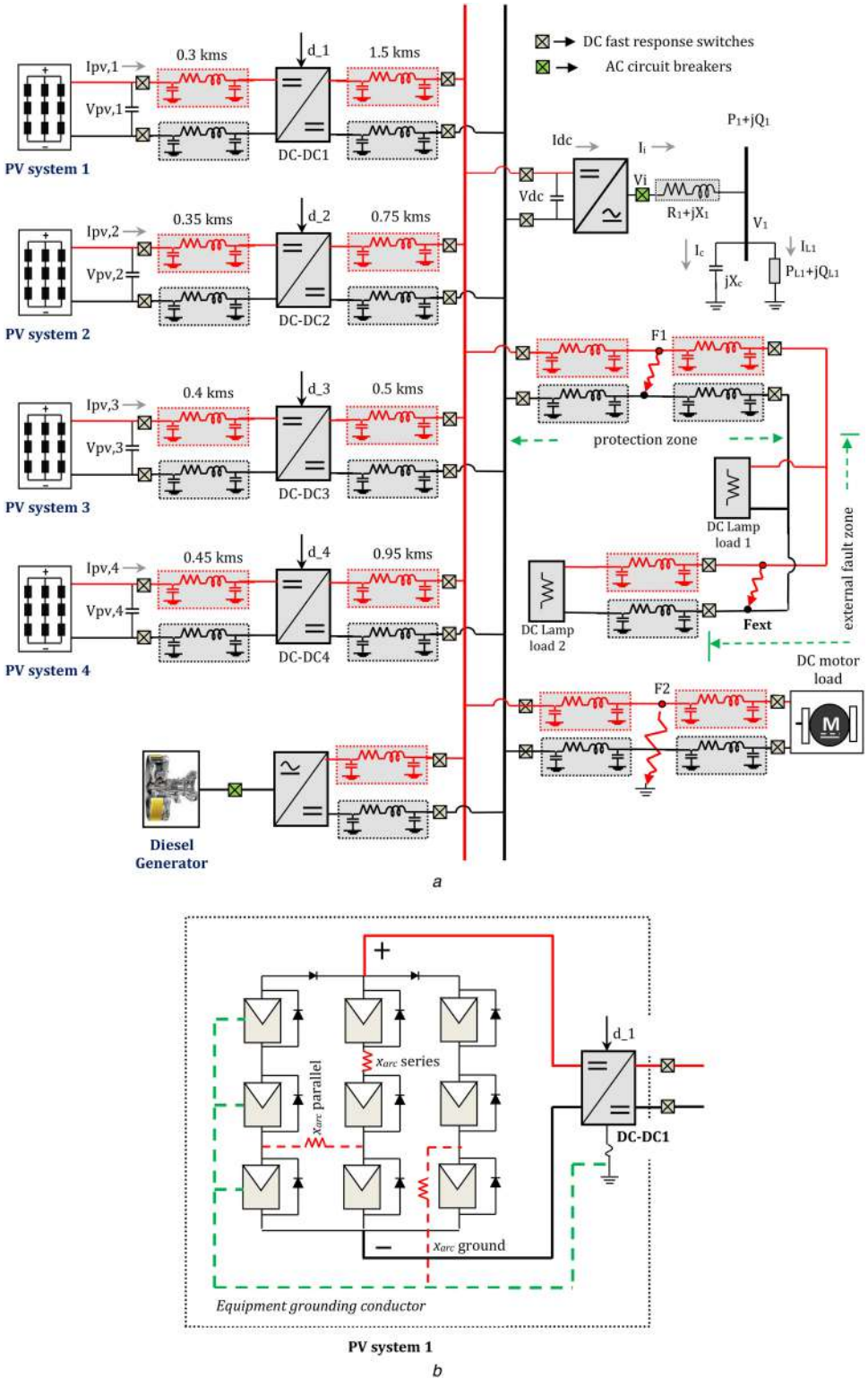

Fig. 2 *DC cable parameters*

(a) Detailed unit protection zones based schematic representation of the proposed multi-PV DC microgrid, ***(b)*** Different types of arc fault configuration for PV system

detection threshold. To understand the scheme, first a detailed mathematical derivation of differential current for a DC cable unit is presented below.

Single DC cable (π model based) is implemented for the proposed network and shown in Fig. 2. The cable parameters are mentioned in Table 2. Points $F1$ and $F2$ are considered for fault location (protection zone) to validate the proposed scheme, where non-detection of external fault is evidenced at point F_{ext}. Validation of external fault non-detection is discussed in Section 5. For present consideration if F1 is the fault location and the DC cable equivalent circuit representation will be as shown in Fig. 3*a*.

In Fig. 3*a*, $V_{dc1}(t)$→input side DC voltage, $I_{dc1}(t)$→input DC current, $V_{dc2}(t)$→output/load side DC voltage and $I_{dc2}(t)$→output/load side DC current. R_1, L_1, R_2, L_2 are the series equivalent resistance, inductance of the cable where C_1 and R_f are the shunt capacitance (coupling point) and fault resistance, respectively. R_f is considered negligible for PP fault calculation; however, for PG it is countable to calculate accurate fault location. Now from Fig. 3, it is possible to apply Kirchhoff's voltage law to obtain the following relationship:

Table 2 DC cable parameters for the proposed utility interactive MTDC network

Component	Data	Parameters		
		Resistive	Inductive	Capacitive
rectifier cable (diesel generator)	1.4 kms	0.125 Ω/km	0.34 mH/km	0.5 μF/km
PV cables	1.8 kms, 1.1 kms, 0.9 kms, 1.4 kms	0.641 Ω/km	0.34 mH/km	0.1 μF/km
DC load cables	3 kms	0.641 Ω/km	0.34 mH/km	0.1 μF/km

$$V_{dc1} - I_{dc1}R_1 - L_1\left(\frac{dI_{dc1}}{dt}\right) - \frac{1}{C}\int i_c\,dt = 0 \tag{1}$$

Here, i_c is instantaneous current across shunt capacitor. As shunt capacitor is combined with fault resistance in a parallel manner a current division scheme is considered for expressing (1) in terms of differential current $[I_{dc3}(t)]$

$$\begin{aligned} &V_{dc1} - I_{dc1}R_1 - L_1\left(\frac{dI_{dc1}}{dt}\right) - \left(\frac{R_f}{C(R_f + x_c)}\right)\int I_{dc3}\,dt = 0 \\ &\text{or } V_{dc1} - I_{dc1}R_1 - L_1\left(\frac{dI_{dc1}}{dt}\right) - \left(\frac{x}{C}\right)\int I_{dc3}\,dt = 0 \end{aligned} \tag{2}$$

In the above expression, x_c is the instantaneous reactance (during fault transient) of shunt capacitor, C_1. This reactance does not have any impact during normal operation where $I_{dc3}(t) = I_{dc1}(t) - I_{dc2}(t)$, is negligible. The expression in (2) is in continuous state transition form. If considered sample time interval is Δt, then $V_{dc1}(t)$ in (2) can be approximated by using a piecewise function as

$$V_{dc1}(k\cdot\Delta t) = \frac{1}{2}[V_{dc1}(k\cdot\Delta t) + V_{dc1}(k\cdot\Delta t + \Delta t)] \cong V_{dc1}(t) \tag{3}$$

where $k\Delta t \le t < (k+1)\Delta t$ and $k = 1, 2, 3, \ldots$ positive integers. Here, $V_{dc1}(k\Delta t)$ is a rectangular wave which is obtained from sampling and polygonal holding of $V_{dc1}(t)$. Now, by replacing all continuous state parameters in discrete representation with a similar approximation, (2) can be rewritten as in (4). The sampling frequency is considered as 2 kHz, and the kth sample instance is expressed the second-order differential system as

$$\begin{aligned} &R_1 I_{dc1}(k\Delta t) + L_1\left[\frac{I_{dc1}(k+1) - I_{dc1}(k)}{\Delta t}\right] \\ &+\frac{x}{C}[I_{dc3}(k+1) + I_{dc3}(k)]\Delta t = V_{dc1}(k\Delta t) \end{aligned} \tag{4}$$

where x is the coefficient of differential current in terms of shunt capacitance, fault resistance and instantaneous reactance and Δt represents the sampling time interval. This transient reactance coefficient (x) is important while considering DC arc faults. The DC cables are resistive one and from the resistive nature the fault distance can be calculated by Moore–Penrose pseudo-inverse where the fault detection is accomplished by a modified cumulative sum (CuSum) method.

3.1 DC arc fault model for PV system

A DC arc series fault meta-model [13] is achieved for the proposed PV system 1, as in Fig. 2*b*, by including Mayr reactance (x_{mayr}) and corona reactance (x_{cor}). The arc reactance ($x_{arc} = x_{mayr} + x_{cor}$) path is having two parallel current diodes with low threshold current (I_s). I_s represents the transition between the corona and arc discharge and it may vary as: $-I_{s,nom} \le I_s \le I_{s,nom}$, according to arc potential (V_{arc}) polarity. V_{arc} is considered in series with current diodes and obtained from Ayrton model

$$V_{arc} = \frac{P_{nom}}{I_{arc}} + V_{nom} \tag{5}$$

Here, P_{nom} and V_{nom} are cooling power and arc potential constant. The DC arc path is depicted in Fig. 3*d*. The potential difference at fault point F1 is obtained from DC arc path, as

$$V_{dc3} = I_{arc} \times x_{arc} - V_{arc} \tag{6}$$

The arc fault reactance (x_{arc}) is calculated as

$$\begin{aligned} x_{arc}(k) &= x_{cor}(k) + x_{mayr}(k) \\ &= x_{cor}(k) + \int \frac{x_{arc}(k-1)}{\Theta}\left(1 - \frac{P_{in}}{P_{nom}}\right) \end{aligned} \tag{7}$$

where Θ is the arc time constant (delay) and P_{in} is the supplied power to arc path. The energy (W_{arc}) stored in arc path during fault is obtained as

$$\frac{\partial W_{arc}}{\partial t} = P_{in} - P_{nom} \tag{8}$$

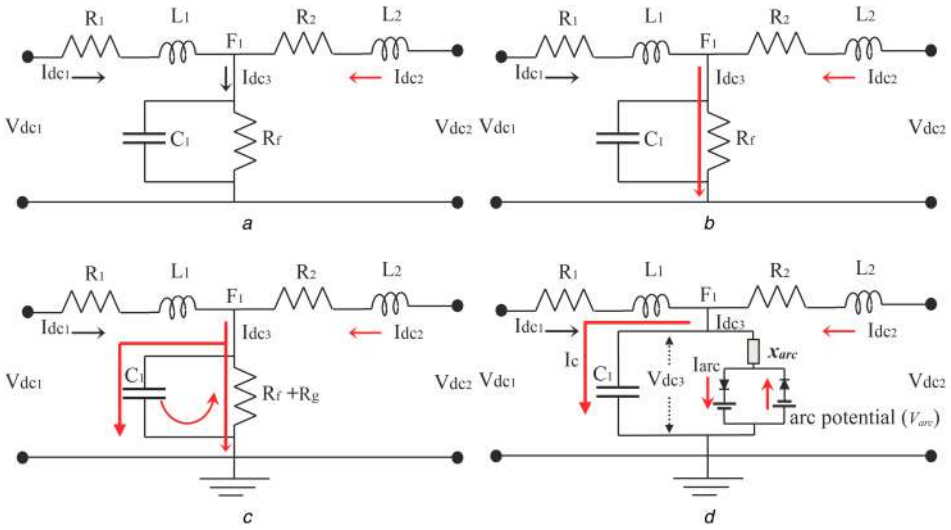

Fig. 3 *Equivalent circuit representation of*
(a) DC cable unit zone, ***(b)*** During PP fault, ***(c)*** During PG fault, ***(d)*** During DC arc fault

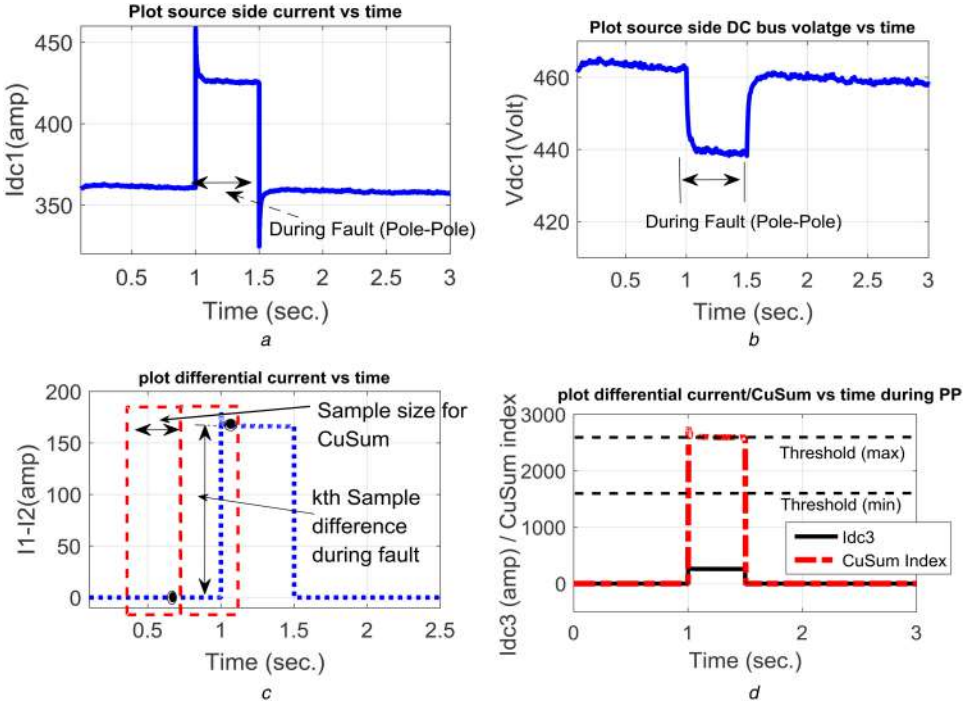

Fig. 4 *Proposed fault detection by modified CuSum for PP fault*
(a) Input side (I_{dc1}) current, ***(b)*** Input side voltage (V_{dc1}), ***(c)*** Differential current (I_{dc3}), ***(d)*** High index of CuSum during PP fault

Now, the conventional DC cable fault path (PP and PG fault) consideration in (2) is represented with arc fault as

$$V_{dc1}(t) + R_1 I_{dc1}(t) + L_1 \frac{dI_{dc1}(t)}{dt} + x_2 I_{dc3}(t) - \text{sign}(V_{arc}) \times \| V_{arc} \| \quad (9)$$

where $x_2 = [x_c/(x_c + x_{arc})]$ is the arc path reactance. Again by considering piecewise approximation [as in (3)] to convert continuous time-frame to discrete form as

$$R_1 \times I_{dc1}(k\Delta t) + L_1\left(\frac{I_{dc1}(k) - I_{dc1}(k-1)}{\Delta t}\right) + x_2 \times I_{dc3}(k\Delta t) = V_{dc1}(k\Delta t) - \| V_{arc}(k\Delta t) \| \times \text{sign}[V_{arc}(k\Delta t)] \quad (10)$$

Now (4) and (10) are two obtained discrete differential solutions considered for the proposed protection scheme and selection among these is a decision function of CuSum [14] threshold. The fault detection based on modified CuSum is presented in Section 3.2.

3.2 Modified CuSum average-based fault classification

During fault condition the cable voltage and current change significantly. For an effective fault detection scheme these changes should get identified online with minimum detection samples/time. CuSum-based average calculation can be achievable by: (a) *sample-by-sample approach*: in this approach differential current (I_{dc3}) samples (k) are compared with the previous sample ($k-1$) value to throw a higher index during sudden changes. Index higher than detection threshold will count as CuSum detection time (C_d); (b) *window-by-window concept*: for the proposed DC microgrid, a chunk of samples (i.e. n number sample in a chunk) is considered as window for CuSum-based fault detection. Now, the kth sample of the lth window and the kth sample of $(l+1)$th window is compared and if for consecutive three comparisons it throws higher index than detection threshold then a trip signal will follow to fast DC switches, to disconnect both sides of that unit protection zone, as in Fig. 2. The sliding of window can be through overlapped sliding (where window sample size n is higher than sliding sample size m) or separate sliding (where window sample size n is lesser than sliding sample size m). In the proposed detection scheme separate sliding window is proposed as in Figs. 4*c*, 5*a* and *b*.

During PP fault the DC cable differential current flows through the R_f low resistance path as capacitive reactance (x) is higher during this transient as shown in Fig. 3*b*. Thus, current $I_{dc3}(t)$ displays a DC positive transient when voltage $V_{dc1}(t)$ shows a dip in nature, as in Figs. 4*b* and *c*. During PG fault path the ground resistance makes R_f path more resistive and hence capacitive discharge takes place through ground resistance (R_g) and R_f as shown in Fig. 3*c*. Thus, $V_{dc1}(t)$ depicts a swell in nature when $I_{dc1}(t)$ shows negative polarity transient, as in Fig. 5*a*. For PV-side DC arc fault (ground), the fault differential current is as shown in Fig. 5*b*. The series arc is similar to ground arc, where fault path has high arc potential instead of high resistance. Thus, the detection threshold of CuSum index is quite low to distinguish these types of faults, as in Fig. 5*d*. The series, ground arc faults are due to failure of intended continuity of DC cable; moreover, parallel arc faults resulted through unintentional current path between two PV systems (i.e. arrays or modules). DC parallel arc fault energy can be very high, where series, ground arc fault current can be negligible to distinguish. The proposed technique is able to detect ground arc (Section 5.3), series arc (Section 5.5), where parallel arc (considered to show the protection limit in the proposed arc detection) should be operated by AFCI device or method in [15].

The modified CuSum-based fault detection for DC network unit protection is proposed as in (11)

$$\text{CuSum}(k) = \text{CuSum}(k-1) + I_{dc3}(k) - I_{dc3}(k - \eta N_s) \quad (11)$$

where k is the sample instant, η is the positive integer value (generally considered as unity), N_s is number of samples considered for each window chunk. Now, the CuSum detection time (C_d) is calculated from threshold crossover by high index of CuSum as in (12)

$$\begin{aligned} &\text{if CuSum}(k) > \text{CuSum\_thrshld} \\ &\text{trip\_flag} == 1; \\ &C_d = (\text{CuSum}(k) - \text{CuSum}(j)) \times T_t \end{aligned} \quad (12)$$

Here, the kth instant the index crosses detection threshold, j is the sample instance when *CuSum index* becomes >0, T_t is the sampling

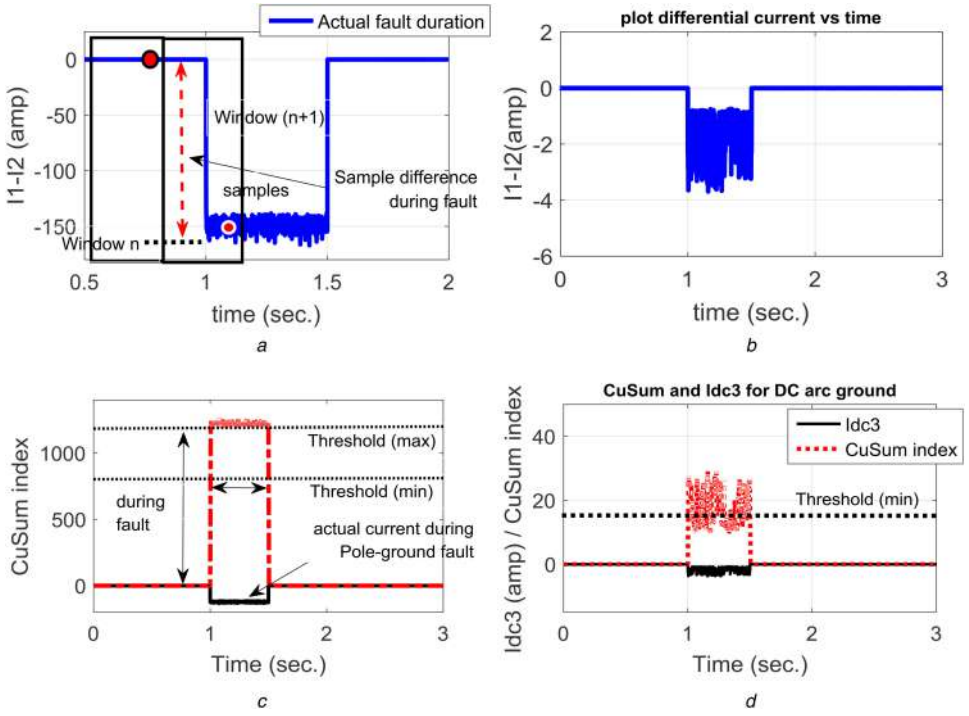

Fig. 5 *Proposed fault detection by modified CuSum for PG and DC arc GFs*

(a) Differential current (I_{dc3}) for PP fault, ***(b)*** Differential current (I_{dc3}) for ground arc fault, ***(c)*** High index of CuSum during PG fault, ***(d)*** CuSum index during ground arc fault

time interval. So finally, trip time (Ts) is: $Ts = C_d +$ DC switching delay [16].

The proposed modified CuSum-based fault detection scheme is incorporated with selectivity between internal (within DC protection zone, Fig. 2*a*) and external faults. As DC measurement units are considered at both ends of the proposed protection zone, the CuSum index for differential current (I_{dc3}) response will be higher than the CuSum index for average current ($I_{dc,avg}$) response for internal faults. For external faults, the relationship between I_{dc3} and $I_{dc,avg}$ will be vice versa. This effectiveness in selectivity for the proposed CuSum is discussed further in Section 5. The average current is calculated as

$$I_{dc,\,avg}(k\Delta t) = \frac{(I_{dc1}(k\Delta t) + I_{dc2}(k\Delta t))}{2} \tag{13}$$

CuSum index for average current ($I_{dc,avg}$) can be calculated with a similar approach as in (11).

For DC arc, due to high-resistive path (ground) and arc potential (series) as in Fig. 3*d*, the differential fault current shows very low detection peak as shown in Figs. 5*b* and 11*a*. During PV series arc fault transient instance, if arc potential is higher than the V_{dc1}, the flow of I_{dc3} might get reverse path, which will lead to complexity in fault detection. The CuSum index during this fault is significantly less and thus easy to design in fault classification algorithm. Moreover, to implement CuSum detection in a computational platform, power amplifier is needed to reduce the actual fault current magnitude to a very low-level suitable for electronic instrumentation. Thus, based on only fault current magnitude, series arc fault detection might become erroneous. Thus to avoid this, the fault classification is done by binary tree (BT) classifier by investigating polarity of fault current (y_1) and CuSum threshold (y_2) as shown in (14)

$$\begin{aligned}
&\text{if } y_1 == +ve \\
&\text{if } y_2 > 340 \,\&\, y_2 < 2800 \\
&\quad \text{Dscn_flg} == 1; \\
&\text{else if } y_2 > 750 \,\&\, y_2 < 1490 \\
&\quad \text{Dscn_}f\,\text{lg} == 2; \text{end} \\
&\text{else if } y_2 > 15 \& y_2 < 140 \\
&\quad \text{Dscn_}f\,\text{lg} == 3; \text{ end} \\
&\text{end} \\
&\text{end}
\end{aligned} \tag{14}$$

The decision flag (Dscn_flg) is 1 for PP fault, 2 for PG and 3 for PV-side DC arc fault (PV cable). The threshold values are estimated for full PV irradiation level (1000 W/m^2). The fast-response DC switch trips while index value reaches detection threshold.

To achieve effective protection through fast DC switching opening and reclosing with minimum potential error (i.e. synchronisation problem), an effective communication measure is required. The proposed unit protection requires measured DC voltage (V_{dc1}, V_{dc2}) and current (I_{dc1}, I_{dc2}) samples from both sides of protection zone to be communicated to the protective relay. Owing to lack of standard, to support futuristic fast relaying operation (international electrochemical commission (IEC)-61850), open standard with plug and play integration approach is needed to be considered. Here, the DC switching delay is considered where communication delay is neglected. For the proposed system, 2000 samples are collected each second from all measured quantities. According to IEC-61850 standard (up to 64,000 bits/s), this sampling rate with minimum of 16 bit channel will be sufficiently fast for the proposed protection. This work will incorporate with detailed communication standard study in future scope.

3.3 Adaptive detection threshold calculation

During utility grid-connected mode of steady-state operation is directly compensated the AC/DC local loads. However, during faults, the threshold limits (i.e. maximum and minimum) are varied according to the PV penetration level. Initial PV (rated) contribution will remain for standard test condition (1000 W/m^2,

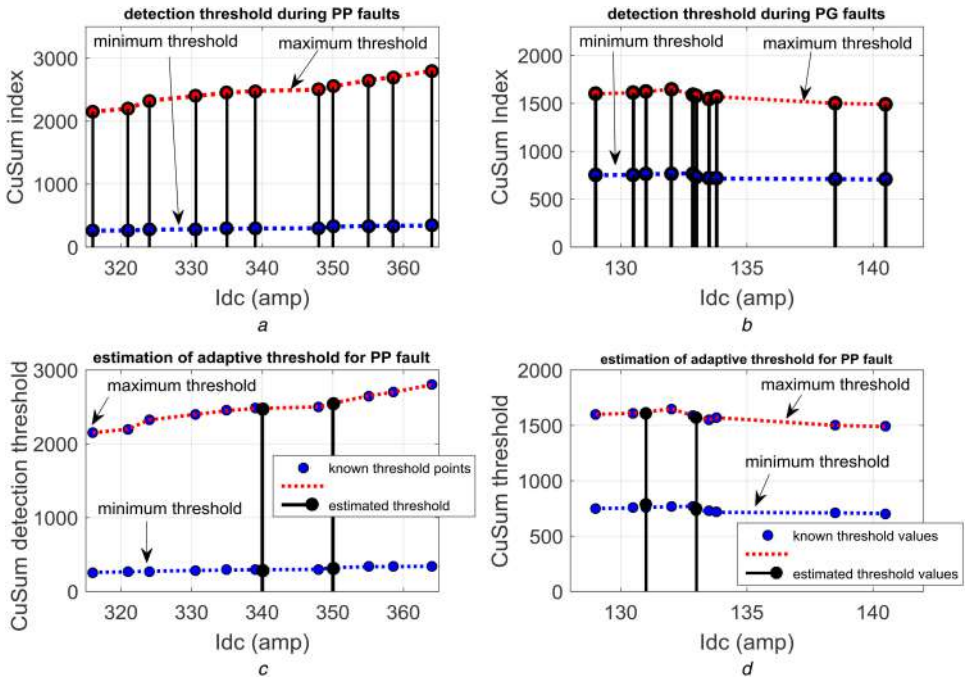

Fig. 6 *Adaptive threshold calculation for utility interactive DC microgrid protection*
(a) Threshold variation during PP faults, ***(b)*** Threshold variation during PG faults, ***(c)*** Threshold detection during PP faults, ***(d)*** Threshold detection during PG faults

Table 3 CuSum detection threshold variation during PP faults

G1	G2	G3	G4	I_{dc}, amp	CuSum index (maximum)	CuSum index (minimum)
100	100	100	100	316	2150	260
175	200	225	250	320.95	2200	265
250	275	300	325	324	2325	275
350	375	400	425	330.6	2400	285
400	450	500	525	335	2450	290
475	545	590	600	339	2480	295
560	640	680	700	348	2500	300
600	750	800	850	350	2550	325
775	850	900	950	355	2650	335
900	950	1000	875	358.5	2700	338
1000	1000	1000	1000	364	2800	340

Table 4 CuSum detection threshold variation during PG faults

G1	G2	G3	G4	I_{dc}, amp	CuSum index (maximum)	CuSum index (minimum)
100	100	100	100	129	1600	750
175	200	225	250	130.5	1610	754
250	275	300	325	131	1620	760
350	375	400	425	132	1650	765
400	450	500	525	132.85	1590	770
475	545	590	600	133	1580	730
560	640	680	700	133.5	1550	725
600	750	800	850	133.8	1570	715
775	850	900	950	138.5	1500	710
850	950	900	950	140	1498	708
1000	1000	1000	1000	142.5	1490	705

25°C) and inconsistency of solar irradiation throughout the day will contribute to the maximum and minimum detection thresholds (i.e. differential over current during faults, I_{dc3}). As the direct reflection of PV generation variation can be noted from common DC bus current (I_{dc}), it is considered for determining the threshold limit in an adaptive manner, for the proposed multiple PV-based system. In Tables 3 and 4, the threshold changes are recorded for PP and PG faults, respectively, when PV irradiation is altered from maximum (1000 W/m^2) to minimum (100 W/m^2). Similar study is conducted for PV-side DC arc faults. From Tables 3 and 4, maximum and minimum thresholds are drawn for both faults, as shown in Figs. 6*a* and *b*, respectively. Fault resistance (R_f) is subjected to a change of 0.5–2 Ω for PP and PG faults where the arc fault reactance (x_{arc}) deviation is considered 5–30 Ω, calculated according to arc energy [(7) and (8)].

To calculate detection threshold dynamically during variation in solar irradiation, a PCHP interpolation scheme is adopted. PV generation variation is reflected through I_{dc} and by varying PV irradiation for four parallel PV systems, in Fig. 2, the maximum and minimum threshold values are obtained from PCHP

interpolation [12] technique, where two 11th-order (as in Table 3) system of linear equation are expressed for CuSum detection threshold as functions of DC current (I_{dc}). In a cubic hermite interpolation each piece is expanded as third degree polynomial in hermite form, where resulting spline is continuous with first derivative and can be expressed for given interval (z_k, z_{k+1}) as in (15)

$$\begin{aligned} F(z) = {} & h_{00}(m)F_{z,k} + h_{10}(m)(z_{k+1} - z_k)t_k \\ & + h_{01}(m)F_{z,k+1} + h_{11}(m)(z_{k+1} - z_k)t_{k+1} \end{aligned} \tag{15}$$

where $m = ((z - z_k)/z_{k+1} - z_k)$; moreover, h is the hermite basis functions; t_k is the starting tangent and t_{k+1} is the ending tangent. Thus, the polynomial coefficients are obtained as a simultaneous solution from the system of polynomial equations.

For the proposed scheme, dynamically calculated threshold parameters are depicted in Figs. 6*c* and *d*. The proposed adaptive detection of CuSum index is estimated accurately by the piecewise cubic hermite polynomial (PCHP) algorithm. After effective detection of DC faults for the proposed network, the distance of fault occurrence is also estimated from same differential current-based protection scheme as discussed in Section 4.

4 New fast fault distance estimation

As shown in Fig. 2, the differential current measured from both sides of the fault point (F1) is used to obtain fault distance through a non-iterative adaptive Moore–Penrose pseudo-inverse solution. The differential equations expressed in (4) and (10) are considered for the fault location in the proposed DC microgrid. For PP and PG faults (4) and for PV-side arc fault and (10) are used for distance calculation, based on decision flag (Dscn_flg). The differential current-based second-order system in (4) derived from DC cable equivalent resistor-inductor-capacitor (RLC) network in Section 3 can be rewritten as matrix formation in terms of n number of measured samples [i.e. $V_{dc1}(k\Delta t)$, $V_{dc2}(k\Delta t)$, $I_{dc1}(k\Delta t)$ and $I_{dc2}(k\Delta t)$]

$$\begin{bmatrix} I_{dc1}(k) & I_{dc1}(k) - I_{dc1}(k-1) & I_{dc3}(k) + I_{dc1}(k+1) \\ I_{dc1}(k+1) & I_{dc1}(k+1) - I_{dc1}(k) & I_{dc3}(k+1) + I_{dc1}(k+2) \\ \vdots & \vdots & \vdots \\ I_{dc1}(n) & I_{dc1}(n) - I_{dc1}(n-1) & I_{dc3}(n) + I_{dc1}(n+1) \end{bmatrix} \begin{bmatrix} R_1\Delta t \\ \dfrac{L_1}{\Delta t} \\ \dfrac{x}{C_1\Delta t} \end{bmatrix} = \begin{bmatrix} V_{dc1}(k\Delta t) \\ V_{dc1}((k+1)\Delta t) \\ \vdots \\ V_{dc1}(n\Delta t) \end{bmatrix} \tag{16}$$

For PV arc fault, (10) can be expressed similarly with n number of sample values

$$\begin{bmatrix} I_{dc1}(k) & I_{dc1}(k) - I_{dc1}(k-1) & I_{dc3}(k) \\ I_{dc1}(k+1) & I_{dc1}(k+1) - I_{dc1}(k) & I_{dc3}(k+1) \\ \vdots & \vdots & \vdots \\ I_{dc1}(n) & I_{dc1}(n) - I_{dc1}(n-1) & I_{dc3}(n) \end{bmatrix} \begin{bmatrix} R_1\Delta t \\ \dfrac{L_1}{\Delta t} \\ x_2\Delta t \end{bmatrix} = \begin{bmatrix} V_{dc1}(k\Delta t) - V_{arc}(k\Delta t) \times \text{sign}(V_{arc}(k\Delta t)) \\ V_{dc1}((k+1)\Delta t) - V_{arc}((k+1)\Delta t) \times \text{sign}(V_{arc}((k+1)\Delta t)) \\ \vdots \\ V_{dc1}(n\Delta t) - V_{arc}(n\Delta t) \times \text{sign}(V_{arc}(n\Delta t)) \end{bmatrix} \tag{17}$$

From the above expression, Moore–Penrose pseudo-inverse scheme is implemented to estimate unknown R_1 and L_1 values. For this consideration, input current matrix is $\boldsymbol{I}_{DC} \in \boldsymbol{R}^{n\times 3}$, unknown cable parameters vector is $\boldsymbol{Z}_{DC} \in \boldsymbol{R}^{3\times 1}$ and input DC voltage vector is $\boldsymbol{V}_{DC} \in \boldsymbol{R}^{n\times 1}$. Thus, (16) and (17) can be represented as

$$[\boldsymbol{I}_{DC}] \times [\boldsymbol{Z}_{DC}] = [\boldsymbol{V}_{DC}] \tag{18}$$

To obtain $\boldsymbol{Z}_{DC}$ from the above (18), a Moore–Penrose pseudo-inverse, $[I^{+}_{DC}]$ is implemented as

$$[\boldsymbol{Z}_{DC}] = [\boldsymbol{V}_{DC}][\boldsymbol{I}_{DC}]^{+} \tag{19}$$

The available data samples are assumed to be M and n number of samples, used for each set (chunk) of this incremental learning of unknown cable parameters. Minimum learning sequence with adaptive updating of $\boldsymbol{Z}_{DC}$ is effective for accurate calculation of fault location. For Moore–Penrose approach, pseudo-inverse $[I^{+}_{DC}]$ is calculated from given n number of data chunk as

$$I^{+}_{DC}(n) = I^{T}_{DC}(n)\left(\tau \boldsymbol{I} + I_{DC}(n) \times I^{T}_{DC}(n)\right)^{-1} = I^{T}_{DC}(n) \times M \tag{20}$$

where I^{T} is the conjugate transpose of $\boldsymbol{I}_{DC}$, $\boldsymbol{I}$ is the identity matrix and τ is the coefficient with small value. This approach will calculate the actual value of line resistance during fault (R_1). Initial chunk might have some noisy data and calculation error might be more. To reduce this error, adaptive $\boldsymbol{Z}_{DC}$ is obtained from simultaneous chunks of another n samples from total M number of samples. The calculated R_1 is obtained effectively within 2–5 simultaneous chunks for the proposed DC microgrid-based fault distance calculation. For this chunk-by-chunk approach, pseudo-inverse M is calculated for the kth chunk as

$$\begin{aligned} M(k+1) = {} & M(k) - M(k)I^{T}_{DC}(k+1)[\mathbf{I} + \boldsymbol{I}_{DC}(k+1) \\ & \times M(k)I^{T}_{DC}(k+1)]^{-1}\boldsymbol{I}_{DC}(k+1)M(k) \end{aligned} \tag{21}$$

Now, the unknown cable parameters are updated adaptively as described in (22)

$$\begin{aligned} \boldsymbol{Z}_{DC}(k+1) = {} & \boldsymbol{Z}_{DC}(k) + M(k+1)I^{T}_{DC}(k+1) \\ & \times [\boldsymbol{V}_{DC}(k+1) - (\boldsymbol{I}_{DC}(k+1)\boldsymbol{Z}_{DC}(k))] \end{aligned} \tag{22}$$

where k is the number of chunks. Now, fault distance is calculated from measured R_1 and unit resistance of cable (R_{cable}/km). As in Fig. 3, it is clear that the DC cable fault path is parallel to shunt cable capacitance (C_1) which provides transient snubber reactive path. This reactance will be minimum during PP fault, but during PG fault the reactance approach could give the cable distance resistance (R_1) value erroneously. In result discussion section, Tables 5 and 6 provide similar conclusion. Fig. 7 represents the fault detection parameters by the proposed method, where Fig. 7*a* shows the trip time (*Ts*) and actual fault duration, Figs. 7*b–d* depict the various parameters considered within trip time to calculate distance.

Normally, high-frequency switching is adopted for converter application, where different nodes of it can generate high-amplitude switching noise (i.e. few hundred kHz to few MHz) [10, 17]. This high range of noise can contribute to a false detection, sympathetic tripping etc. for conventional fault detection; especially, during low-fault current magnitudes (DC arc faults). The proposed detection method is performed successfully during the effect of this noise, and is discussed in Section 5.5.2. However, the effect is visible for distance calculation error, which is increased for the proposed technique during noisy channel operation. The solution to it is increased number of samples (M), which leads to a higher *Ts* value. This problem will be focused in future scope of this paper.

Table 5 Percentage error in fault location calculation for PP fault

Fault distance, kms	Fault resistance, Ω			
	0.5	1	1.5	2
	ε, %	ε, %	ε, %	ε, %
0.5	0.320	1.081	3.206	5.980
0.75	0.326	1.702	3.387	4.388
1	0.201	0.635	1.646	3.238
1.25	0.198	0.725	1.640	2.825
1.5	0.310	0.601	1.486	2.706
1.75	0.091	0.864	1.363	2.363
2	0.090	0.732	1.360	2.360
2.25	0.086	0.642	1.286	2.219
2.5	0.076	0.555	1.238	2.140
2.75	0.064	0.418	1.224	1.923
3	0.262	0.360	1.182	1.826

Table 6 Percentage error in fault location calculation for PG fault

Fault distance, kms	Fault resistance, Ω			
	0.5	1	1.5	2.0
	ε, %	ε, %	ε, %	ε, %
0.5	0.486	1.181	3.306	6.242
1	0.401	0.835	2.424	5.380
1.5	0.368	0.748	2.210	4.862
2	0.321	0.736	1.894	4.121
2.5	0.312	0.595	1.468	3.452
3	0.284	0.410	1.210	2.424

5 Result analysis

To evaluate the effectiveness of the proposed unit protection scheme by reducing the fault trip time (Ts) and improving accuracy, a multiple DGs based AC utility integrated low-voltage DC distribution network with different DC loads (Table 1: DC lamp load, DC motor load) is simulated in MATLAB environment. Various possible fault conditions (case 1: PP; case 2: PG and case 3: DC ground arc fault) are implemented in Section 5.1−5.3 to validate the proposed protection scheme. Detection of DC series arc fault and effectiveness of circuit breakers during noise are presented in Section 5.5.

5.1 Case 1: PP fault analysis for DC motor load

DC motor load is highly preferable during PV-based pumping system applications. This DC load is effective for rural/ suburban DC distribution network and hence considered for this case study as mentioned in Table 1. The motor load cable distance is considered as 3 km, where fault location F2 is varied from 0.5 to 3 km, to check the effectiveness of the proposed scheme. The fault resistance (R_f) is considered to be varied from 0.5 to 2 Ω for present focus. The fault is created at instance $t = 1$ to 1.5 s.

Various parametric variations are given in Fig. 8. The trip time is obtained as 65 ms, as evidenced the fastness of the proposed protection irrespective of loading condition. As in Fig. 8*b*, the PP fault occurred inside the protection zone and thus CuSum(I_{dc3}) > CuSum($\boldsymbol{I}_{dc,avg}$) for this internal fault. Selectivity of the proposed CuSum is evidenced in Figs. 8*c* and *d*, for external PP fault at point $\boldsymbol{F}_{ext}$, Fig. 2*a*, where CuSum (I_{dc3}) < CuSum ($I_{dc,avg}$). The proposed detection scheme successfully segregates the protection zones.

5.2 Case 2: PG fault analysis for DC lamp load

The considered lamp load parameters are mentioned in Table 1, where DC cable connecting the load to common DC bus is mentioned in Table 2. At time $t = 1$ to 1.5 s, PG fault is subjected at F1 for DC lighting load. The variation of fault resistance, R_f and distance (i.e. 0.5–2 Ω and 0.5–3 km, respectively) is considered for this case and the result verification is depicted in Fig. 9. From Fig. 9*a* the trip time is obtained as 48 ms. Similar selectivity study of CuSum index is shown in Figs. 9*b–d* where for internal PG fault CuSum(I_{dc3}) > CuSum($I_{dc,avg}$), but for external fault at point $\boldsymbol{F}_{ext}$, CuSum(I_{dc3}) < CuSum($I_{dc,avg}$). The proposed protection is effective from error detection.

5.3 Case 3: DC ground arc fault for PV system

DC ground arc faults are very difficult to measure due to their low detection threshold. The series and ground arc are almost similar due to low-fault current level through high-resistive (ground), high arc potential (series) paths. DC arc reactance (x_{arc}) is considered as

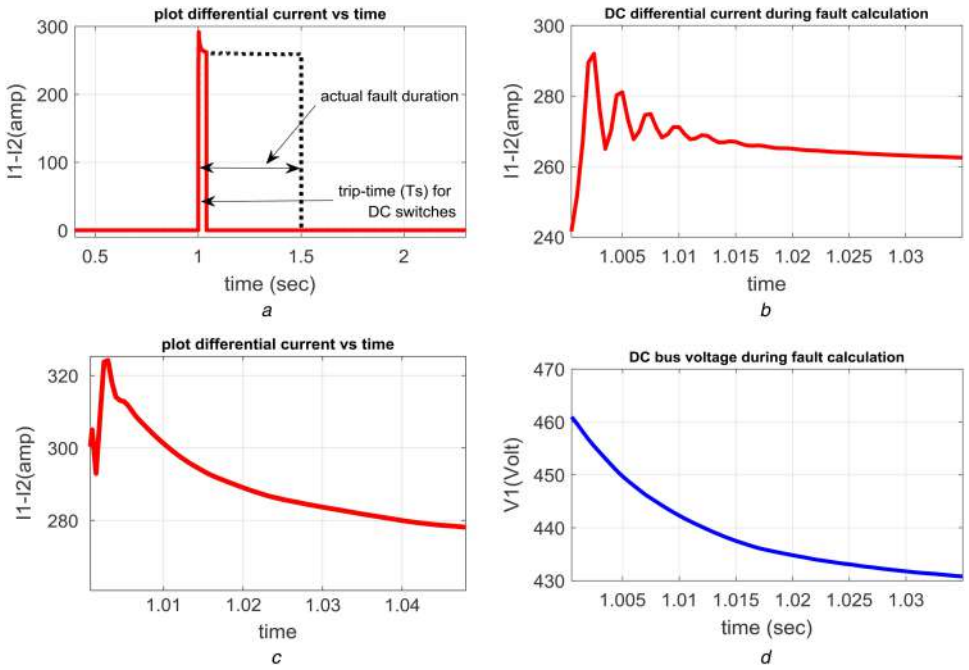

Fig. 7 *Differential current-based fault distance measurement*

(a) Actual fault duration and fault duration to calculate distance, ***(b)*** Fault current considered for distance measurement for DC lamp load, ***(c)*** Fault current considered for distance measurement for DC motor load, ***(d)*** DC voltage (V_{dc}) during fault

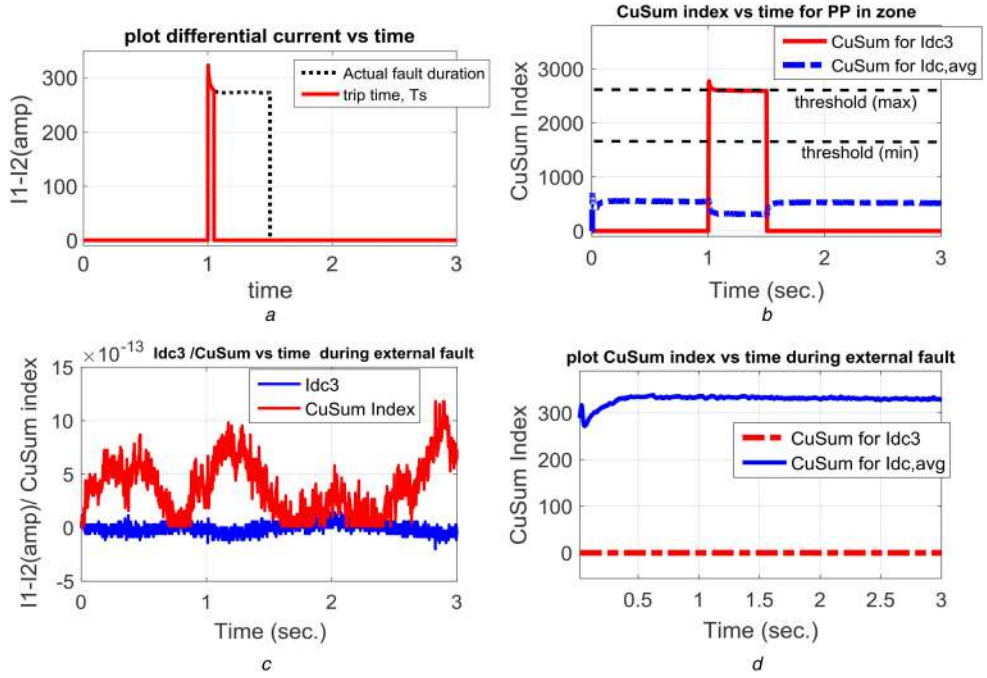

Fig. 8 *Effective fault protection during PP fault to the DC motor load*

(a) Trip time (*Ts*) of DC switches with fault current (I_{dc3}), ***(b)*** CuSum index for I_{dc3} and $I_{dc,avg}$ for internal fault, ***(c)*** Differential current (I_{dc3}) and CuSum of I_{dc3} for external fault, ***(d)*** CuSum(I_{dc3}) < CuSum ($I_{dc,avg}$) for external fault

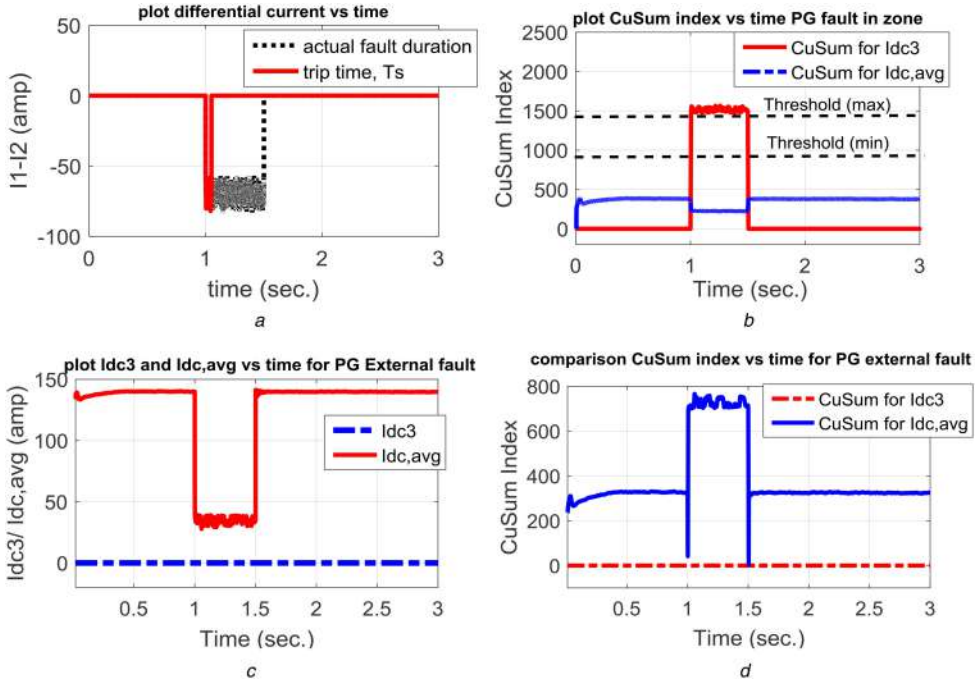

Fig. 9 *Variation of DC network parameters during PG fault for DC lighting load*

(a) Trip time (*Ts*) of DC switches with fault current (I_{dc3}), ***(b)*** CuSum index for I_{dc3} and $I_{dc,avg}$ for internal fault, ***(c)*** Differential current (I_{dc3}) and average current ($I_{dc,avg}$) for external fault, ***(d)*** CuSum(I_{dc3}) < CuSum ($I_{dc,avg}$) for external fault

20 Ω where arc potential is considered 10% of V_{dc1} during fault. DC current and various voltage parameters are shown in Fig. 10. The trip time is obtained as 96 ms and is shown in Fig. 10*a*.

For DC ground arc, the proposed protection is effective as for external arc fault at point $\boldsymbol{F}_{ext}$, CuSum(I_{dc3}) < CuSum($I_{dc,avg}$) which avoids false detection.

5.4 Comparative analysis

The proposed fault protection scheme is effective in terms of accurate fault distance calculation as shown in Tables 5 and 6. Table 5 shows error variation for PP fault where error is high for short-distance faults and increased R_f values. In Table 6, for PG fault error variation is recorded similarly for the proposed protection measure. The range of error variation for PG is high as compared with PP fault. The calculated percentage of error is less as compared with existing PPU [10] method.

The percentage of error is calculated as given in (23)

$$\%\varepsilon = \left|\frac{d_{cal} - d_{act}}{d_{act}}\right| \times 100 \tag{23}$$

where d_{cal} is calculated distance and d_{act} is actual fault distance.

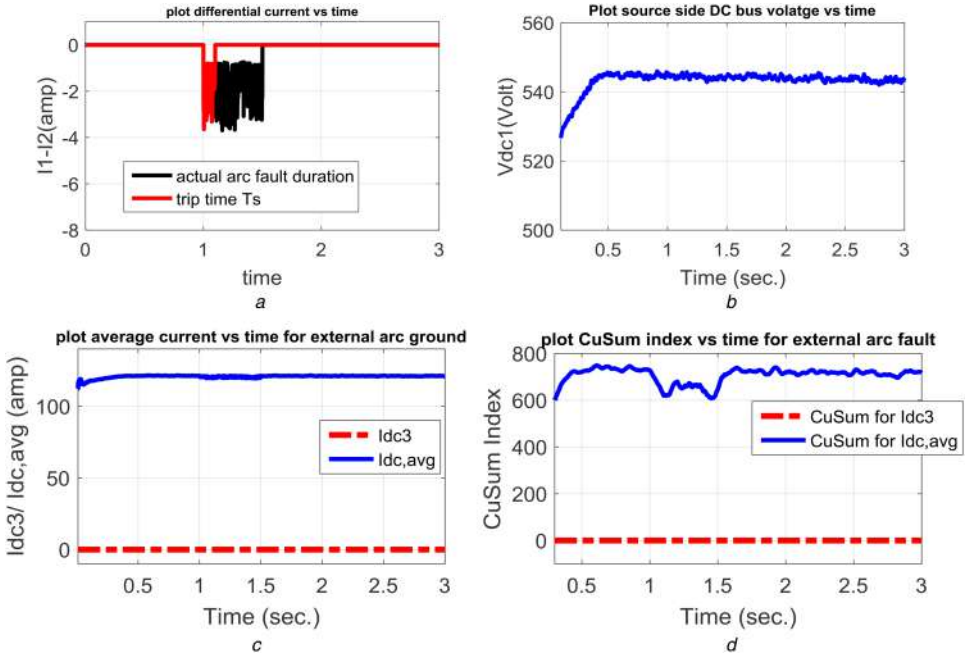

Fig. 10 *Variation of DC network parameters during DC ground arc fault for PV1 system*

(a) Trip time (*Ts*) of DC switches with fault current (I_{dc3}), ***(b)*** Input DC voltage (V_{dc1}) to the load, ***(c)*** Differential current (I_{dc3}) and average current ($I_{dc,avg}$) for external fault, ***(d)*** CuSum(I_{dc3}) < CuSum ($I_{dc,avg}$) for external fault

5.5 Hardware validation at TMS320 C6713 digital signal processor (DSP) platform

A test bench simulation is achieved for the proposed DC microgrid protection scheme, through efficient 32 bit DSP, TMS320C6713 [18]. The proposed CuSum-based detection and Moore–Penrose pseudo-inverse fault distance solution is obtained as a function on TMS320 DSP Starter Kit with the help of embedded MATLAB coder. The test bench system is proposed for validation of the fault detection scheme for DC series arc faults; and influence of noisy converter channel.

5.5.1 Series arc for PV system: DC arc faults are treacherous phenomena for DC cables, due to the high stored energy and the temperature rise (i.e. fire hazard) at arc point. Standard circuit breakers, GF circuit breakers are generally failure to detect this event due to impedance limited, below threshold fault current level. DC arcing is a spark across air or another dielectric, and PV systems are prone to this event due to various series, parallel configured modules, arrays in a small distanced area. With a broken connection, leaving two adjacent cables in a junction box, between modules and within modules are possible sources for series arc. Two different voltage cable points within a module or array, especially with compromised parallel cable insulation is potential source of parallel arc. Limited fault current is produced by series arc due to the load with which it is in series, while parallel arc can absorb high current, as much as the source is capable to supply. Disorganised array, module operations, failure of bypass diode etc. may cause due to these arc faults.

For the proposed detection scheme, series arc faults are well distinguished by the proposed CuSum calculation as shown in Fig. 11*b*. Though the fault current level (I_{dc3}) is very minimum with fault resistance of 25 Ω (Fig. 11*a*) for a series arc at $t = 0.75$ s to 1.5 s, BT detection scheme detects the fault due to significant CuSum index. However, for parallel arc, the high current flow trip the backup breaker (conventional, AFCI) before the proposed fault detection scheme. The details of AFCI interfacing and its effect for PV-based converter operation are discussed in [5]. Detection of DC series arc (i.e. low-fault current detection peak, more heating) by AFCI is disadvantageous due to challenges related to electromechanical air gap, calibration control, and requirement of constant replacement of electrode. To overcome these, extra apparatus and methods are to be needed [19]. However, for DC parallel arc (i.e. high-fault current overshoot in a short span) AFCI works comfortably. In the proposed scheme, the series arc is detected by CuSum-based amplified detection peak and local circuit breakers, to avoid AFCI burden.

5.5.2 Circuit breaker operation and converter noise: GFCIs are able to detect very small leakage current (mA) within 200 ms trip [5] and considered for DC arc fault detection by NEC. According to underwriters laboratories (UL) 1699B (article 690 of NEC), AFCI devices are mandatory for implementation of any PV system. Asea Brown Boveri (ABB) circuit breakers (S800PV-S) for direct current applications, are well suited for DC microgrid (< 1 kV) operations and hence considered for the proposed detection scheme validation. A 1 km PP fault with fault resistance 0.5 Ω is subjected for the proposed DSP test bench at $t = 1$ s to 1.45 s, as in Fig. 12*a*. The circuit breaker tripped successfully within 100 ms; moreover, the semiconductor switching off transient shows a small reverse recovery characteristic, as shown in Fig. 12*b*. A reclosing event is subjected after fault clearance with a restricting current [20] for <40 ms. The recommended standards (Indian standards (IS)/IEC 60947-2, 2003) are followed [21] by S800PV-S for commercial circuit breaker operation in the distribution level networks. The detailed characteristic of S800PV-S circuit breaker is presented in [22]. From the tripping characteristic the delay time (total switch-off time) for this DC switch is found to be <2.5 ms for 1.2 kV DC link. For a trip time range within 100 ms (i.e. the proposed scheme) this switching delay is included as mentioned in Section 3.2. For capacitor-based protection [23], the maximum discharging time of capacitor current is recorded in microsecond range, which is negligible for this scheme.

High-frequency converter switching introduces noise to the system operation (discussed in Section 4) and may cause false detection, sympathetic tripping etc. The range of such noise varies from few hundred kHz to few MHz, and thus 30−60 dB noise is subjected to the DSP-based test bench validation as shown in Fig. 12*c*. In this figure, fault current with noise (30 dB) is obtained from DC converter output, and subjected to the proposed detection scheme. The effective detection and circuit breaker tripping is validated in Fig. 12*d*, where 60 dB noise is subjected. The noise distortion and false trip of circuit breakers are well described in the literature. Fast disconnection in DC lines can be achieved by fuses and mechanical switches. The slow response is the main drawback of these methods. To cope with this problem, the semiconductor circuit breaker has been paid attention [24]. Furthermore, the noise generated during circuit breaker switch cut-off can be suppressed

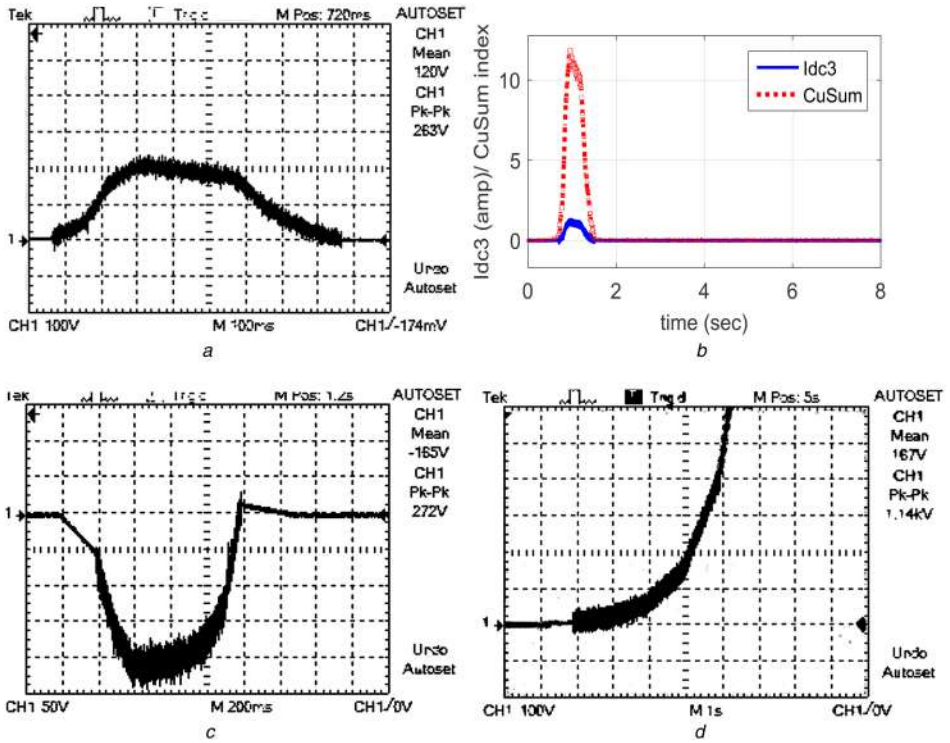

Fig. 11 *Different DC arc faults characteristic at PV arrays*

(a) Differential fault current (I_{dc3}), ***(b)*** CuSum index with I_{dc3} for series arc, ***(c)*** Voltage deviation (V_{dc}) during series arc, ***(d)*** Differential fault current (I_{dc3}) for parallel arc fault scenario

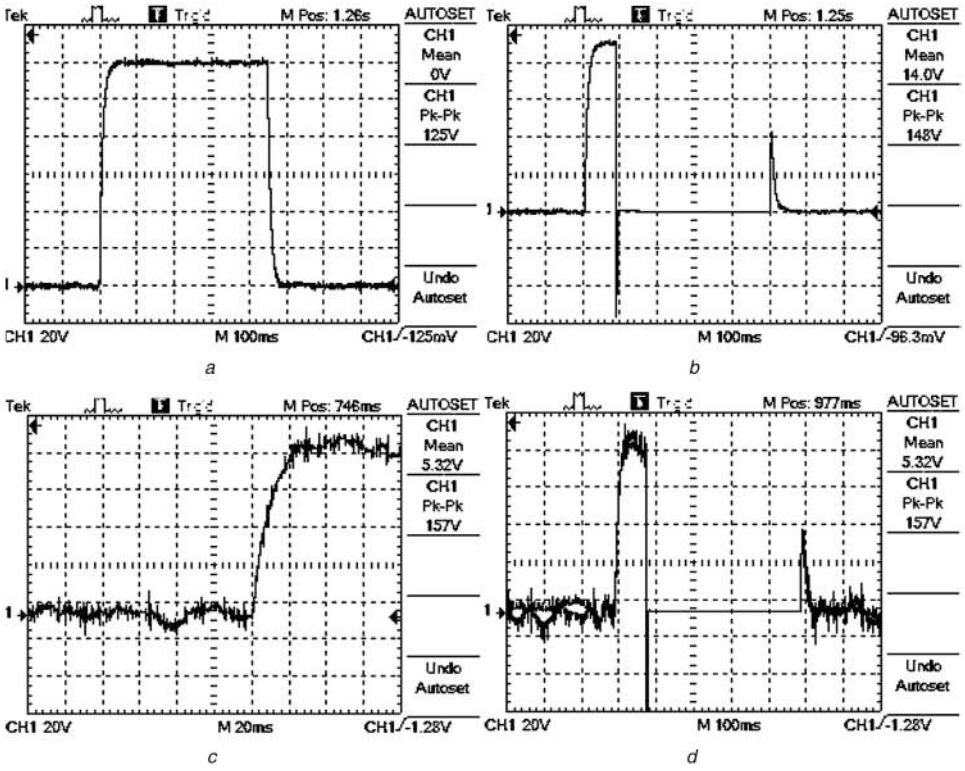

Fig. 12 *Performance of the proposed scheme during PP fault with fast DC switching*

(a) Actual differential current (I_{dc3}), ***(b)*** Differential current (I_{dc3}) trip with restricting current at reclosing, ***(c)*** Differential current with permissible noise input (30 dB), ***(d)*** Effective circuit breaker trip during noisy (60 dB) differential current

apparently by applying bypass capacitor [25], to avoid malfunction. The proposed circuit breaker trips effectively for 30−60 dB noise (maximum allowable range).

6 Conclusion

A new differential current-based fault detection and distance calculation scheme is proposed in this paper based on CuSum and Moore–Penrose pseudo-inverse techniques. This protection scheme is proposed for a multiple PV-based MTDC low-voltage distribution network connected with utility. As various high-frequency power electronics converters of the DGs are connected to the common DC bus, fast fault detection is essential for protecting the power electronic converters. The proposed protection scheme is subjected to different faults such as PP, PG

etc. for validating its effectiveness. Worst-case scenario is presented with DC arc (ground, series) faults, when PV system is absent from proper grounding. A rigorous case study is presented here based on MATLAB/Simulink platform where test validation is achieved by TMS320C6713-based DSP. Trip time (*Ts*) and percentage error are considered for efficiency calculation of the proposed approach. The proposed differential current-based protection method is effectively used for fast (<100 ms) fault detection as well as accurate distance measurement as compared with [11], and this non-iterative scheme is superior in comparison to the PPU-based protection [10] by abolishing the requirement of extra equipment for fault distance measurement.

7 References

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