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A Common-Gate Current-Reuse UWB LNA for Wireless Applications in 90 nm CMOS

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Abstract
In this paper, a CMOS low noise amplifier (LNA) for ultra-wideband (UWB) wireless applications is presented. The proposed CMOS LNA is designed using common-gate (CG) topology at the first stage to achieve ultra wideband input matching. The common-gate has been cascaded with common-source (CS) current-reused configuration to enhance the gain and noise figure (*NF*) performance of the LNA with low power consumption. In order to ensure maximum power flow from CG input stage to g_{m} boosted CS current-reused stage, parallel-series LC matching has been used. The output-matching network is used to improve the output reflection coefficient. The LNA is designed using standard 90 nm CMOS process for 3.1–10.6 GHz UWB. It exhibits a power-gain (S_{21}) of 19.2–20.8 dB, an *NF* of 2.3–3.7 dB, a reverse-isolation (S_{12}) of less -53.8 dB and an S_{22} of less than -6 dB for the entire UWB frequency range. The proposed LNA has an input reflection coefficient (S_{11}) of less than -10.6 dB for 3.1–10.6 GHz. It achieves input 1-dB compression point (*P1dB*) of -17 dBm at 6 GHz and input third-order intercept point (*IIP3*) of -8 dBm, while it consumes only 5.05 mW of power from a V_{dd} supply of 0.7 V.

Keywords Common-gate · Current-reuse · Input-matching · Low noise amplifier · UWB · Wireless communication

1 Introduction

The continuously emerging new applications of wireless communication devices lead to the development of communication systems with low power consumption, high data rate and wider bandwidth. Simultaneously in 2002, Federal Communications Commission (FCC) [1] releases 3.1–10.6 GHz frequency spectrum for unlicensed operations and attract researchers and engineers to design communication devices for UWB frequency. In last

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few years ultra-wideband (UWB) technology is proving itself as the best candidate for designing of UWB digital applications with high data transmission rate, low complex circuits and high immunity. The UWB consists of fourteen channels each having bandwidth of 528 MHz which are further clustered in five band-groups (BG) as shown in Fig. 1. FCC imposed maximum upper power emission limit of −41.3 dBm/MHz on UWB channels to avoid any inter-channel interference with neighboring channels. This motivates researchers to design wireless communication devices for UWB.

Further, in order to survive and fulfill the requirements of current and future market trends, the complementary metal-oxide semiconductor (CMOS) technology is preferably used to design radio frequency integrated circuits (RFICs) with low power consumption, large integration and smaller size. In comparison to SiGe based HBTs, GaAs based HEMTs and BJTs, the continuous scaling in CMOS with advanced fabrication technologies makes it now possible to fabricate RFICs as a system on chip (SOC) using CMOS, without sacrificing the performance of RFICs [2].

The low noise amplifier (LNA) is a primary module in the receiver chain of all wireless communication devices. Low noise figure (*NF*) preferably less than 3.0 dB, high flat power gain (S_{21}) to amplify weak input signal received from 50 Ω antenna, wideband band input-matching, high reverse-isolation (S_{12}), high linearity and unconditional stability are the key factors in defining the overall performance of the CMOS UWB receiver [3]. Simultaneous achievement of all the performance parameters of LNA is a very critical task as there are trades off between these performance parameters which make the LNA design process more critical. Input-matching and the noise figure characteristics of an UWB LNA forms the basis for broadly categorizing the architectures of CMOS UWB LNA into two major groups specifically: common-source and Common-gate as shown in Fig. 2.

Common-source resistive termination shown in Fig. 2a could be a way to enhance the bandwidth of LNA [4–6]. But the inclusion of a resistance at gate of input CS transistor is not only attenuates the input signal but also adds to the noise figure of the CS-LNA. Adding resistance at the input also puts a lower bound on the noise figure i.e., $NF \geq 2 + 4(\gamma/\alpha)(1/g_m R_s)$ of the CS-resistive termination LNA, where α is the ratio of the transconductance (g_m) and zero-bias transconductance (g_{ds0}) of the input transistor. The trade-off between power-gain (S_{21}) and noise figure (*NF*) is also seen in this topology. Resistive-feedback shown in Fig. 2b has also been explored by many researchers [7–9] to achieve UWB input-matching and low *NF*. As, extra noise has been added by the feedback resistor R_f, lower limit of *NF* is restricted to nearly 3.5 dB. CS with inductive-degeneration (CSID) shown in Fig. 2c can be another solution for wideband

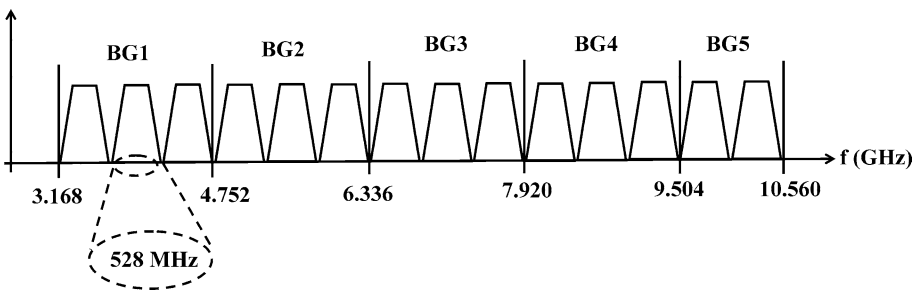

Fig. 1 Ultra-wideband frequency spectrum released by FCC in the year 2002

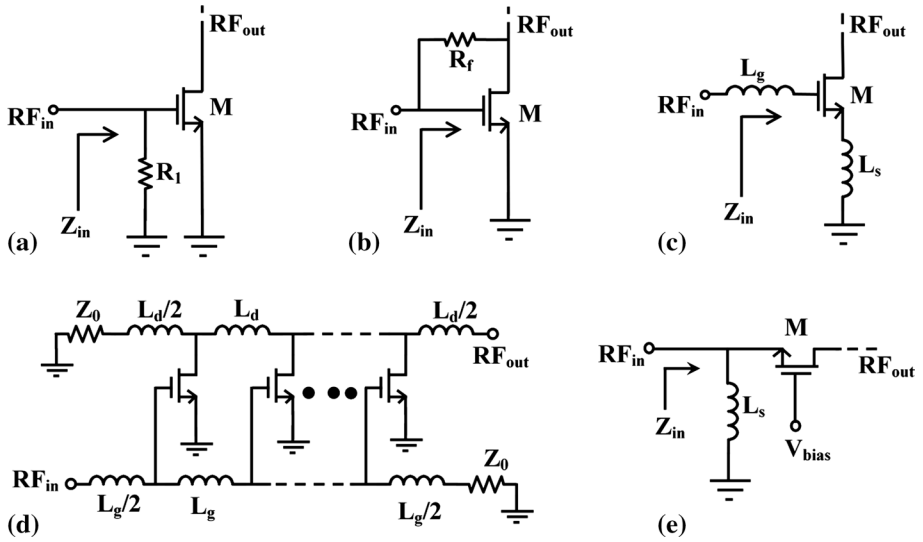

Fig. 2 Basic wide-band LNA topologies **a** Common Source with resistive termination, **b** Common Source with resistive feedback, **c** Common Source with inductive degeneration, **d** Distributed LNA, and **e** Common Gate LNA

LNA with low noise figure [6, 10, 11]. The input impedance, $Z_{in}(\omega)$ of CSID is given by $Z_{in}(\omega) = j\omega\left(L_g + L_s\right) + \left(j\omega C_{gs}\right)^{-1} + \omega_T L_s$, ω_T is the unity gain frequency of the transistor and is given by ratio of the tansconductance (g_m) and the gate-source parasitic capacitance (C_{gs}) of the input transistor M. The input resonance frequency (ω_0) of the CSID-LNA is given by $\omega_0 = \left(\left(L_g + L_s\right)C_{gs}\right)^{-1}$. The matched input quality-factor (Q_{in}) and the noise figure of the CS LNA in matched condition can be expressed as $\left(2\omega_0 R_s C_{gs}\right)^{-1}$ and $\left\{1 + \gamma/\left(g_m R_s Q_{in}^2\right)\right\}$, respectively, where γ is the coefficient of the channel induced thermal noise [6–9]. The quality factor of the CS-LNA under matching conditions is very small and this makes CS-LNA more suitable only for the design of narrow band or wide-band LNAs. The quality factor of CS-LNA can be increased by the use of small input transistors. However, this in turn demands for large size of the source inductor to resonate with small gate-source parasitic capacitance of the input transistor, which increases the chip area. Distributed-LNAs shown in Fig. 2d, on the other hand could be another solution for wideband LNA, but due additive nature, gain of distributed-LNA is limited to 8–10 dB and large chip area is another major disadvantage of distributed-LNA [12–14].

Common-gate LNA shown in Fig. 2e on the other hand provides a less complicated way to achieve constant ultra-wideband input match by providing $1/g_m \approx 50$ ohms [15–17]. But noise figure of CG-LNA is higher than that of CS-LNA due to low power gain capability. This paper reports a common-gate low noise amplifier topology, cascaded to a cascoded common-source current-reused amplifier to design UWB LNA with flat and high power gain by boosting up the gain and with very small power consumption.

The rest of this paper is organized as follows: Section 2 describes the circuit of the proposed LNA. Circuit analysis for the proposed LNA design is given in Sect. 3. Section 3.1 describes the input matching analysis and frequency response analysis for S_{21}, whereas Sect. 3.2 provides noise figure analysis for the proposed LNA design. Simulation results

for the proposed LNA design is shown in Sect. 4 with a table of comparison with existing LNA topologies. Finally conclusion is done in Sect. 5.

2 Proposed LNA design

Figure 3 shows the circuit diagram of the proposed LNA design. It consists of a common-gate input stage followed by a cascoded common-source current-reused stage and an output-matching circuit. The common-gate configuration at the input side has been utilized here due to its wide-band input-matching capability with 50 Ω antenna impedance. Connecting an inductor L_{s1} at the source terminal of M_1 forms a parallel LC resonator with gate-source parasitic capacitance C_{gs1} of M_1 as shown by the small signal model of the proposed LNA in Fig. 4a, which decides the Q-factor of the input common-gate stage. Parallel LC resonance circuit provides a low value of Q-factor under matching conditions i.e.,$Q_{in,CG,matched} = (\omega C_{gs1} R_s/2)$, which ensures a large input-matching bandwidth.

At the output of common-gate, the inductor L_{d1} resonates in parallel with gate-drain parasitic capacitance C_{gd1} of M_1 at $1/\sqrt{(L_{d1}C_{gd1})}$. The capacitor C_1 has been used as coupling capacitor. The inductor L_{g2} forms a series LC tank with gate-source parasitic capacitance C_{gs2} of M_2 resonating at $1/\sqrt{(L_{g2}C_{gs2})}$. This forms a parallel to series LC matching network between common-gate and common-source stage. Conceptually, the band-pass filter's frequency response can easily be achieved from this parallel-series LC matching when both the parallel and series LC tanks resonates at the same resonance frequency and this could be achieved when $L_{d1}C_{gd1} = L_{g2}C_{gs2}$. For analysis of the inter-stage matching network the conceptual diagram of the matching network is given in Fig. 4a. In this impedance (Z_p) of the parallel network can be expressed as

$$Z_P = \left(\frac{1}{R_{out,CG}} + j\omega C_{gd1} + \frac{1}{j\omega L_{d1}} \right)^{-1} = R_P + jX_P \tag{1}$$

Assuming

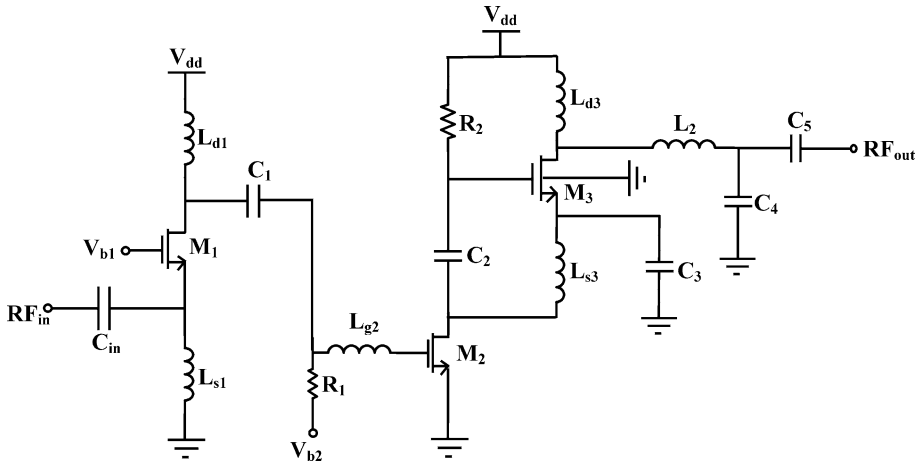

Fig. 3 Circuit diagram of the proposed common gate UWB current reused LNA

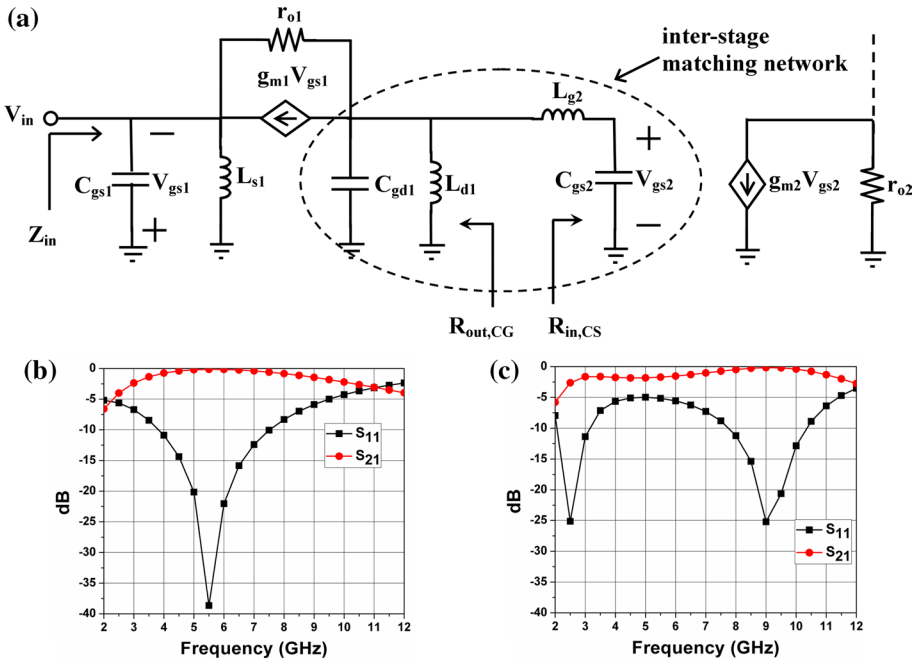

Fig. 4 **a** Small-signal model of the proposed LNA showing parallel-series LC inter-stage matching between CG and the cascaded CS stage, **b** Frequency response for S_{11} and S_{21} of inter-stage matching network, with $R_{out,CG}=R_{in,CS}=50\ \Omega$, $C_{gd1}=0.22$ pF, $L_{d1}=5.2$ nH, $L_{g2}=2.0$ nH, $C_{gs2}=0.45$ pF, **c** Frequency response for S_{11} and S_{21} with $R_{out,CG}=170\ \Omega$, $R_{in,CS}=50\ \Omega$

$$\omega C_{gd1}-\frac{1}{\omega L_{d1}}=\frac{\omega^2-\omega_0^2}{\omega_0^2\omega L_{d1}}=\pm K_P \tag{2}$$

where $\omega_0=\left(\sqrt{L_{d1}C_{gd1}}\right)^{-1}$ and here + sign is considered for $\omega>\omega_0$ while − sign is considered for $\omega<\omega_0$.

Similarly, the impedance (Z_S) of the series network can be expressed as

$$Z_S=\left(R_{in,CS}+j\omega L_{g2}-\frac{1}{j\omega C_{gs2}}\right)=R_S+jX_S \tag{3}$$

Assuming

$$\omega L_{g2}-\frac{1}{\omega C_{gs2}}=\frac{\omega^2-\omega_0^2}{\omega_0^2\omega C_{gs2}}=\pm K_S \tag{4}$$

where $\omega_0=\left(\sqrt{L_{g2}C_{gs2}}\right)^{-1}$ and here + sign is considered for $\omega>\omega_0$ while − sign is considered for $\omega<\omega_0$.

Case-I: When $\omega>\omega_0$, after substituting (2) into (1) and (4) into (3) we have

$$Z_P = \frac{R_{out,CG} - jK_P R_{out,CG}^2}{1 + K_P^2 R_{out,CG}^2} \tag{5}$$

$$Z_S = R_{in,CS} + jK_S \tag{6}$$

By forcing $R_P = R_S$ and $X_P = -X_S$ at $\omega = \omega_H$, we have

$$\frac{R_{out,CG}}{1 + K_P^2 R_{out,CG}^2} = R_{in,CS} \quad \text{or} \quad K_P^2 = \frac{R_{out,CG} - R_{in,CS}}{R_{out,CG}^2 R_{in,CS}} \tag{7}$$

$$\frac{K_P R_{out,CG}^2}{1 + K_P^2 R_{out,CG}^2} = K_S \tag{8}$$

which mean that

$$R_{out,CG} > R_{in,CG} \tag{9}$$

$$K_P R_{out,CG} R_{in,CS} = K_S \tag{10}$$

On substituting the values of K_P and K_S in Eqs. (2) and (4), we have

$$L_{d1} = R_{out,CG} R_{in,GS} C_{gs2} \tag{11}$$

Case-II: When $\omega < \omega_0$.

Similarly, Eqs. (1) and (3) becomes

$$Z_P = \frac{R_{out,CG} + jK_P R_{out,CG}^2}{1 + K_P^2 R_{out,CG}^2} \tag{12}$$

$$Z_S = R_{in,CS} - jK_S \tag{13}$$

By forcing $R_P = R_S$ and $X_P = -X_S$ at $\omega = \omega_L$, we again obtained the same results of (7) and (8). For conjugate matching, ω_H and ω_L can be expressed in terms of K_P and K_S as given below

$$\omega_H = \frac{K_P \omega_0^2 L_{d1} + \left(K_P^2 \omega_0^4 L_{d1}^2 + 4\omega_0^2\right)^{1/2}}{2} \tag{14}$$

$$\omega_H = \frac{K_S \omega_0^2 C_{gs2} + \left(K_S^2 \omega_0^4 C_{gs2}^2 + 4\omega_0^2\right)^{1/2}}{2} \tag{15}$$

$$\omega_L = \frac{-K_P \omega_0^2 L_{d1} + \left(K_P^2 \omega_0^4 L_{d1}^2 + 4\omega_0^2\right)^{1/2}}{2} \tag{16}$$

$$\omega_L = \frac{-K_S\omega_0^2 C_{gs2} + \left(K_S^2\omega_0^4 C_{gs2}^2 + 4\omega_0^2\right)^{1/2}}{2} \tag{17}$$

In order to equalize Eqs. (14) and (15), Eqs. (10) and (11) must be satified and similary is the case for Eqs. (16) and (17).

With the presumption of conditions that the output resistance of CG ($R_{out,CG}$) and input resistance of CS stage ($R_{in,CS}$) is equal to 50 Ω, in a sample run of parallel-series LC matching network it has been observed from Fig. 4b that the frequency response of S_{11} and S_{21} for parallel-series network shows a band-pass behavior. When $R_{out,CG}$ deviates from 50 Ω then due to complex-conjugate resonance between parallel and series LC tanks, gain slightly decreases from center frequency with an increase in the bandwidth, as shown in Fig. 4c.

In the next stage, cascoded common-source current-reused topology has been used to achieve a very high gain with very low power consumption, which improves the overall noise figure of the proposed LNA design. The operation of current-reused structure can be explained using its DC and AC analysis. In DC-mode, inductor L_{d3} and L_{s3} behaves as short circuit and provides dc-biasing voltage to M_2 and M_3. In AC-mode, the capacitor C_2 behaves as short circuit and L_{s3} resonates in parallel with gate-source parasitic capacitance (C_{gs3}) of M_3, whereas the capacitor C_3 will behaves as a bypass capacitor at higher frequencies of ultra wide-band. Inductor L_{d3} on the other hand forms parallel LC tank with gate-drain parasitic capacitance C_{gd3} of M_3. Table 1 provides the component values for the proposed LNA design.

3 Circuit analysis

3.1 Input matching analysis and frequency response of S_{21}

Figure 5a shows the small signal equivalent circuit common-gate stage with load impedance $Z_{load1}(\omega)$ connected at the drain of M_1. If Z_x is the impedance looking into the source of the common-gate transistor M_1, then $Z_x(\omega)$ can be expressed as

$$Z_x(\omega) = \frac{r_{o1} + Z_{Load1}(\omega)}{1 + g_{m1}r_{o1}} \tag{18}$$

where, $Z_{Load1}(\omega)$ is the total load impedance connected at drain terminal of M_1 and is given by

Table 1 Component values for the proposed LNA

Transistors No. of Finger × W(μm) × L(μm)		Inductance (nH)		Capacitance (pF)		Resistance (KΩ)	
M_1	50 × 50 × 0.09	L_{s1}	5.1	C_{in}	2.0	R_1	5.0
M_2	1 × 90 × 0.09	L_{d1}	8.5	C_1	2.0	R_2	0.2
M_3	10 × 178 × 0.09	L_{g2}	5.6	C_2	1.0		
		L_{s3}	0.36	C_3	3.2		
		L_{d3}	4.0	C_4	0.2		
		L_2	0.9	C_5	2.5		

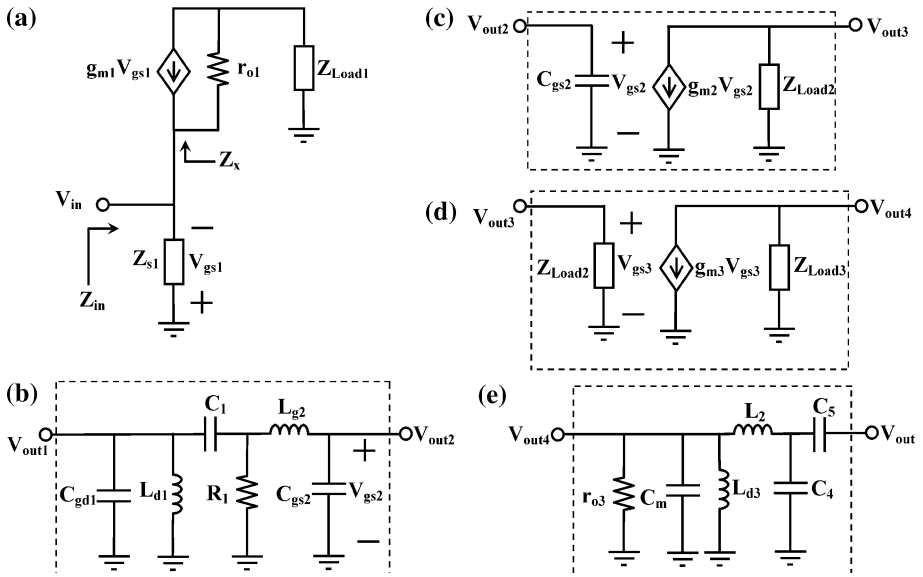

Fig. 5 Stage-wise small signal equivalent circuit of the proposed LNA design for input-matching and voltge-gain analysis

$$Z_{Load1}(\omega) = j\omega L_{d1} \left\| \frac{1}{j\omega C_{gd1}} \right\| \left(\frac{1}{j\omega C_1} + R_1 \left\| \left(j\omega L_{g2} + \frac{1}{j\omega C_{gs2}} \right) \right. \right) \approx jX_{Load1}(\omega) \quad (19)$$

If $Z_{s1}(\omega)$ is the impedance of the parallel combination of L_{s1} and C_{gs1}, then $Z_{s1}(\omega)$ can be approximated as $jX_{s1}(\omega)$. Therefore the input impedance of the proposed common-gate UWB LNA can be approximated as

$$\begin{aligned} Z_{in}(\omega) == & \left[\frac{1}{Z_{s1}(\omega)} + \frac{1 + g_{m1} r_{o1}}{r_{o1} + Z_{Load1}(\omega)} \right]^{-1} \\ = & \left[g_{m1} - j \frac{1}{X_{s1}(\omega)} + \frac{1 - j g_{m1} X_{Load1}(\omega)}{r_{o1} + j X_{Load1}(\omega)} \right]^{-1} \\ = & \left[\left(g_{m1} - \frac{g_{m1} X_{Load1}^2(\omega) - r_{o1}}{r_{o1}^2 + X_{Load1}^2(\omega)} \right) - j \left(\frac{1}{X_{s1}(\omega)} + \frac{1 + g_{m1}.r_{o1}}{r_{o1}^2 + X_{Load1}^2(\omega)} X_{Load1}(\omega) \right) \right]^{-1} \end{aligned} \quad (20)$$

In Eq. (20) the imaginary part is dominated by the term $1/X_{s1}(\omega)$ because for the frequency of interest, $g_{m1}.r_{o1}, X_{Load1}(\omega)$ would be far less than $r_{o1}^2 + X_{Load1}^2(\omega)$. Further, $g_{m1}.X_{Load1}^2(\omega)$ is very small as compared to the $r_{o1}^2 + X_{Load1}^2(\omega)$ and this will results in a good wide-band input impedance matching by providing a relatively constant real part. ie., $1/g_{m1}$. The g_{m1} of M_1 is set to a large value that results in less than 50 Ω because the amount less by 50 Ω will be contributed by the total load impedance connected to the drain of M_1. Simultaneously, the inductor L_{s1} is set to 5.1 nH such that it resonates with the small valued C_{gs1} near the center frequency of UWB. The input reflection coefficient is then approximated using the standard expression as [18]

$$S_{11} = \frac{Z_{in}(\omega) - R_s}{Z_{in}(\omega) + R_s} \tag{21}$$

Since, in the proposed LNA design the current-reused stage has been used at the second stage and this stage has been used to improves overall performance of the LNA circuit in terms of its noise figure and power gain. For frequency response analysis of S_{21} the small signal model of each stage shown in Fig. 5 has been used. The frequency response of S_{21} can be approximated by calculating the transfer function of the complete LNA design. Let A_{V1}, A_{V2}, A_{V3}, A_{V4} and A_{V5} are the voltage gain of respective block shown in Fig. 5. Then the expression for the overall voltage gain (A_v) can be expresses as

$$A_V = \frac{V_{out}}{V_{in}} = A_{V1} \times A_{V2} \times A_{V3} \times A_{V4} \times A_{V5} \tag{22}$$

where, $A_{V1} = \frac{V_{out1}}{V_{in}}$, $A_{V2} = \frac{V_{out2}}{V_{out1}}$, $A_{V3} = \frac{V_{out3}}{V_{out2}}$, $A_{V4} = \frac{V_{out4}}{V_{out3}}$ and $A_{V5} = \frac{V_{out}}{V_{out4}}$.

Applying network theorems we have

$$A_{V1} = \left(1 + g_{m1} r_{o1}\right) / \left(1 + \frac{r_{o1}}{Z_{Load1}(\omega)}\right) \tag{23}$$

$$A_{V2} = j\omega R_1 C_1 / \left(\left(1 - \omega^2 L_{g2} C_{gs2}\right) + j\omega R_1 \left(C_{gs2} + C_1 \left(1 - \omega^2 L_{g2} C_{gs2}\right)\right)\right), \tag{24}$$

$$A_{V3} = -g_{m2} Z_{Load2}(\omega) \tag{25}$$

where, $Z_{Load2}(\omega) = r_{o2} \left\| Z_{gs3}(\omega) \right.$ and $Z_{gs3}(\omega) = R_2 \left\| \left(\frac{1}{j\omega C_{gs3}} \| j\omega L_{s3} \right) \right.$.

The voltage gain A_{v4} is given by

$$A_{V4} = -g_{m3} Z_{Load3}(\omega) \tag{26}$$

where, $Z_{Load3}(\omega) = r_{o3} \left\| \left(\frac{1}{j\omega C_{m3}} \| j\omega L_{d3} \right) \right\| \left(j\omega L_2 + \frac{1}{j\omega C_4} \right)$ and C_{m3} is the miller capacitance at drain-ground terminal of M_3. Finally, A_{v5} can be expresses as

$$A_{V5} = \frac{1}{1 - \omega^2 L_2 C_4} \tag{27}$$

Therefore, the power gain (S_{21}) of the proposed common-gate current reused UWB LNA can be expressed using the overall voltage gain A_v as [18]

$$S_{21} = 2.\frac{V_{out}}{V_s} \approx 2.\frac{Z_{in}(\omega)}{R_s + Z_{in}(\omega)} \times A_V \tag{28}$$

where V_s is the input signal source voltage and V_{out} is the respective output voltage.

3.2 Noise figure analysis

Noise figure of an LNA is the key parameter in deciding the performance of a UWB receiver. For calculating the noise-figure, small-signal noise equivalent model of the proposed LNA is shown in Fig. 6. Three major noise sources have been considered here, the

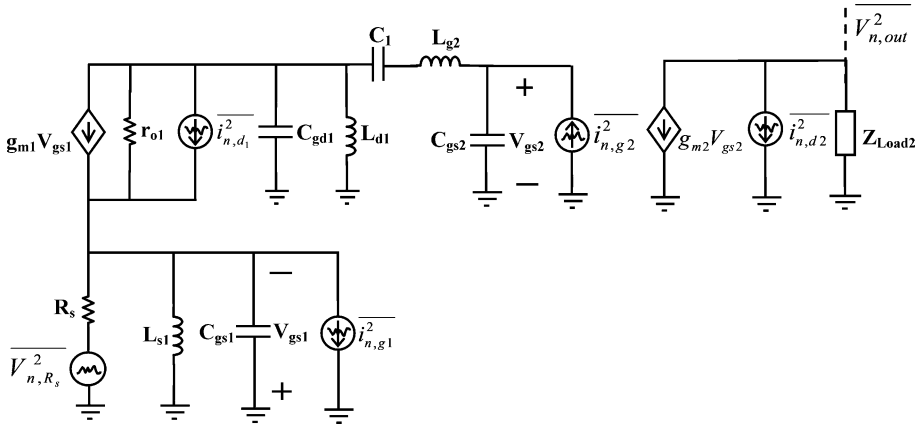

Fig. 6 Noise equivalent small signal model of the proposed LNA

thermal noise of antenna source resistance $\left(\overline{V_{n,Rs}^2}\right)$, gate induced noise $\left(\overline{i_{n,g1}^2}, \overline{i_{n,g2}^2}\right)$ and channel induced thermal noise $\left(\overline{i_{n,d1}^2}, \overline{i_{n,d2}^2}\right)$ due to M_1 and M_2 respectively, where $\overline{V_{n,Rs}^2} = 4kTR_s\Delta f$, $\overline{i_{n,g1}^2} = 4kT\delta g_{g1}\Delta f$, $\overline{i_{n,d1}^2} = 4kT\gamma g_{d01}\Delta f$, $\overline{i_{n,g2}^2} = 4kT\delta g_{g2}\Delta f$ and $\overline{i_{n,d2}^2} = 4kT\gamma g_{d02}\Delta f$, with k=Boltzmann constant, T=temperature in Kelvin, Δf=noise bandwidth and the equivalent gate conductances $g_{g1} = \left(\omega^2 C_{gs1}^2\right)/\left(5g_{d01}\right)$ and $g_{g2} = \left(\omega^2 C_{gs2}^2\right)/\left(5g_{d02}\right)$, respectively.

Firstly, the output noise voltage due to each noise sources have been calculated here using the voltage gain relations as follows

$$V_{n,out,Rs} = \frac{Z_{Load1}(\omega)\left(1+g_{m1}r_{o1}\right)}{\left(r_{o1}+Z_{Load1}(\omega)\right)\left(1+\frac{R_s}{Z_{s1}(\omega)}\right)+R_s\left(1+g_{m1}r_{o1}\right)} \times V_{n,Rs} \times A_{V2} \times A_{V3} \times A_{V4} \times A_{V5} \tag{29}$$

$$V_{n,out,g1} = \frac{Z_{Load1}(\omega)\left(1+g_{m1}r_{o1}\right)R_s}{\left(r_{o1}+Z_{Load1}(\omega)\right)\left(1+\frac{R_s}{Z_{s1}(\omega)}\right)+R_s\left(1+g_{m1}r_{o1}\right)} \times i_{n,g1} \times A_{V2} \times A_{V3} \times A_{V4} \times A_{V5} \tag{30}$$

$$V_{n,out,d1} = \frac{r_{o1}Z_{Load1}(\omega)\left(1+\frac{R_s}{Z_{s1}(\omega)}\right)}{\left(r_{o1}+Z_{Load1}(\omega)\right)\left(1+\frac{R_s}{Z_{s1}(\omega)}\right)+R_s\left(1+g_{m1}r_{o1}\right)} \times i_{n,d1} \times A_{V2} \times A_{V3} \times A_{V4} \times A_{V5} \tag{31}$$

$$V_{n,out,g2} = -g_{m2}Z_{in,m2}(\omega)Z_{Load3}(\omega) \times i_{n,g2} \times A_{V4} \times A_{V5} \tag{32}$$

$$V_{n,out,d2} = -Z_{Load3}(\omega) \times i_{n,d2} \times A_{V4} \times A_{V5} \tag{33}$$

then using the Eqs. (29)–(33), the noise figure can be approximated as

$$
\begin{aligned}
NF &= \frac{\overline{V_{n,out,Rs}^2} + \overline{V_{n,out,g1}^2} + \overline{V_{n,out,d1}^2} + \overline{V_{n,out,g2}^2} + \overline{V_{n,out,d2}^2}}{\overline{V_{n,out,Rs}^2}} \\
&= 1 + \frac{\alpha\delta\omega^2 C_{gs1}^2 R_s}{5g_{m1}} + \frac{\gamma g_{m1}}{\alpha R_s}\left\{\frac{r_{o1}^2\left(1+\frac{R_s^2}{|Z_{s1}(\omega)|^2}\right)}{\left(1+g_{m1}^2 r_{o1}^2\right)}\right\} \\
&\quad + \frac{\alpha\delta}{5g_{m2}\left(1+g_{m1}r_{o1}\right)^2 A_{V2}^2} \times \left\{\left(1+\frac{r_{o1}^2}{|Z_{Load1}(\omega)|^2}\right)\left(1+\frac{R_s^2}{|Z_{s1}(\omega)|^2}\right)\right. \\
&\quad \left. + \left(\frac{R_s^2}{|Z_{s1}(\omega)|^2}\right)\left(1+g_{m1}r_{o1}\right)^2\right\} \\
&\quad + \frac{\gamma g_{m1}|Z_{Load3}(\omega)|^2}{\alpha R_s}\left\{\frac{\left(r_{o1}+Z_{Load1}(\omega)\right)\left(1+\frac{R_s}{Z_{s1}(\omega)}\right)+R_s\left(1+g_{m1}r_{o1}\right)}{Z_{Load1}(\omega)\left(1+g_{m1}r_{o1}\right)\times A_{V2}^2 \times A_{V3}^2}\right\}
\end{aligned}
\tag{34}
$$

Equation (34) can further be approximated and re-written as

$$
NF \approx 1 + \frac{\alpha\delta\omega^2 C_{gs1}^2 R_s}{5g_{m1}} + \frac{\gamma g_{m1}}{\alpha R_s} \times \frac{r_{o1}^2\left(1+R_s^2 1/|Z_{s1}(\omega)|^2\right)}{\left(1+g_{m1}^2 r_{o1}^2\right)} + \frac{\alpha\delta}{5g_{m2}\left(1+g_{m1}r_{o1}\right)^2 A_{V2}^2} \tag{35}
$$

Equation (35) reveals that in order to decrease the noise figure for the entire frequency of interest, the large value of g_{m1} and g_{m2} are preferred with the condition that $|Z_{s1}(\omega)|^2$ should also be large.

4 Results and discussions

The proposed CG current-reused UWB LNA is designed and then simulated using Cadence Spectre-RF using standard 90 nm CMOS process. To achieve the desired performance, the LNA is firstly designed and simulated for low noise figure with acceptable power-gain and input-matching conditions, constrained by the power consumption for different values of width of M_1 and M_2. As observed from Eq. (35) g_{m1} should be large to reduce noise figure. So, $W_1 = 50$ µm has been selected to cope-up *NF* with ultra wide-band input-matching and gain. Further, it has been observed from Eq. (35), that the width of the transistor M_2 is selected in such a way that it satisfies both the power-gain and low noise figure. For this purpose the value of W_2 was set to 90 µm. It has been observed from Fig. 7a–c that the S_{21}, which directly proportional to g_{m1} was ranging from 19.2 to 20.8 dB and $S_{11} < -10.6$ dB for 3.1–10.6 GHz, with *NF* was ranging from 2.3 to 3.7 dB for the frequency range of interest.

Using the small-signal model of output matching circuit shown in Fig. 5e, the output reflection coefficient can be estimated by calculating $Z_{out}(\omega)$ for proposed LNA and can be expressed as

$$
Z_{out}(\omega) = \left(r_{o3}||\left(1/j\omega C_M\right)||\left|j\omega L_{d3} + j\omega L_2\right)||(1/j\omega C_4\right) \tag{36}
$$

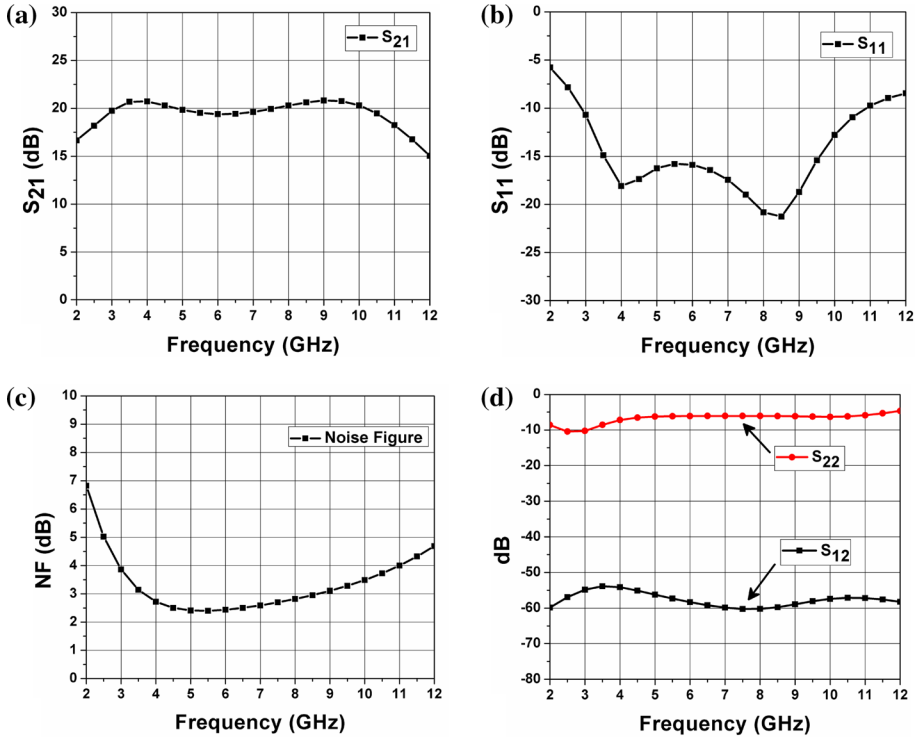

Fig. 7 Simulation results **a** S_{21} vs Frequency, **b** S_{11} vs Frequency, **c** *NF* vs Frequency and **d** S_{12} and S_{22} vs Frequency

where C_M is the miller capacitance due to gate-drain parasitic capacitance of M_3.Therefore, S_{22} can be expressed as [18].

$$S_{22} = \frac{Z_{out}(\omega) - R_s}{Z_{out}(\omega) + R_s} \tag{37}$$

The LNA achieves S_{22} less than −6.2 dB with an excellent reverse isolation (S_{12}) of less than −53.8 dB throughout the complete ultra-wideband range as shown in Fig. 7d.

Another important performance parameter for LNA is linearity that is to be taken care at the time of LNA design because it defines the capability of handling the large input signals, as linearity of the LNA mainly survives due to the non-linear components presents in expression of transconductance (g_m) of the transistor.

So further, the LNA was simulated to find analyze linearity in terms of 1-dB compression point (*P1dB*) and third order intercept point (*IIP3*). The simulated *P1dB* is −17 dBm at which gain of the LNA reduces by 1-dB and the output power at P1dB was 1.3 dBm as shown in Fig. 8a–c, respectively. For *IIP3*, two tones test has been carried out with $f_1 = 5.995$ GHz and $f_2 = 6.005$ GHz with a frequency spacing of 10 MHz and centred at 6.0 GHz. Input power has been swept from −60 to 0 dBm and extrapolating the fundamental and the third order signal response, it has been found that *IIP3* was nearly −8.0 dBm, as shown in Fig. 8d.

The inductors are the most area requirement components in the chip layout design for any LNA and they are the main key components in deciding the phase linearity of the LNA

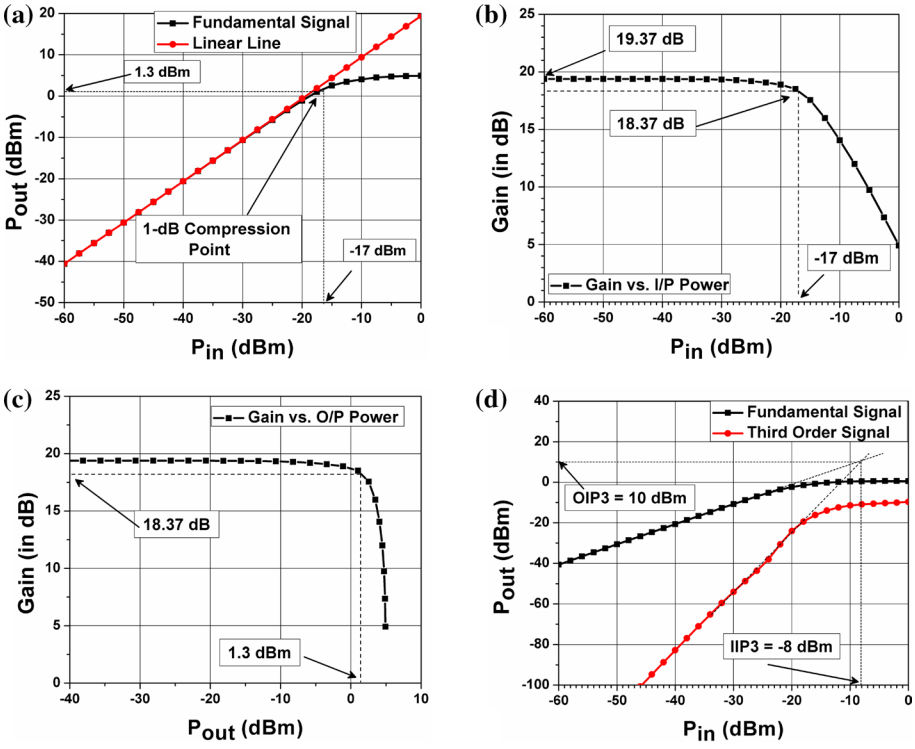

Fig. 8 **a** 1-dB compression point (*P1dB*), **b** Gain vs. Input power, **c** Gain vs. Output power and **d** Third order intercept point (*IIP3*)

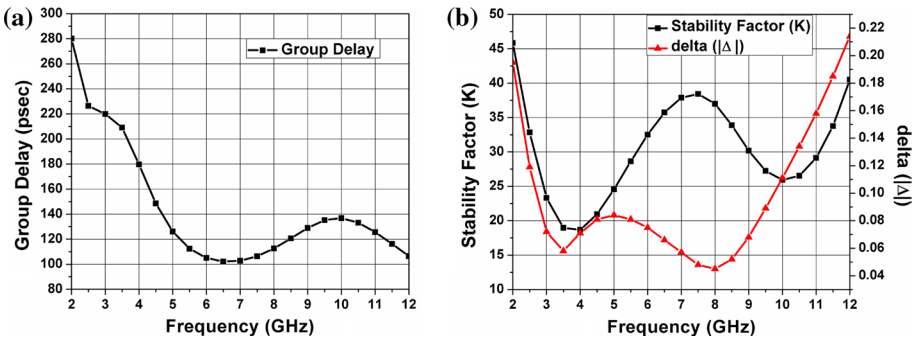

Fig. 9 **a** Group delay for the proposed LNA design and **b** stability factor (K) and delta (|Δ|) vs frequency

design. In order to achieve better phase linearity, the phase derivative of power-gain, also known as group delay of the LNA should be constant at all frequencies or there should be minimum variation in signal delay at different frequencies. The group delay of the proposed LNA is shown in Fig. 9a and it has been observed from the figure that for 3.1–10.6 GHz frequency its minimum value was 102.2 psec at 6.5 GHz and maximum value was at 219.9 psec at 3.1 GHz with an average of ±58 psec. However due the use of large sized inductors present

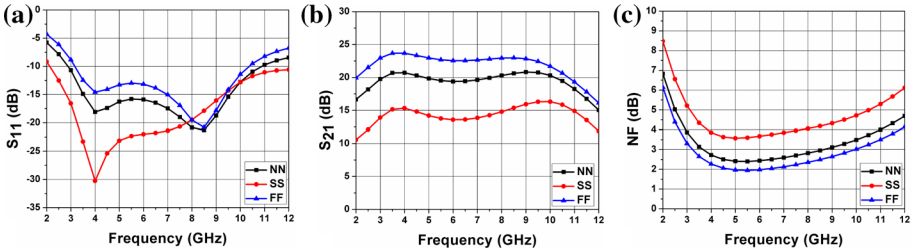

Fig. 10 Simulation results for process variations, **a** S_{11} vs Frequency, **b** S_{21} vs Frequency and **c** *NF* vs Frequency

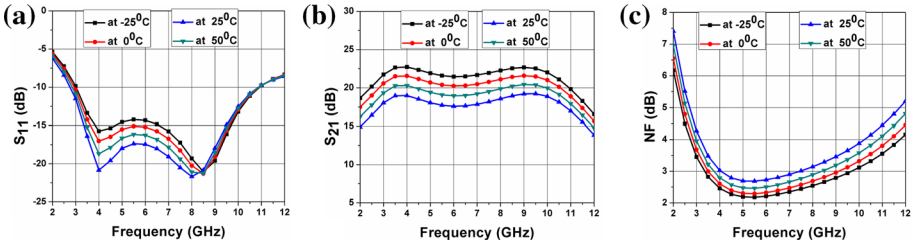

Fig. 11 Simulation results for temperature variations, **a** S_{11} vs Frequency, **b** S_{21} vs Frequency and **c** *NF* vs Frequency

in common- gate stage, the group delay of the proposed LNA is not constant, but still it is comparable with LNAs reported in [19–21], i.e., 190 ± 110 psec, ±28 psec, and ±115 psec, respectively.

Beyond the NF, S-parameters, and linearity, the designed LNA should also have unconditional stability throughout the frequency of interest. The stability of an LNA can analyzed using stability factor (K) and can be expressed [18]

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} > 1 \quad \text{and} \quad |\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{38}$$

The stability factor (K) was greater than 18.67 and delta was ranging from 0.04 to 0.21, as shown in Fig. 9b, which confirms the unconditional stability of the proposed LNA in 3.1–10.6 GHz UWB frequency.

In order to analyze the effect of process and temperature variations on S_{11}, S_{21} and *NF*, the designed LNA was simulated at nominal-nominal (NN), slow-slow (SS) and fast–fast (FF) process corner and different temperatures ranging from −25 to 50 °C. It has been observed from Fig. 10 that, S_{11} was less than −9.5 dB, S_{21} was greater than 13.5 dB and *NF* was less than 5.2 dB for all the given process corners. Simulation results for temperature variations on performance parameters is shown in Fig. 11 and it has observed that, S_{11}, S_{21}, and NF was ranging from −21.67 to −10 dB, 17.59 dB–22.73 dB and 2.17 dB–4.2 dB respectively for 3.1–10.6 GHz frequency range. The chip layout diagram of the proposed LNA is shown in Fig. 12. In chip layout, metal-1 layer having width and spacing of 5 µm

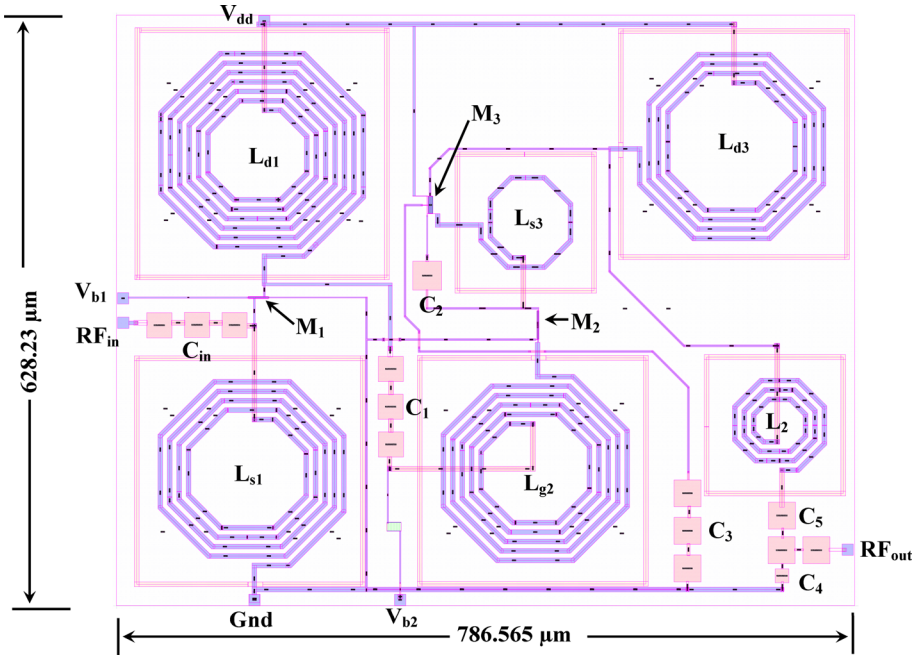

Fig. 12 Chip layout of the proposed LNA design

has been used for designing of all inductors. The Q-factor of inductors used was considered in the range of 0.8–1.2 to ensure wide-bandwidth. Capacitors have been designed using metal–insulator–metal (MIM) for which metal-2 and metal-3 layers have been considered and the biasing resistor R_1 has been design n-diffusion layer to reduce overall chip area. The chip layout has dimension of 628.23 µm × 786.565 µm with an overall area of 0.4941 mm^2.

In order to evaluate and compare overall performance the proposed LNA with existing LNA circuits, a scalar quantity figure-of-merit (*FOM*) has been used. *FOM* can provide direct view regarding the quality of LNA designed because LNA described in different literatures have different circuits, bandwidth, noise figure and other related parameters. The figure-of-merit can be expressed as [4, 20–24]

$$FOM\left[GHz/mW\right] = \frac{\left|S_{21}\right|_{abs} \times BW_{GHz}}{(F-1) \times P_{mW}} \tag{40}$$

where it includes absolute value of S_{21} ($|S_{21}|_{abs}$), 3-dB bandwidth in GHz (BW_{GHz}), Noise factor (F) and power consumption (P_{mW}). The *FOM* of LNA reported in this was 36 GHz/mW which is better than the other reported LNAs in the literature. The performance of the proposed common gate, current-reused UWB LNA is compared with the previously reported LNAs, in Table 2, showing the advantages of the proposed LNA in terms of flat gain, low noise figure and low power consumption.

Table 2 Performance comparison of the propose LNA with previous works

Ref. & Year	Architecture	Tech (nm)	VDD (V)	BW (GHz)	S11 (dB)	S21 (dB)	S22 (dB)	NF (dB)	P1dB (dBm)	IIP3 (dBm)	Power (mW)	FOM (GHz/mW)
This work	CS Current reused	90	0.7	3.1–10.6	<-10.6	20 ± 0.8	<-6.2	2.3–3.7	−17	−8@ 6 GHz	5.05	36
[10], 2011	CS Current reused	90	1.2	2.6–10.2	−9	12.5	–	3–7	−12	–	7.2	–
[27], 2017	CS current reuse	90	1	3.1–10.6	<-9	20.10	–	1.2*	–	−4.22	11.52	17.69
[25], 2009	CS current reuse	130	1.4	2–9	<-10 @ 1–14.6 GHz	11.5 ± 1 @ 2–9 GHz	<-10 @1–14.2	4.45–9 @ 3–10 GHz	–	–	17	–
[23], 2015	CG current reuse with noise cancelling	130	1.3	2.35–9.37	≤-8	10.3$^{\$}$	≤-8	3.68*	−12.55	−4	9.97	5.71
[22], 2013	CS Current reused	180	1.5	3.1–10.6	<-10	9.7$^{\$}$	<-12	4.2*	–	−8.5	11	4.06
[26], 2007	CS Current Reuse	180	1.8	3.1–10.6	<-8	13.5–16	–	3.1–6	–	−7 @ 6 GHz	11.9	–
[24], 2018	CS current reuse and noise cancelling	180	1.8	3–12	<-10	19.24–20.24	–	1.72–1.99	–	−5.5	23.23	7.1

*Minimum, $^{\$}$Maximum, ^{a}Average value, ^{e}Estimated

5 Conclusions

This paper presents a design of common-gate, low power, and low noise amplifier for wireless applications using 90 nm CMOS process. It utilizes common-gate at the input stage to achieve ultra-wideband input-matching and cascaded with common-source current-reused stage to achieve low noise figure throughout UWB. Due to the current-reused topology it achieves a high and flat S_{21} of 20 ± 0.8 dB, with a low noise figure of 2.3–3.7 dB for 3.1–10.6 GHz frequency. The LNA has S_{11} less than -10.6 dB for complete UWB range and achieves input 1-dB compression point of -17 dBm at 6 GHz and input third order intercept point of -8 dBm, while dissipating 5.05 mW of power from a 0.7 V supply. This proves the proposed LNA design as a good solution for the UWB wireless applications.

References

1. FCC. (2002). Revision of part 15 of the commission's rules regarding ultra-wide-band transmission system. Technical Report, ET-Docket (pp. 98–153).
2. Larson, L. E. (1998). Integrated circuit technology for RFICs—Present status and future directions. *EEE Journal of Solid-State Circuits*, *33*(3).
3. Arshad, S., Zafar, F., Ramzan, R., & Wahab, Q. (2013). Wideband and multiband CMOS LNAs: State-of-the-art and future prospects. *Microelectronics Journal, 44*(9), 774–786.
4. Chen, H. K., Chang, D. C., Juang, Y. Z., & Lu, S. S. (2007). A compact wideband CMOS low noise amplifier using shunt resistive feedback and series inductive peaking techniques. *IEEE Microwave and Wireless Components Letters, 17*(8), 616–618.
5. Wei, M. D., Chang, S. F., & Negra, R. (2014). Triple cascaded current-reuse low noise amplifier. *Analog Integrated Circuits and Signal Processing, 80,* 327–333. https://doi.org/10.1007/s10470-014-0334-9
6. Singh, V., Arya, S. K., & Kumar, M. (2018). Gm-boosted current-reuse inductive-peaking common source LNA for 3.1–10.6 GHz UWB wireless applications in 32 nm CMOS. *Analog Integrated Circuits and Signal Processing, 97,* 351–363.
7. Meaamar, A., Boon, C. C., Yeo, K. S., & Do, M. A. (2010). A wideband low power low-noise amplifier in CMOS technology. *IEEE Transactions on Circuits and Systems I: Regular Papers, 57,* 773–782.
8. Chen, M., & Lin, J. (2009). A 0.1–20 GHz low-power self-biased resistive-feedback LNA in 90 nm digital CMOS. *IEEE Microwave and Wireless Components Letters, 19,* 323–325.
9. Nakhlestani, A., Hakimi, A., & Movahhedi, M. (2012). A novel configuration for UWB LNA suitable for low-power and low-voltage applications. *Microelectronics Journal, 43,* 444–451.
10. Sapone, G., & Palmisano, G. (2011). A 3–10-GHz low-power CMOS low-noise amplifier for ultra-wideband communication. *IEEE Transactions on Microwave Theory and Techniques, 59*(3), 678–686.
11. Nieuwoudt, A., Ragheb, T., Nejati, H., & Massoud, Y. (2009). Numerical design optimization methodology for wideband and multi-band inductively degenerated cascode CMOS Low noise amplifiers. *IEEE Transactions On Circuits And Systems—I: Regular Papers, 56*(6), 1088–1101.
12. Guan, X., & Nguyen, C. (2006). Low-power-consumption and high-gain CMOS distributed amplifiers using cascade of inductively coupled common-source gain cells for UWB systems. *IEEE Transactions On Microwave Theory And Techniques, 54*(8), 3278–3283.
13. Machiels, B., Reynaert, P., & Steyaert, M. (2010). Power efficient distributed low noise amplifier in 90 nm CMOS. *IEEE International Symposium on Radio Frequency Integrated Circuits*. https://doi.org/10.1109/rfic.2010.5477322
14. Mæland, K., Kjelgård, K. G., & Lande, T. S. (2015). CMOS distributed amplifiers for UWB radar. *IEEE International Symposium on Circuits and Systems*. https://doi.org/10.1109/iscas.2015.7168879
15. Shen, M., Tong, T., Mikkelsen, J. H., Jensen, O. K., & Larsen, T. (2011). Design and implementation of a 1–5 GHz UWB low noise amplifier in 0.18 µm CMOS. *Analog Integrated Circuits and Signal Processing, 67,* 41–48. https://doi.org/10.1007/s10470-010-9508-2
16. Woo, S., Shao, J., & Kim, H. (2014). A gm-boosted common-gate CMOS low-noise amplifier with high P1dB. *Analog Integrated Circuits and Signal Processing, 80,* 33–37. https://doi.org/10.1007/s10470-014-0306-0

17. Cen, M., & Song, S. (2014). A high gain, low-power low-noise amplifier for ultra-wideband wireless systems. *Circuits, Systems, and Signal Processing, 33,* 3251–3262. https://doi.org/10.1007/s00034-014-9801-x
18. Razavi, B. (2013). *RF microelectronics* (2nd ed.). London: Pearson Education.
19. Lee, J.-Y., Park, H.-K., Chang, H.-J., & Yun, T.-Y. (2012). Low-power UWB LNA with common-gate and current-reuse techniques. *IET Microwaves, Antennas & Propagation, 6*(7), 793–799. https://doi.org/10.1049/iet-map.2011.0415
20. Pandey, S., & Singh, J. (2015). A low power and high gain CMOS LNA for UWB applications in 90nm CMOS process. *Microelectronics Journal, 46*(5), 390–397.
21. Pandey, S., Gawande, T., & Kondekar P. N. (2018). A 3.1–10.6 GHz UWB LNA based on self cascode technique for improved bandwidth and high gain. *Wireless Personal Communications*. https://doi.org/10.1007/s11277-018-5795-1
22. Hsu, M.-T., Chang, Y.-C., & Huang, Y.-Z. (2013). Design of low power UWB LNA based on common source topology with current-reused technique. *Microelectronics Journal, 44,* 1223–1230.
23. Arshad, S., Ramzan, R., Muhammad, K., & Wahab, Q. (2015). A sub-10mW, noise cancelling, wideband LNA for UWB applications. *International Journal of Electronics and Communications, 69*(1), 109–118. https://doi.org/10.1016/j.aeue.2014.08.002
24. Hayati, M., Cheraghaliei, S., & Zarghami, S. (2018). Design of UWB low noise amplifier using noise-canceling and current-reused techniques. *Integration the VLSI Journal, 60,* 232–239.
25. Taris, T., Majek, C., Deval, Y., & Begueret, J.-B. (2009). Current reuse topology in UWB CMOS LNA. *Analog Integrated Circuits and Signal Processing, 61,* 149–158.
26. Lin, Y.-J., Hsu, S. S., Jin, J.-D., & Chan, C. Y. (2007). A 3.1–10.6 GHz ultra-wideband CMOS low noise amplifier with current-reused technique. *IEEE Microwave and Wireless Components Letters, 17*(3), 232–234.
27. Pandey, S., Gawande, T., & Kondekar, P. N. (2017). A 0.9 V, 4.57 mW UWB LNA with improved gain and low power consumption for 31–106 GHz ultra-wide band applications. *Wireless Personal Communications*. https://doi.org/10.1007/s11277-017-4185-4

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