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A Non-Inverting High Gain DC-DC Converter With Continuous Input Current

ARSHAD MAHMOOD[1], MOHAMMAD ZAID[1], (Member, IEEE), JAVED AHMAD[2], MOHD ANAS KHAN[1], SHAHRUKH KHAN[1], (Student Member, IEEE), ZAID SIFAT[1], CHANG-HUA LIN[2], (Member, IEEE), ADIL SARWAR[1] (Senior Member, IEEE), MOHD TARIQ[1], (Senior Member, IEEE), AND BASEM ALAMRI[3], (Member, IEEE)

[1]Department of Electrical Engineering, ZHCET, Aligarh Muslim University, Aligarh 202002, India
[2]Department of Electrical Engineering, National Taiwan University of Science and Technology, Taipei 10607, Taiwan
[3]Department of Electrical Engineering, College of Engineering, Taif University, Taif 21944, Saudi Arabia

Corresponding authors: Mohammad Zaid (mohammad.zaid@zhcet.ac.in) and Mohd Tariq (tariq.ee@zhcet.ac.in)

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ABSTRACT High gain DC-DC converters are increasingly being used in solar PV and other renewable generation systems. Satisfactory steady-state and dynamic performance, along with higher efficiency, is a pre-requirement for selecting the converter for these applications. In this paper, a non-inverting high gain DC-DC boost converter has been proposed. The proposed converter has only one switch with continuous input current and reduced voltage stress across switching devices. The operating range of the duty cycle is wider, and it obtains a higher gain at a lower value of the duty cycle. Moreover, the converter has higher efficiency at a lower duty cycle while drawing a continuous input current. The continuous input current is a desirable feature of the dc-dc converter making it suitable for solar photovoltaic applications. The converter's operation has been discussed in detail and extended to include the real circuit parameters for a practical performance evaluation. The proposed converter has been compared with other similar recently proposed converters on various performance parameters. The loss analysis for the proposed converter has also been carried out. Finally, the simulation has been validated with results from the experimental prototype.

INDEX TERMS Continuous conduction mode, duty cycle, high gain, DC-DC boost converter, voltage stress.

I. INTRODUCTION

For sustainable development, renewable energy is going to play a significant role in energy generation. The generation of electricity by solar PV system for grid-connected and off-grid application has already proven to be the game-changer in the energy market scenario [1]–[3]. While the transportation system is also seeing a shift, with electric vehicles promising to be the future's commutation system. Fuel cells are increasingly being used for electric transportation system [4]. However, both solar PV and fuel cells produce low voltage which is required to be boosted up for practical applications [5]. Therefore, a high voltage gain DC-DC converter is an integral part of the solar PV generation and electric vehicle system. Boost DC-DC converters are also used high-intensity headlamps in automobiles, uninterruptible power supply, motor drives, and many others [6]–[9]. Power converters are used for applications ranging from few watts in a smart battery charging system to hundreds of kilowatts in a converter station in an HVDC transmission system.

The conventional boost converter is not suitable for a very high voltage gain as it achieves high voltage gain at a high value of the duty cycle. A higher value of duty cycles mounts the problems for transient response [10], [11]. And Another demerit of the converter's operation at extreme duty cycle is that enough time is not provided to transfer the stored energy of inductor and capacitor for a diode with reverse recovery time [12]. The conventional boost converter (CBC) is reduced significantly at higher duty ratios because of voltage drops across diodes, switches, and equivalent series resistance of capacitors and inductors [13]. The converter's efficiency depends on the number of the components present in the circuit, their conduction time as well as on switching frequency [14].

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Several topologies of DC-DC converter with isolation using high-frequency transformer are proposed in the literature. High voltage gain is achieved by raising the transformer's turn ratio but due to the transformer the cost, size, and weight of the converter increases. Moreover, transformers also introduce non-idealities in the system. Sometimes the leakage inductance of coupled inductor can also create a problem of current transients through the switch [15], [16]. High voltage gain could be achieved using coupled inductors, but a clamp circuit needs to be designed [17], [18]. The converter efficiency can decrease in the two-stage operation of the converters with coupled inductor because of reverse recovery issues and leakage inductance if the energy stored in the leakage inductance is not properly utilized [19].

Two or more converters can be connected in series to achieve a high voltage gain, but this increases the number of passive components in the circuit. The converter's operation with a large number of components at an extreme duty ratio increases the power loss, which is not appreciable [10], [20], [22]. In [22] switched inductors and capacitors are used to synthesize new hybrid converters. Switched capacitors topologies although draws higher current in charging the capacitors are more popular than switched inductor topologies owing to small size and better voltage gain. In [23], two converters are cascaded which has a quadratic gain slightly greater than that of the conventional quadratic boost. The converter proposed by Fardoun and Ismail [24] has a single switch with two inductors, and that has extended from the relief circuit [25]. The converter has a high voltage gain but also has high voltage stress on the switches. In [26], authors have proposed a single switch quadratic voltage gain converter is proposed, but inductor counts are more, and voltage stress on the switch is the same as output voltage. A schematic diagram that shows the application of DC-DC converter in DC Microgrid is shown in Figure 1.

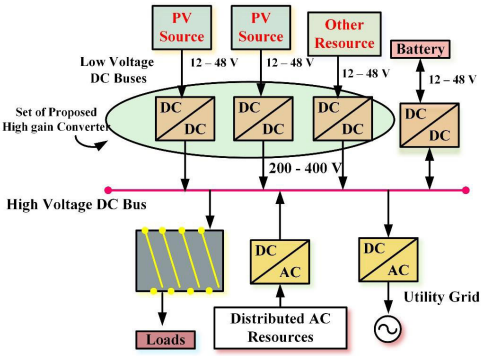

FIGURE 1. Simple Schematic of DC Microgrid.

This paper analyzes a converter topology with high gain using a single switch and comparatively low voltage stresses across the switch and other power components. The key features of the proposed converter are

(i) Voltage gain is more than twice as compared with a conventional quadratic boost converter and twice quadratic boost converter presented in [26]

(ii) Coupled inductor is not used to increase the gain hence the problems caused due to leakage inductance are not there.

(iii) Only one switch is used and hence control is easy.

(iv) Input current is continuous with low ripple that reduces the cost of input filter.

The converter can be operated with a wide range of duty ratios avoiding operation at extreme duty ratio, and hence there is no problem related to reverse recovery time for diodes in the proposed converter. This converter has comparatively more components, but its voltage gain is high and input current is continuous. The circuits of the conventional boost converter and twice the quadratic boost converter [26] are shown in Figure. 2(a) and 2(b) respectively. It can be seen that these converters utilize two and three inductors respectively but still their voltage gain is less than the proposed topology. The schematic of the proposed converter topology is shown in Figure 2(c). The absence of common ground is one of the disadvantages of the converter. However, the proposed converter can be interfaced with solar PV by removing the voltage multiplier circuit used in the converter as shown in Figure 2(c) or by adding other existing multipliers with common ground. This paper is outlined as follows:

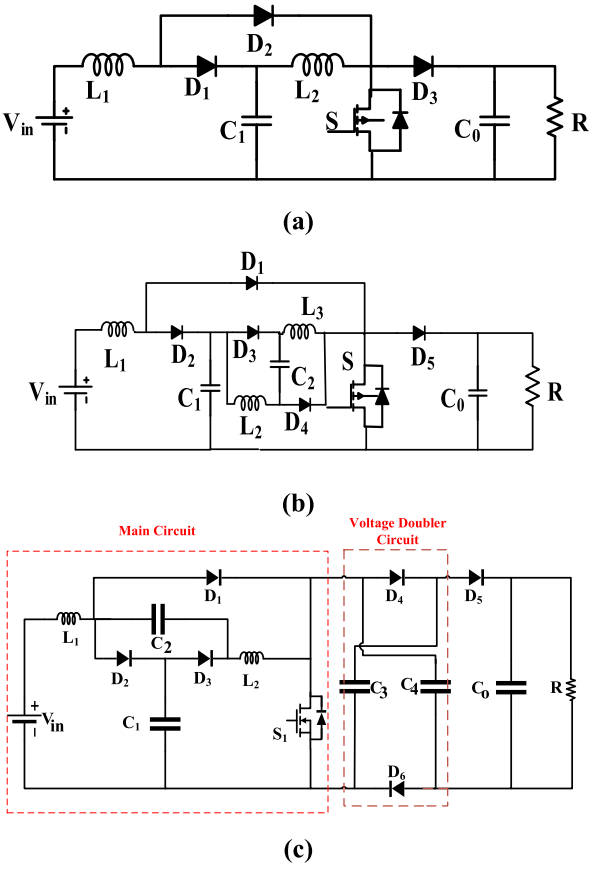

FIGURE 2. (a) Conventional Quadratic Boost Converter (CQBC) (b) Proposed Converter in [26] (c) Proposed Converter.

In section II, circuit description, working, and mode of operation for the proposed converter are detailed in CCM. Further, in section II itself, design parameters like the value of inductances and capacitances are also calculated. Section III has a comparison of this converter among similar converters. Section IV describes the power loss analysis of the converter. Section V shows the simulation and experimental results. The conclusion is discussed in section VI.

II. PROPOSED CONVERTER

A. CIRCUIT DETAILS

The conventional quadratic boost is shown in Figure. 2(a) with two inductors. Proposed converter [26] in Figure. 2(b) uses a voltage multiplier to boost the voltage to achieve voltage gain of twice the quadratic boost converter with three inductors. The proposed converter consists of two inductors but with an advantage greater than the aforementioned converters. The presented converter in Figure 2(c) includes single switch S_1, two inductors L_1 and L_2, five capacitors named C_1, C_2, C_3, C_4 and C_0 and six diodes specified as D_1, D_2, D_3, D_4, D_5, and D_6 and load R. All capacitances and inductances are taken as large for analysis so that voltage across capacitors and current through inductors are constant. The converter has two operating states within one switching Period T_s. All analysis is done in CCM mode; therefore, a continuous input current is assumed. The considerations taken to analyze the circuit operations in equilibrium are as follows:

- All components are ideal; therefore, no loss takes place.
- The switching period is constant.

B. MODES OF OPERATION

The circuit is analyzed in two modes: the first one has been analyzed during switch ON, and the second one is during switch off. Both modes of the circuit are shown in Figure 4. And some graphs related to converter such as diode voltage V_{D1}, inductor current I_{L1}, I_{L2}, and so more are in Figure 3. In the graph, the interval t_o-t_1 is the ON period, and t_1-t_2 is the OFF period.

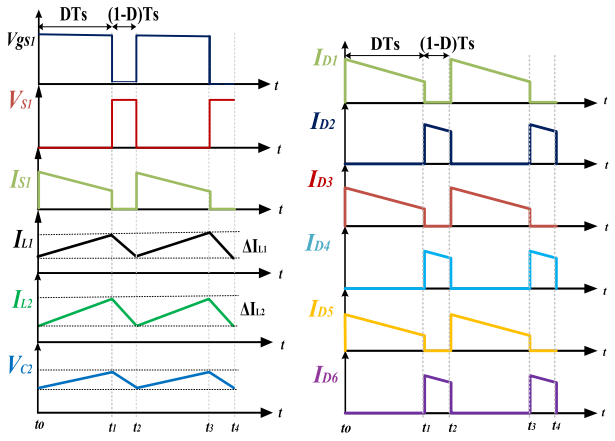

FIGURE 3. Waveforms associated with the converter in CCM.

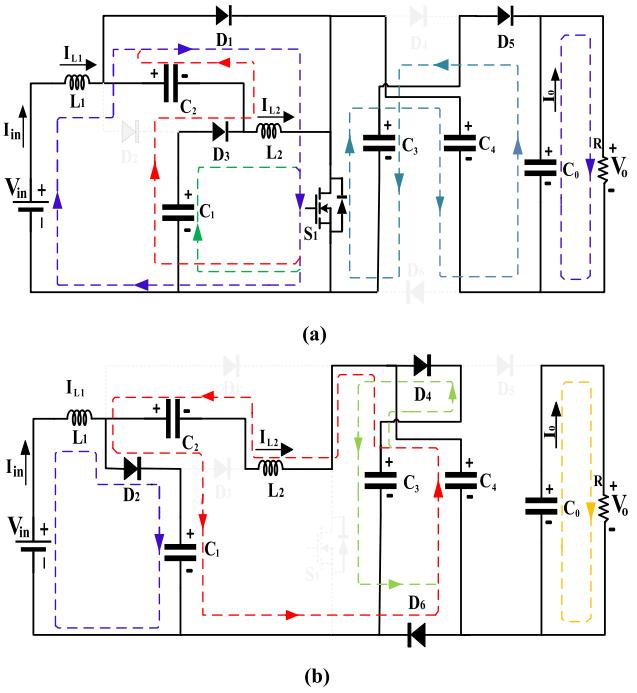

FIGURE 4. Modes of operations for the proposed converter (a) when thw switch is ON (b) when the switch is OFF.

C. MODE I: WHEN SWITCH IS ON($t_0 < t < t_1$)

During switch ON, D_1, D_3, and D_5 are forward biased while D_2, D_4, and D_6 are reversed biased. The equivalent circuit is depicted in Figure 4(a). In this interval, inductor currents I_{L1} and I_{L2} rise to the peak value at the same time, and it means that inductors store the energy. During this interval, capacitor C_1, C_3, and C_3 are transferring their energy to the inductor L_2 and load, respectively. Using basic laws of KVL and KCL derived voltages, and currents relations are:

$$\begin{cases} V_{L1} = L_1 \dfrac{dI_{L1}}{dt} = V_{in} \\ V_{L2} = L_2 \dfrac{dI_{L2}}{dt} = V_{C1} \\ C_1 \dfrac{dV_{C1}}{dt} = I_{C1} = I_{C2} - I_{L2} \\ C_2 \dfrac{dV_{C2}}{dt} = I_{C2} \\ C_3 \dfrac{dV_{C3}}{dt} = C_4 \dfrac{dV_{C4}}{dt} = I_{C3} = I_{C4} \\ C_0 \dfrac{dV_{C6}}{dt} = I_{C0} = I_{C3} - I_o \\ V_0 = V_{C3} + V_{C4} \\ V_{C1} = -V_{C2} \end{cases} \tag{1}$$

D. MODE I: WHEN SWITCH IS OFF($t_1 < t < t_2$)

As shown in Figure 4(b), D_2, D_4, and D_6 are forward biased while D_1, D_3, and D_5 are reversed biased during switch OFF. In this interval, inductor currents I_{L1} and I_{L2} decrease simultaneously, and they transfer their energy to capacitor C_1, C_3, and C_4. Capacitor C_o discharges and feeds the load.

Derived voltages and currents are as follows:

$$\begin{cases} V_{L1} = L_1 \dfrac{dI_{L1}}{dt} = V_{in} - V_{C1} \\ V_{L2} = L_2 \dfrac{dI_{L2}}{dt} = V_{C1} - V_{C2} - V_{C3} \\ C_1 \dfrac{dV_{C1}}{dt} = I_{C1} = I_{L1} - I_{L2} \\ C_2 \dfrac{dV_{C2}}{dt} = I_{C2} = I_{L2} \\ C_3 \dfrac{dV_{C3}}{dt} + C_4 \dfrac{dV_{C4}}{dt} = I_{C3} + I_{C4} = I_{L2} \\ C_0 \dfrac{dV_{C0}}{dt} = I_{C0} = -I_o \\ V_{C4} = V_{C5} \end{cases} \tag{2}$$

E. VOLTAGE GAIN(M) CALCULATION

At the steady-state, the average voltage across an inductor is zero. Applying the volt-second balance principle on L_1 and L_2 using results from (1) and (2) and get results as follows:

$$DV_{in} + (1-D)(V_{in} - V_{C1}) = 0 \tag{3}$$

$$DV_{C1} + (1-D)(V_{C1} - V_{C2} - V_{C3}) = 0 \tag{4}$$

Using (1), (2), (3), and (4), the following results come out:

$$\begin{cases} V_{C1} = \dfrac{V_{in}}{1-D} \\ V_{C1} = \dfrac{(1-D)V_o}{2(2-D)} \end{cases} \tag{5}$$

And finally, using (5) voltage gain for converter comes out as follows:

$$M = \frac{V_o}{V_{in}} = \frac{2(2-D)}{(1-D)^2} \tag{6}$$

F. VOLTAGE AND CURRENT STRESSES OF POWER DEVICES

The switch and other components' voltage stress means that the voltage appeared on the switch and the other components when that particular components are OFF. The voltage stresses across switch S_1 and all diodes D_1, D_2, D_3, D_4, and D_5 are mentioned below:

$$\begin{cases} V_{S1} = \dfrac{(2-D)V_{in}}{(1-D)^2} = \dfrac{V_o}{2}, V_{D1} = \dfrac{V_o}{2(2-D)} \\ V_{D2} = \dfrac{(1-D)V_o}{2(2-D)}, V_{D3} = \dfrac{(1-D)V_o}{2(2-D)} \\ V_{D4} = V_{D5} = V_{D6} = \dfrac{V_o}{2} \end{cases} \tag{7}$$

Assuming a lossless circuit, ideally, input power is delivered to the load entirely. Hence,

$$\begin{cases} P_{in} = P_{out} \\ V_{in} I_{in} = V_o I_o \\ \dfrac{I_{in}}{I_0} = \dfrac{V_0}{V_{in}} = M = \dfrac{2(2-D)}{(1-D)^2} \end{cases} \tag{8}$$

It is clear from Figure 3 that

$$I_{L1} = I_{in}$$

Hence, from (8)

$$I_{L1} = \frac{2(2-D)}{(1-D)^2} I_O \tag{9}$$

Applying ampere-second balance on C_1 and C_2 to get average current through inductor L_2:

$$I_{C1_{on}} D + I_{C1_{off}} (1-D) = 0$$

And

$$I_{C2_{on}} D + I_{C2_{off}} (1-D) = 0$$

Using current equations from (1) and (2), I_{L2} can be extracted as shown in Equation (10).

$$I_{L2} = \frac{2I_0}{(1-D)} \tag{10}$$

Similarly, applying ampere-second balance on C_1 and C_4 to get current through inductor I_S:

$$I_s = \frac{(3-D^2)I_o}{(1-D)^2} \tag{11}$$

Similarly, the current through all diodes can be drawn out as follows:

$$\begin{cases} I_{D1} = \dfrac{2I_o}{(1-D)^2} \\ I_{D2} = \dfrac{2I_o}{(1-D)}, I_{D3} = \dfrac{2I_o}{(1-D)} \\ I_{D4} = I_{D5} = I_{D6} = I_o \end{cases} \tag{12}$$

G. DESIGN PARAMETERS

1) DUTY CYCLE CALCULATION

To obtain the desired output voltage at the given input voltage, duty cycle D can be calculated. From (6), the duty cycle is:

$$D = \frac{V_0 - V_{in} + \sqrt{V_{in}(V_{in} + 2V_o)}}{V_o} \tag{13}$$

2) COMPONENT DESIGN

For a given suitable value of ripple of inductor currents ΔI_{L1} and ΔI_{L2} at a fixed value of switching frequency f_s for this converter, inductances can be extracted from (1) as:

$$\begin{cases} L_1 = \dfrac{V_{in} D T_s}{\Delta I_{L1}} = \dfrac{V_{in} D}{\Delta I_{L1} f_s} \\ L_2 = \dfrac{V_{in} D T_s}{(1-D)\Delta I_{L2}} = \dfrac{V_{in} D}{(1-D)\Delta I_{L2} f_s} \end{cases} \tag{14}$$

Moreover, within the valid range of voltage ripple value of capacitances can be calculated from (2) as:

$$\begin{cases} C_1 = \dfrac{2V_o D}{(1-D) R \Delta V_{C1} f_s} \\ C_2 = \dfrac{2DV_o}{(1-D) R \Delta V_{C2} f_s} \\ C_3 = \dfrac{DV_o}{R \Delta V_{C4} f_s} \\ C_4 = \dfrac{DV_o}{R \Delta V_{C5} f_s} \\ C_0 = \dfrac{(1-D)V_o}{R \Delta V_{C4} f_s} \end{cases} \tag{15}$$

For a specific value of D, f_s, V_o, V_{in}, R and suitable current and voltage ripples, convenient inductors and capacitors can be chosen.

H. BOUNDARY CONDITION

For continuous conduction mode of operation, the minimum current in each inductor should be greater than zero. And therefore, the minimum inductance required for both the inductors are calculated as follows

$$\begin{cases} I_{L1} = \dfrac{2(2-D)}{(1-D)^2} I_o \\ \Delta I_{L1} = \dfrac{V_{in} D}{L_1 f_s} \\ I_{L1min} = I_{L1} - \dfrac{\Delta I_{L1}}{2} \\ L_1 \geq \dfrac{D(1-D)^4 R}{8(2-D)^2 f_s} \end{cases} \tag{16}$$

$$\begin{cases} I_{L2} = \dfrac{2I_0}{(1-D)} \\ \Delta I_{L2} = \dfrac{V_{in} D}{(1-D) L_2 f_s} \\ I_{L2min} = I_{L2} - \dfrac{\Delta I_{L2}}{2} \\ L_2 \geq \dfrac{D(1-D)^2 R}{8(2-D) f_s} \end{cases} \tag{17}$$

Defining normalized inductor time constant for inductor L_2

$$\tau = \frac{8 L_2 f_s}{R} \tag{18}$$

Using (17) the boundary normalized inductor time constant τ_B can be expressed as

$$\tau_B = \frac{D(1-D)^2}{(2-D)} \tag{19}$$

To operate in continuous conduction mode τ must be greater than τ_B otherwise, it operates in a discontinuous conduction mode of operation. In other words,

$$\begin{cases} \tau > \tau_B; \text{ Continuous conduction mode(CCM)} \\ \tau < \tau_B; \text{ Discontinuous conduction mode (DCM)} \\ \tau = \tau_B; \text{ Boundary mode} \end{cases}$$

The converter may operate in different region depending upon the condition as shown in Figure 5. It should be noted that switching frequency is constant for both CCM and BCM.

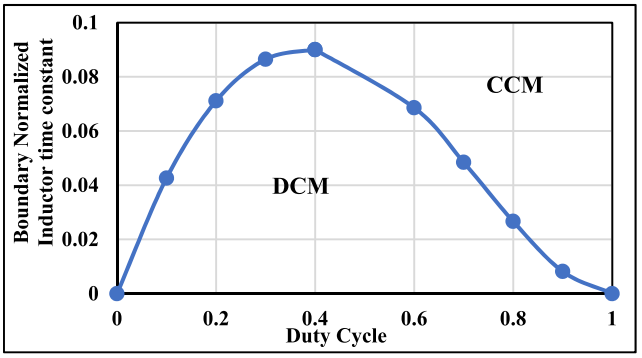

FIGURE 5. Boundary normalized inductor time constant vs duty cycle.

III. COMPARISON AMONG OTHER SIMILAR HIGH GAIN BOOST CONVERTER

The proposed converter's features with other similar high gain DC-DC boost converters are listed in Table 1. Comparative analysis of the proposed converter is based on the following: the number of components, voltage gain, and voltage stress of switch. The proposed converter provides 2(2-D) times of CQBC (Conventional Quadratic Boost Converter) utilizing only a single switch and two inductors. The converter introduced in Lee and Do [17] provides the gain (at turn ratio n = 1 to 2) lower than the proposed converter while one inductor and one coupled inductor are brought into service, and as a result voltage stress across the switch is higher than the proposed topology. The converters detailed in Pires *et al.* [23], Fardoun and Ismail [24] and Mohamed and

TABLE 1. Comparison among other high gain DC-DC converters.

TOPOLOGY	Number of Switch	Number of Inductors	Number of Diodes	Number of Capacitors	The voltage stress on the switch (V_S/V_{in})	Voltage Gain (M)	Voltage gain at D = 0.5
Proposed	1	2	6	5	$\frac{(2-D)}{(1-D)^2}$	$\frac{2(2-D)}{(1-D)^2}$	12
[17]	1	1+1 coupled inductor	5	3	$\frac{3}{1-D}$	$\frac{(3-D)}{(1-D)^2}$, n = 2	10
[23]	1	2	4	5	$\frac{1}{(1-D)^2}$	$\frac{1+D}{(1-D)^2}$	6
[24]	1	2	5	4	$\frac{4}{1-D}$	$\frac{3+D}{1-D}$	7
[26]	1	3	5	3	$\frac{2}{(1-D)^2}$	$\frac{2}{(1-D)^2}$	8
[27]	1	2	5	4	$\frac{1}{(1-D)^2}$	$\frac{2-D}{(1-D)^2}$	6
[28]	6	6	14	8	$\frac{1}{1-D}$	$\frac{3+D}{1-D}$	7
[29]	2	4	9	1	$S_1 = \frac{1+D}{1-D}, S_2 = \frac{2D}{1-D}$	$\frac{1+3D}{1-D}$	5

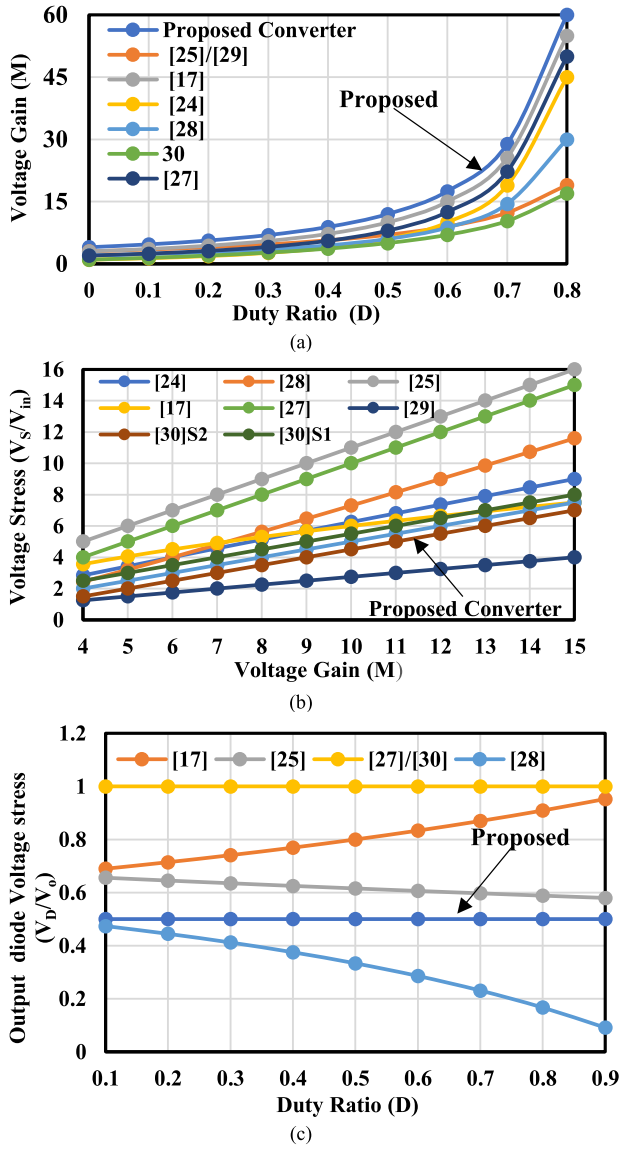

FIGURE 6. Comparison (a) Voltage gain vs duty ratio (b) Voltage stress vs Voltage Gain (c) Output diode voltage stress (V_D/V_0) vs duty ratio.

Fardoun [27] utilize the same number of inductor and switch as proposed one but voltage gains of the converters are low and voltage stress on the switches are higher than the proposed converter. The converter analyzed in Javed *et al.* [26] provides a voltage gain of 2 times of CQBC that is lower than the proposed converter and in this converter stress across the switch is the same as that of CQBC. Although this converter brings into service three inductors which makes it heavier. The converters in Maalandish *et al.* [28] and Gupta *et al.* [29] provides very low gain compared to the proposed converter utilizing six inductors, six switches and four inductors, two switches respectively. The voltage stress on the switches in both the converters are lower than the proposed converter but they use more switches which makes its control complex. Voltage gains of all converters listed in Table 1 at a duty ratio of 50% have calculated where it can be seen that the voltage gain of the proposed converter is the highest among listed converter. It should be noted that all comparison is shown in CCM. Figure 6(a) presents the graph of voltage gain versus duty cycle for the converters listed in Table 1, from where it can be analyzed that other converters hold high gain at an extreme duty cycle, but the proposed converter holds that same gain at a lower duty cycle. This is the one advantage of this converter. Figure 6(b) shows the graph of voltage stress on switch versus voltage gain for the listed converters in Table 1 from where it can be observed the voltage stress on the switch of the proposed converter is lower than other listed converters at a particular gain excluding converters proposed in Maalandish *et al.* [28] and Gupta *et al.* [29]. The output diode voltage stress (V_D/V_0) is shown in Figure 6(c) of the listed converter in Table 1. It can be observed that the proposed converter has low diode voltage stress among other converters. Because of low voltage stress across the power devices, the proposed converter can utilize the low rating devices which is helpful to gain high efficiency.

IV. POWER LOSS ANALYSIS OF THE CONVERTER

An equivalent circuit with parasitic resistances of the converter is shown in Figure 7. Where r_{S1} is the MOSFET on-resistance, r_{D1}, r_{D2}, r_{D3}, r_{D4}, r_{D5} and $r_{D6}$are the diode on-resistance, V_F is the diode threshold voltage, r_{L1} and r_{L2} are the ESRs of inductors L_1, and L_2 and r_{C1}, r_{C2}, r_{C3}, r_{C4}, and r_{C0} are the ESRs of capacitors respectively. Conduction losses have calculated assuming that inductors currents are ripple-free, and switching losses are not included.

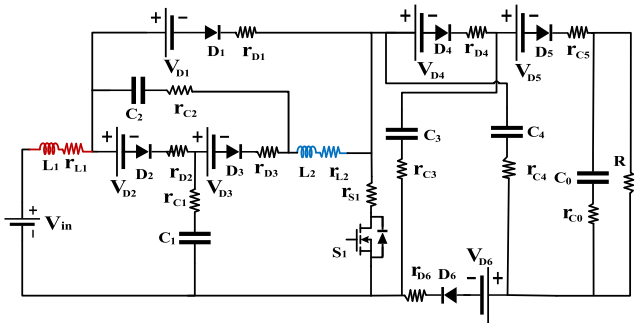

FIGURE 7. Equivalent circuit considering nonidealities.

Since, $P_0 = V_0 I_0 = I_0^2 R$

1) MOSFET CONDUCTION LOSS

$I_{S1,rms}$ is the root mean square value of current passing through switch and P_{rS1} is the power loss due to switch ON-resistance.

$$\begin{cases} I_{S1,rms} = \left(\frac{3-D^2}{\sqrt{D}(1-D)^2}\right) I_0 \\ P_{rS1} = I_{S1,rms}^2 r_{S1} = \left(\frac{(3-D^2)^2}{D(1-D)^4}\right) I_0^2 r_{S1} = \left(\frac{(3-D^2)^2}{D(1-D)^4}\right) \frac{r_{S1}}{R} P_0 \end{cases} \tag{20}$$

2) POWER LOSSES IN DIODES DUE TO ON-RESISTANCE AND FORWARD-VOLTAGE DROPS

$I_{D,rms}$ and I_{D1} are the rms currents and average currents passing through diodes respectively. P_{rD} is the power loss in

converter due to diodes on-resistance and P_{V_F} is the loss due to forward-voltage drop across the diode. These losses are determined as follows.

$$\begin{cases} I_{D1,rms} = \frac{2I_0}{\sqrt{D}(1-D)^2}, I_{D1} = \frac{2I_0}{(1-D)^2} \\ P_{rD1} = I_{D1,rms}^2 r_{D1} = \frac{4I_0^2}{D(1-D)^4} r_{D1} = \frac{4}{D(1-D)^4} \frac{r_{D1}}{R} P_0 \\ P_{V_{F1}} = V_{F1} I_{D1} = \frac{2I_0}{(1-D)^2} V_{F1} = \frac{2}{(1-D)^2} \frac{V_{F1}}{V_0} P_0 \end{cases} \tag{21}$$

$$\begin{cases} I_{D2,rms} = \frac{2I_0}{(\sqrt{1-D})^3}, I_{D2} = \frac{2I_0}{(1-D)} \\ P_{rD2} = I_{D2,rms}^2 r_{D2} = \frac{4I_0^2}{(1-D)^3} r_{D2} = \frac{4}{(1-D)^3} \frac{r_{D2}}{R} P_0 \\ P_{V_{F2}} = V_{F2} I_{D2} = \frac{2I_0}{(1-D)} V_{F2} = \frac{2}{(1-D)} \frac{V_{F2}}{V_0} P_0 \end{cases} \tag{22}$$

$$\begin{cases} I_{D3_{rms}} = \frac{2I_0}{\sqrt{D}(1-D)}, I_{D3} = \frac{2I_0}{(1-D)} \\ P_{rD3} = I_{D3_{rms}}^2 r_{D3} = \frac{4}{D(1-D)^2} I_0^2 r_{D3} = \frac{4}{D(1-D)^2} \frac{r_{D3}}{R} P_0 \\ P_{V_{F3}} = V_{F3} I_{D3} = \frac{2I_0}{(1-D)} V_{F3} = \frac{2}{(1-D)} \frac{V_{F3}}{V_0} P_0 \end{cases} \tag{23}$$

$$\begin{cases} I_{D4,rms} = I_{D6,rms} = \frac{I_0}{\sqrt{1-D}} \\ I_{D4} = I_{D6} = I_0 \\ P_{rD4} = I_{D4,rms}^2 r_{D4} = \frac{I_0^2}{(1-D)} r_{D4} = \frac{1}{(1-D)} \frac{r_{D4}}{R} P_o \\ P_{rD6} = I_{D6,rms}^2 r_{D6} = \frac{I_0^2}{(1-D)} r_{D6} = \frac{1}{(1-D)} \frac{r_{D6}}{R} P_o \\ P_{V_{F4}} = V_{F4} I_{D4} = V_{F4} I_0 = \frac{V_{F4}}{V_0} P_o \\ P_{V_{F6}} = V_{F6} I_{D6} = V_{F6} I_0 = \frac{V_{F6}}{V_0} P_o \end{cases} \tag{24}$$

$$\begin{cases} I_{D5,rms} = \frac{I_0}{\sqrt{D}}, I_{D5} = I_0 \\ P_{rD5} = I_{D5,rms}^2 r_{D5} = \frac{I_0^2}{D} r_{D5} = \frac{1}{D} \frac{r_{D5}}{R} P_o \\ P_{V_{F5}} = V_{F5} I_{D5} = V_{F5} I_0 = \frac{V_{F5}}{V_0} P_0 \end{cases} \tag{25}$$

Following assumptions can be taken:

$$\begin{cases} r_{D1} = r_{D2} = r_{D3} = r_{D4} = r_{D5} = r_{D6} = r_D \\ V_{F1} = V_{F2} = V_{F3} = V_{F4} = V_{F5} = V_{F6} = V_F \end{cases} \tag{26}$$

Hence, total diode losses due to on-resistance and forward-voltage drops can be drawn out using (21), (22), (23), (24), (25), and (26) as follows:

$$\begin{cases} P_{rD} = \left(\frac{(3-D^2)(D^2-2D+3)}{D(1-D)^4} \right) \frac{r_D}{R} P_o \\ P_{V_F} = \left(\frac{3D^2-10D+9}{(1-D)^2} \right) \frac{V_F}{V_0} P_o \end{cases} \tag{27}$$

3) LOSSES IN INDUCTORS DUE TO ESRs

Since it has assumed that inductor currents are ripple-free. Hence, their rms values and average values are equal in magnitude. In equation (28), I_L is the average current through the inductor and P_{rL} is the power dissipation by inductor due to its equivalent series resistance (ESR) as follows.

So, from (9) and (10), the following results can be shown.

$$\begin{cases} I_{L1,rms} = I_{L1} = \frac{2(2-D)I_0}{(1-D)^2} \\ I_{L2,rms} = I_{L2} = \frac{2I_0}{(1-D)} \\ P_{rL1} = I_{L1,rms}^2 r_{L1} = \frac{4(2-D)^2}{(1-D)^4} I_0^2 r_{L1} = \frac{4(2-D)^2}{(1-D)^4} \frac{r_{L1}}{R} P_0 \\ P_{rL2} = I_{L2,rms}^2 r_{L2} = \frac{4}{(1-D)^2} I_0^2 r_{L2} = \frac{4}{(1-D)^2} \frac{r_{L2}}{R} P_0 \end{cases} \tag{28}$$

It can be assumed that,

$$r_{L1} = r_{L2} = r_L$$

Hence, total inductor loss from (28),

$$P_{rL} = \left(\frac{4(2D^2-6D+5)}{(1-D)^4} \right) \frac{r_L}{R} P_0 \tag{29}$$

4) LOSSES IN CAPACITORS DUE TO ESRs

$I_{C,rms}$ is the rms current flowing through capacitor and P_{rC} is the power loss due to equivalent series resistance (ESR) of the capacitor.

$$\begin{cases} I_{C1,rms} = \frac{2}{\sqrt{D}(\sqrt{1-D})^3} I_0 \\ P_{rC1} = I_{C1,rms}^2 r_{C1} = \frac{4}{D(1-D)^3} I_0^2 r_{C1} = \frac{4}{D(1-D)^3} \frac{r_{C1}}{R} P_0 \end{cases} \tag{30}$$

$$\begin{cases} I_{C2,rms} = \frac{2}{\sqrt{D(1-D)}} I_0 \\ P_{rC2} = I_{C2,rms}^2 r_{C2} = \frac{2}{D(1-D)} I_0^2 r_{C2} = \frac{2}{D(1-D)} \frac{r_{C2}}{R} P_0 \end{cases} \tag{31}$$

$$\begin{cases} I_{C3_{rms}} = I_{C4_{rms}} = \frac{1}{\sqrt{D(1-D)}} I_0 \\ P_{rC3} = I_{C3,rms}^2 r_{C3} = \frac{1}{D(1-D)} I_0^2 r_{C3} = \frac{1}{D(1-D)} \frac{r_{C3}}{R} P_0 \\ P_{rC4} = I_{C4,rms}^2 r_{C4} = \frac{1}{D(1-D)} I_0^2 r_{C4} = \frac{1}{D(1-D)} \frac{r_{C4}}{R} P_0 \end{cases} \tag{32}$$

$$\begin{cases} I_{C0,rms} = \left(\frac{\sqrt{1-D}}{\sqrt{D}} \right) I_0 \\ P_{rC0} = I_{C0,rms}^2 r_{C0} = \frac{(1-D)}{D} I_0^2 r_{C0} = \frac{(1-D)}{D} \frac{r_{C0}}{R} P_0 \end{cases} \tag{33}$$

And it is assuming that,

$$r_{C1} = r_{C2} = r_{C3} = r_{C4} = r_{C0} = r_C$$

From (30), (31), (32) and (33), total capacitor losses due to ESRs can be shown as follows:

$$\begin{cases} P_{rC} = \frac{(D^2-2D+3)^2}{D(1-D)^3} \frac{r_C}{R} P_0 \end{cases} \tag{34}$$

From (20), (27), (29) and (34), total losses in the converter can be calculated as follows:

$$P_{loss,total} = P_{rS1} + P_{rD} + P_{V_F} + P_{rL} + P_{rC}$$

Hence,

$$P_{loss,total} = \left[4a\frac{r_L}{R} + b\left(c\frac{r_D}{R} + \frac{r_S}{R} \right) + d\frac{V_F}{V_0} + e\frac{r_C}{R} \right] P_0 \tag{35}$$

where,

$$\begin{cases} a = \dfrac{(2D^2 - 6D + 5)}{(1-D)^4}, b = \dfrac{(3-D^2)^2}{D(1-D)^4} \\ c = \dfrac{(D^2 - 2D + 3)}{(3-D^2)}, d = \left(\dfrac{3D^2 - 10D + 9}{(1-D)^2}\right) \\ e = \dfrac{(D^2 - 2D + 3)^2}{D(1-D)^3} \end{cases}$$

And efficiency,

$$\eta = \frac{1}{1 + \frac{P_{loss,total}}{P_0}}$$

Hence, the efficiency of the converter can be determined using (35) as follows:

$$\eta = \frac{1}{1 + 4a\frac{r_L}{R} + b\left(c\frac{r_D}{R} + \frac{r_S}{R}\right) + d\frac{V_F}{V_0} + e\frac{r_C}{R}} \tag{36}$$

V. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

The parameters used to extract the simulation results using PLECS software are shown in Table 2. From (1) and (2), it has been drawn out theoretically that $V_{C3} = V_o/2$. For input voltage of 24V with 0.3 duty cycle, output voltage V_o is found to be 166V and V_{C3} to 83V. Figure 8 shows the value of inductor currents I_{L1} and I_{L2} along with a gate pulse at a duty cycle of 0.3. It can be seen that inductor currents are continuous and the average values are found to be 5.8A and 2.6A respectively. The ideal output voltage V_o is found to be 166V for a duty ratio of 30% at $V_{in} = 24$ V as shown in Figure 9. It can be inferred that approximately a voltage gain of more than 6.8 times can be achieved at a small duty ratio of 0.3. Practically the voltage gain will be reduced owing to the voltage drop across switch, diodes, capacitors and inductors.

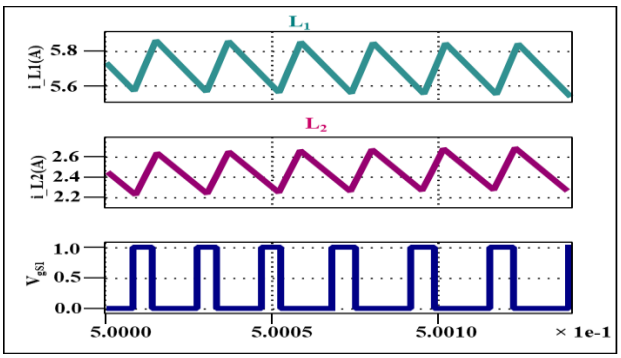

FIGURE 8. Simulated waveforms of I_{L1} and I_{L2} and V_{gS1} at D = 0.3.

It can be observed in Figure 10 that the converter draws a continuous current with low ripple that increases its adaptability into PV systems and fuel cells and that is why this converter reduces the cost of input filter. Figure 11 presents the very low variation in voltage across C_1, C_3, and C_4 having values of 34V, 83V, and 83V respectively. Figure 12 shows

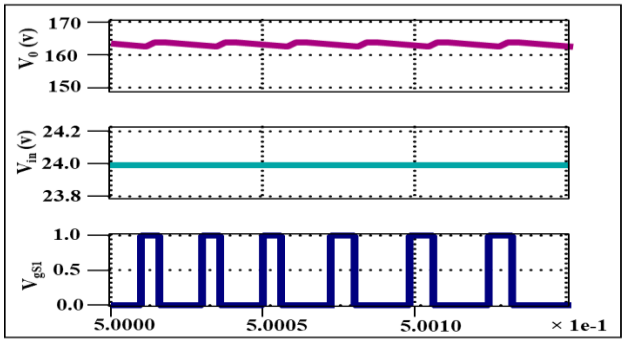

FIGURE 9. Simulated waveforms of V_0 and V_{in} at D = 0.3 with V_{gS1}.

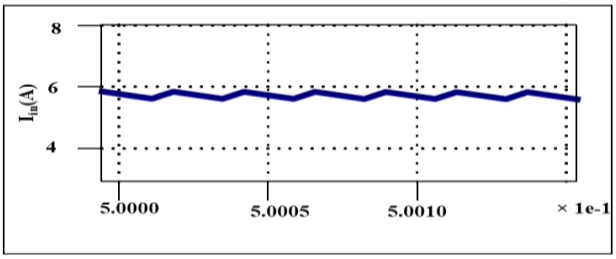

FIGURE 10. Simulated waveforms of input current I_{in} at D = 0.3.

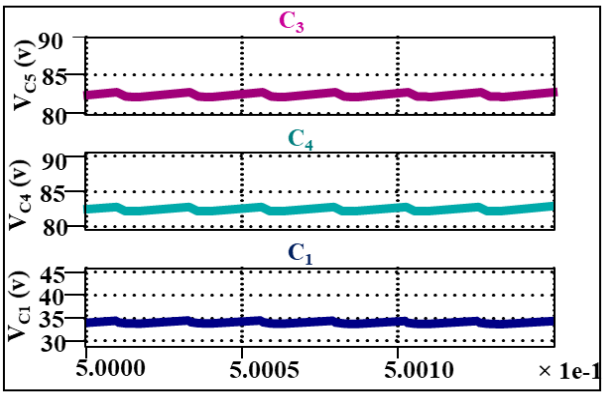

FIGURE 11. Simulated Waveforms of V_{C1}, V_{C3} and V_{C4} at D = 0.3.

the stress on switch S_1 with the value of 83V at V_o of 166V which is far less than V_o. Because of low voltage stress across switch S_1, the proposed converter utilizes a low power rating switch which reduces the loss contribution and increases the efficiency.

Figure 12 presents the voltage across output diode D_5, V_{D5} also having the value of 83V. Voltage appeared across the output diode is half than output voltage V_0 that is advantageous for the converter that it can be operated with low rating power semiconductor devices. Simulation results have drawn out at duty ratio of 30% with source voltage $V_{in} = 24$V having fed to a resistive load of 200 Ω.

B. EXPERIMENTAL RESULTS

A 200W prototype has been developed to evaluate and verify the operation of the converter practically. Design parameters and components are listed in Table 2. The hardware prototype

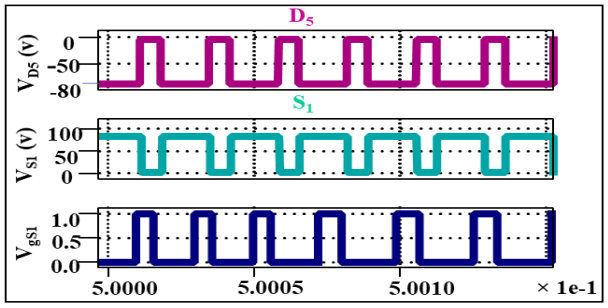

FIGURE 12. Simulated Waveforms of V_{D5}, V_{S1} and V_{gS1} at D = 0.3.

TABLE 2. Experimental parameters.

Elements	Specification
Maximum Power	200 W
Input Voltage	24V
Rated Output Voltage	166V
Switching Frequency	50kHz
Load Resistance	R=200 Ω, Chroma electronic load simulator model 63202
Inductors	L_1=L_2=330µH
Capacitors	C_1=47µF/200V, C_2= 47µF/100V C_3 = C_4 = 47µF/200V & C_O=100µF/250V
Power MOSFET	SPW52N50C3
Diodes	HER806
Gate Drivers IC	TLP250H
Microcontroller	STM32F334R8

is depicted in Figure 13. The proposed converter can be operated with a wide range of duty ratio but since the converter has a quadratic gain, a high voltage gain of more than 15 times can be achieved for D less than 0.5. All experimental results have been provided at a duty ratio of 30%. This duty cycle is just for illustration to validate the theoretical results of the proposed converter, correctly and any other duty cycle can be employed. In Figure. 14, inductor currents I_{L1} and I_{L2} are shown having small ripples with an average value of 5.2A and 2.2A, respectively.

As shown in Figure 15 the for the input voltage of 24 V the output voltage V_o is found to be 160 V at a duty cycle of = 0.3. The practical output voltage is reduced due to voltage drop across R_{DSON} of MOSFET, parasitic resistances of inductors capacitors and switch. As depicted in Figure. 16 the value of capacitor voltages V_{C1}, V_{C3}, and are found to be 30V, 80V and 80V respectively. It can be observed that the voltage stress across capacitors is less than V_0. Figure 17 shows the waveform of stress V_{S1} on switch S_1 with a value of 80V. All values of experimental waveforms closely agree with simulation results. The proposed converter has operated at D = 0.3 only for the verification of the simulation and theoretical results. It can be operated at a higher duty ratio to get a high voltage level which is required by the inverter.

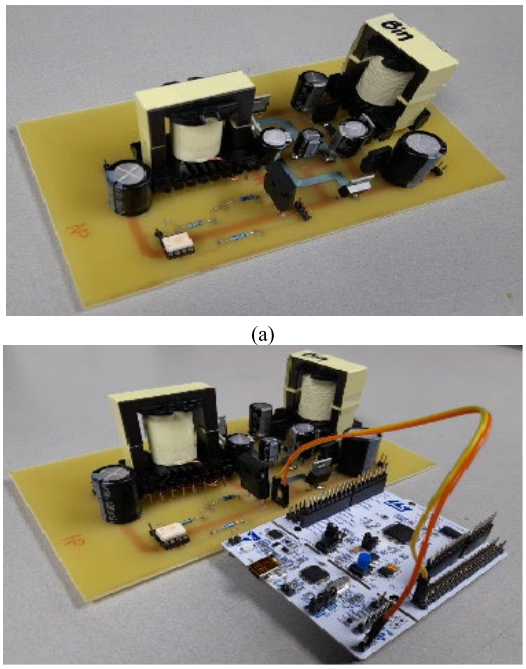

FIGURE 13. Hardware prototype of the proposed converter.

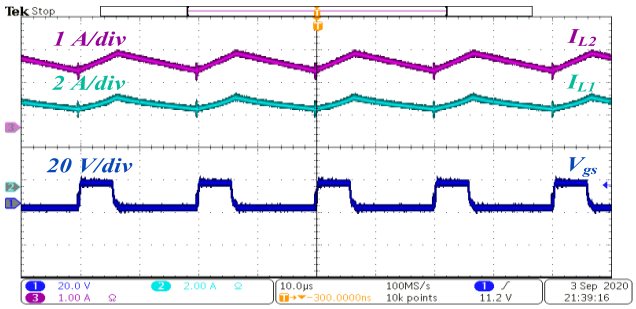

FIGURE 14. Experimental waveforms of I_{L1} and I_{L2} and V_{gS1} at D = 0.3.

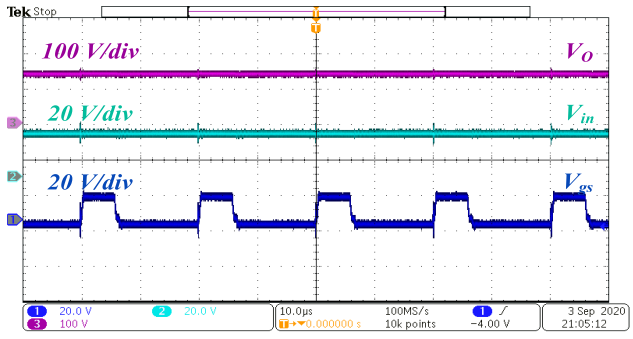

FIGURE 15. Simulated waveforms of V_o and V_{in} at D = 0.3 with V_{gS1}.

To quantify the losses in the converter and the efficiency of the converter, a complete analysis is performed. The simulated efficiency of the proposed converter versus output power P_o is plotted in Figure 18 at different value of source voltage V_{in}. It can be observed in Figure 18 that an increment

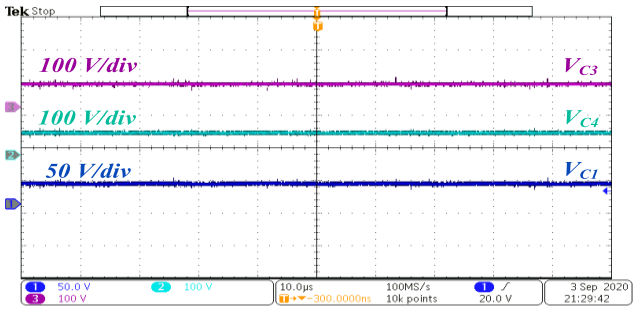

FIGURE 16. Simulated Waveforms of V_{C1}, V_{C3} and V_{C4} at D = 0.3.

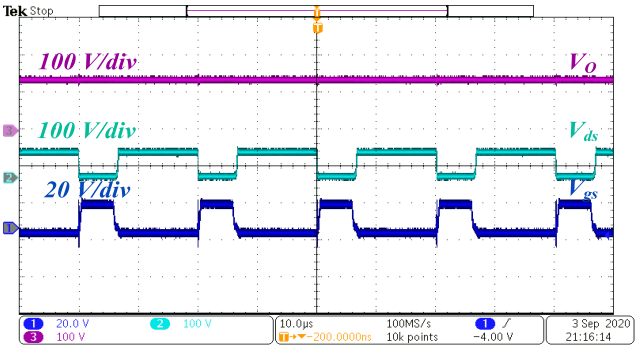

FIGURE 17. Simulated Waveforms of V_o, V_S and V_{gS1} at D = 0.3.

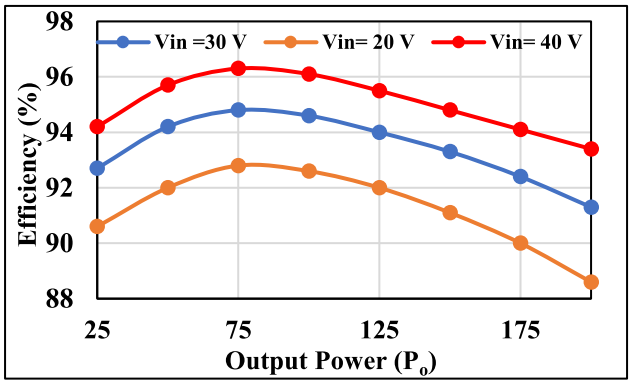

FIGURE 18. The efficiency of the Proposed Converter for different input voltages.

in input voltage improves the efficiency of the converter. The converter can be used in renewable energy applications up to 300 W with high efficiency. The proposed converter's peak efficiency is found to be greater than 95% when the input is 40 V and $P_o = 75$ W. Figure 19 illustrates the losses per group of the same components used in the proposed converter for $V_{in} = 24$V and D = 0.3. It can be noticed in Figure 19 that a 36% loss of total loss is due to diodes, and the contribution of switch S in loss is 14%. The losses in the converter can be further reduced by choosing fast recovery diodes with low internal resistance and cut-in voltage. Further, inductor resistance should also be kept low to increase the efficiency of the converter. It should be noted that steady-state equations of losses derived in this paper are used for calculation.

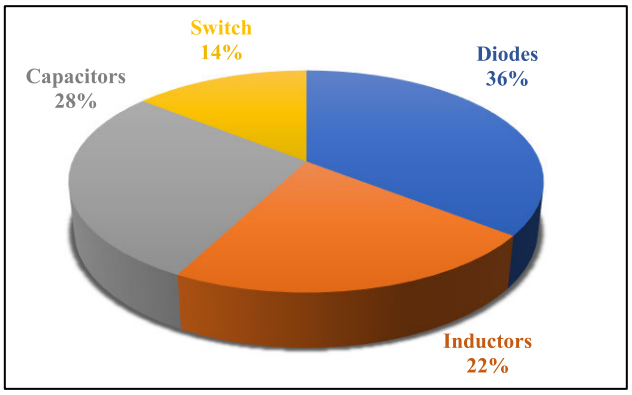

FIGURE 19. Losses in different components in the proposed converter.

VI. CONCLUSION

A new non-inverting DC-DC boost converter is proposed in this paper. The proposed converter has high gain and utilizes only one switch to operate the converter, and therefore, control is easy. The voltage stress on the switch and diodes is low, and therefore low voltage-rated switch can be chosen which increases the efficiency and reduces the cost. The converter has draws continuous input current and thus the need for an input filter does not arise. Hence, it can be used in microgrid applications as the voltage of the converter at a low duty ratio is high compared to the conventional boost converter and other high gain converters. To verify the analysis practically, a 200W hardware prototype has been prepared for the converter. The peak of the efficiency of the proposed converter is observed to be greater than 95% but the efficiency decreases at high output power on account of losses. Thus, the proposed converter is suitable for medium power range suitably up to 300W. The merits of the converter make it suitable to be used in solar PV applications, automobiles, fuel cells and electric vehicles.

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ARSHAD MAHMOOD is currently pursuing the Bachelor of Technology (B. Tech.) degree in electrical engineering from the Zakir Husain College of Engineering and Technology, Aligarh Muslim University, Aligarh, India. He has submitted and presented several papers on power electronics DC/DC converters in various conference proceedings and journals. His research interests include high gain DC to DC converter, solar PV systems, and maximum power point techniques. In one of his proceeding, he has won the Best Paper Award.

MOHAMMAD ZAID (Member, IEEE) received the degree and master's degree from the Zakir Husain College of Engineering and Technology (ZHCET), Aligarh Muslim University (AMU), Aligarh, India. He is currently working as an Assistant Professor with the Department of Electrical Engineering, ZHCET, AMU. He is also a Branch Counsellor of the IEEE Student Branch of the College. He has published research papers in the fields of DC/DC converters, multilevel inverters, and DG placement. The current research interest includes developing new topologies of high gain DC/DC converters for renewable energy applications.

JAVED AHMAD received the B.Tech. degree in electrical engineering from Aligarh Muslim University, Aligarh, India, in 2017, and the M.E. degree in electrical power from Universiti Teknologi Malaysia, Johor Bharu, Malaysia, in 2019. He is currently pursuing the Ph.D. degree with the National Taiwan University of Science and Technology (Taiwan Tech), Taipei, Taiwan. His research interests include managing hybrid energy storage systems, DC to DC converters, interleaved converters, multilevel inverter, and power conversion for electric vehicle applications.

MOHD ANAS KHAN is currently pursuing the B.Tech. degree in electrical engineering from Aligarh Muslim University, Aligarh, India. His research interests include modeling and design of power electronics circuits, efficient power conversion, and renewable electrical energy systems.

SHAHRUKH KHAN (Student Member, IEEE) is currently pursuing the B.Tech. degree with the Department of Electrical Engineering, Zakir Husain College of Engineering and Technology, Aligarh Muslim University, Aligarh, India. He has published and presented research papers on power electronic DC-DC converters in international conferences and reputed journals. His research interest includes design and control of power electronic converters, interleaved converters, and maximum power point techniques algorithms. He has won the Best Paper Award in one of his proceedings. He is the joint Secretary of IEEE Student Branch, AMU for the session 2020–2021.

ZAID SIFAT is currently pursuing the bachelor's degree in electrical engineering with the Zakir Hussain College of Engineering, Aligarh Muslim University, Aligarh, India. He has been an Active Member of IEEE Students Branch, AMU, since 2019. His research interests include multilevel inverters, grid connected inverters, power electronics converter, and its applications to renewable energy systems, and microgrid.

CHANG-HUA LIN (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electronic engineering from the National Taiwan University of Science and Technology, Taipei, Taiwan, China, in 1989, 1991, and 2000, respectively. He joined the Department of Electrical Engineering, National Taiwan University of Science and Technology, China, in 2016. He has engaged in research and teaching in the areas of power electronics, and electronic circuit design. He has developed eight Taiwan patents and six U.S. patents. His research interests include energy storage systems design, battery management systems design, and high voltage impulse circuits design. He is a member of the IEEE Power Electronics and Industrial Electronics Societies. He received the Young Researcher Award and the Best Paper Award from the National Science Council, China, in 2005.

ADIL SARWAR (Senior Member, IEEE) received the B. Tech., M. Tech., and Ph.D. degrees from Aligarh Muslim University, in 2006, 2008, and 2012, respectively. He was associated with the Electrical Engineering Department, Galgotias College of Engineering and Technology, G. Noida, India, from 2012 to 2015. He has been working with the Department of Electrical Engineering, Aligarh Muslim University, Aligarh, India, since 2015. He has published more than 50 research papers in international journals and conferences. He is also working on world-bank sponsored research projects. He is a Life Member of the Systems Society of India. He has contributed a chapter in *Handbook of Power Electronics* (Fourth Edition) Edited by M. H. Rashid.

MOHD TARIQ (Senior Member, IEEE) received the bachelor's degree in electrical engineering from Aligarh Muslim University, Aligarh, the master's degree in machine drives and power electronics from the Indian Institute of Technology (IIT)-Kharagpur, and the Ph.D. degree in electrical engineering from Nanyang Technological University (NTU), Singapore, with focus on power electronics and control.

He is currently working as an Assistant Professor with Aligarh Muslim University, where he is directing various sponsored research projects and leading a team of multiple researchers in the domain of power converters, energy storage devices, and their optimal control for electrified transportation and renewable energy application. Previously, he has worked as a Researcher with the Rolls-Royce-NTU Corporate Laboratory, Singapore, where he has worked on the design and development of power converters for more electric aircraft. Before joining his Ph.D. degree, he has worked as a Scientist with the National Institute of Ocean Technology, Chennai, under the Ministry of Earth Sciences, Government of India, where he has worked on the design and development of BLDC motors for the underwater remotely operated vehicle application. He also served as an Assistant Professor with Maulana Azad National Institute of Technology (MANIT), Bhopal, India. He has authored more than 130 research papers in international journals/conferences including many articles in IEEE Transactions/Journals. He is also the inventor of approximately 20 patents granted/published by the patent offices of USA, GB and India.

He was a recipient of the 2019 Premium Award for Best Paper in *IET Electrical Systems in Transportation* Journal for his work on more electric aircraft and the Best Paper Award from the IEEE Industry Applications Society's (IAS) and the Industrial Electronic Society (IES), Malaysia Section–Annual Symposium (ISCAIE-2016) held in Penang, Malaysia. He is the Young Scientist Scheme Awardee in 2019 supported by the Department of Science and Technology, Government of India and the Young Engineer Awardee in 2020 by the Institution of Engineers, India. He is also the Founder Chair of the IEEE AMU SB and the Founder Chair of the IEEE SIGHT AMU.

BASEM ALAMRI (Member, IEEE) received the B.Sc. degree (Hons.) in electrical engineering from the King Fahd University of Petroleum and Minerals (KFUPM), the M.Sc. degree (Hons.) in electrical power systems from King Abdulaziz University, Jeddah, Saudi Arabia, the M.Sc. degree (Hons.) in sustainable electrical power from Brunel University, London, U.K., in 2007 and 2008, respectively, and the Ph.D. degree in electrical power engineering from Brunel University, in 2017. He is currently an Assistant Professor of electrical engineering with the College of Engineering, Taif University. His research interests include power systems, power quality, power filter design, and smart grids, with a particular emphasis on the integration of renewable energy sources with power grids. He is a member of many international and local professional organizations. He is also a Certified Energy Auditor (CEA ®), Certified Energy Manager (CEM ®), and a Certified Measurement & Verification Professional (CMVP ®) of the Association of Energy Engineers (AEE), USA. He has received many awards and prizes, including a certificate from the Advance Electronics Company (AEC) in recognition of the Outstanding Academic Achievement during the B.Sc. degree with KFUPM. He also received the National Grid (NG) Prize, the Power Grid Operator, U.K., for his M.Sc. degree of the SEP Program with Brunel.