A Low Phase-Noise Dual-Frequency Oscillator Based on Filter Switching Technique

Jinming Lai, Hailong Wang, Chaojie Wang, Xiaohua Ma, and Zhiyou Li

***Abstract*— This letter presents a parallel-feedback dual-frequency oscillator (DFO) with low phase noise. It is achieved based on the filter switching technique. By using four switches to control two oscillator loops with a common active device, the oscillation frequency of the proposed DFO can be switched from one to another. Due to the high isolation level of the employed switches, the two oscillator loops almost operate independently. Thus, there is no intermodulation (IM) spurs generated in the output spectrum of the proposed DFO. In the meantime, to improve the phase noise performance of the DFO, each oscillator loop utilizes a high frequency-selectivity bandpass filter with high group delay (GD) as a frequency selective element. In this way, the low phase-noise DFO is developed. For demonstration, the DFO is designed, fabricated, and tested. As seen from the measurement results, the oscillator can oscillate at 2.04 or 3.092 GHz by controlling the four switches. At 100 kHz and 1 MHz frequency offset from the carrier frequency, the phase noises are −108.5 and −129.7 dBc/Hz for 2.04 GHz, while −112.7 and −135.7 dBc/Hz for 3.092 GHz.**

***Index Terms*— Dual-frequency oscillator (DFO), low phase-noise, microwave planar oscillator, parallel-feedback, pin switch, switching filter.**

I. Introduction

DUAL-FREQUENCY oscillator (DFO) catering to the multi-band or multi-standard wireless transceivers has drawn more attention in recent years [1]–[9]. Among the specifications of the DFO, the low phase noise and high intermodulation (IM) suppression, which are beneficial to the sensitivity and anti-interference performance improvement of a wireless transceiver [10], should be taken into prime consideration. As for a DFO, the oscillation frequencies usually can oscillate concurrently or independently by using the switching technique.

The concurrent DFO always associates with IM products due to the nonlinear behavior of the active device. Usually, the low isolation between the two oscillation frequencies leads to poor IM suppression [1]–[3]. For the purpose of enhancing IM suppression, the isolation between two oscillation frequencies was strengthened by using a compact diplexer [4] and an orthogonal dual-mode resonator [5]. To avoid the generation of IM products completely, the switchable DFO based on the CMOS process was proposed in [6] and [9]. This type of DFO can oscillate at one of two frequencies at a time by controlling switches. However, the phase noise remains to be improved as compared to the concurrent DFO achieved in [4].

Manuscript received August 4, 2021; revised September 5, 2021; accepted September 19, 2021. Date of publication October 6, 2021; date of current version January 10, 2022. *(Corresponding author: Zhiyou Li.)*

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Color versions of one or more figures in this letter are available at https://doi.org/10.1109/LMWC.2021.3114728.

Digital Object Identifier 10.1109/LMWC.2021.3114728

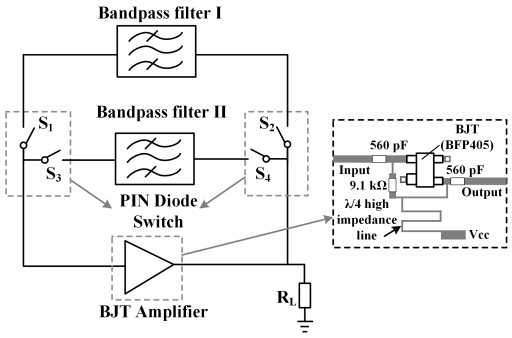

Fig. 1. Block diagram of the proposed parallel-feedback DFO.

In this letter, a low phase-noise parallel-feedback DFO based on the PCB process is realized by using four switches with a high isolation level. By controlling the switches, the oscillation frequency can be switched from one to another. Since the DFO outputs one oscillation frequency at a time, there are no mixing IM products for the proposed DFO. At the same time, the low phase noise is obtained by inserting a narrow-band bandpass filter with high group delay (GD) into each of the two oscillator loops [11]. The demonstrative DFO is designed, manufactured, and measured. The measured results show that the two oscillation frequencies of the DFO are 2.04 and 3.092 GHz with respective phase noise of −108.5 and −112.8 dBc/Hz at 100 kHz frequency offset.

II. Design of Parallel-Feedback DFO

A. Analysis

Fig. 1 presents the block diagram of the proposed parallel-feedback DFO. The DFO is composed of one BJT amplifier (BJT BFP405), four p-i-n diode switches, and two bandpass filters with different center frequencies. When switches S_1 and S_2 are "ON" state and switches S_3 and S_4 are "OFF" state, the oscillator can oscillate near the center frequency of the bandpass filter I. While the oscillator can oscillate near the center frequency of the bandpass filter II with switches S_3 and S_4 being "ON" state, switches S_3 and S_4 being "OFF" state. The switches S_1–S_4 are realized by using the p-i-n diode MA4AGP907 ($R_s = 3\ \Omega$, $C_t = 27$ fF) from MA/COM corporation.

As for the parallel-feedback oscillator, the phase noise can be effectively weighed by the Leeson model and improved by employing a filter with high GD (τ) and low insertion loss (IL) [11]–[13]. In this design, the compact filter with high GD which is similar to the structure in [14], is adopted to realize the bandpass filters I and II, as shown

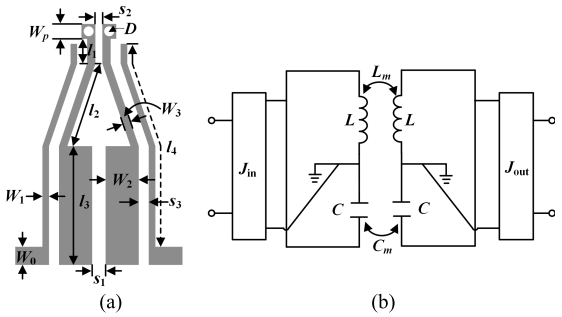

Fig. 2. Compact second-order filter. (a) Layout. (b) Equivalent circuit.

in Fig. 2. Therefore, the low phase-noise DFO with compact size is constructed.

B. Filter Design

For the realization of two bandpass filters shown in Fig. 1, the center frequency is set as 2.0 and 3.1 GHz, respectively. Fig. 2 presents the corresponding filter structure and its equivalent circuit. The filter consists of two quarter-wavelength step-impedance resonators (SIRs), which are fed by an open-ended parallel-coupled line. By introducing mixed electric and magnetic coupling, a transmission zero (TZ) is generated at the edge of the filter passband, which enhances the GD peak value [11].

As observed from Fig. 2, the capacitive coupling E_C (C_m) is realized by changing gap s_1, while the inductive coupling $M_C(L_m)$ is realized by choosing proper l_1 and s_2. When $E_c > M_c$, the TZ locates at the left side of the passband. Otherwise, the TZ locates on the right side. To design the filters, the RT/Duroid 4003 C substrate ($\varepsilon_r = 3.38$, $h = 0.508$ mm, tan $\delta = 0.0027$) is employed. Based on the calculation formulas for the SIR resonator [15], the dimensions of the 2-GHz filter can be initiated. A detailed analysis for the TZ shift with different parameters is made, as shown in Fig. 3. As l_1 decreases and s_2 increases, the TZ shifts from the right side to the left side of the passband, as shown in Fig. 3(a) and (b). The variation of l_1 causes the passband shift, which can be compensated by slightly changing l_2, while the decrement of s_1 also can change TZ location in the same way, as shown in Fig. 3(c). In this design, the TZ is designed at the right side of the passband, resulting in phase variation with a negative slope [16]. So the bandwidth and TZ location can be decided by optimizing l_1, s_1, and s_2. The good return loss (*RL*) of the passband can be obtained by optimizing W_1 and s_3. By using Ansoft's High Frequency Structure Simulator (HFSS) software, the 2-GHz filter is optimized and final dimensions are obtained as: $W_0 = 1.1$, $W_1 = 0.2$, $W_2 = 2$, $W_3 = 0.3$, $W_p = 0.5$, $s_1 = 0.15$, $s_2 = 0.16$, $s_3 = 0.35$, $l_1 = 1.5$, $l_2 = 5.28$, $l_3 = 7.2$, $l_4 = 12.58$, $D = 0.3$ (unit: mm). Using the same design procedure, the 3.1-GHz filter is also designed and its final dimensions with the same denotation as 2-GHz filter are: $W_0 = 1.1$, $W_1 = 0.28$, $W_2 = 2$, $W_3 = 0.3$, $W_p = 0.5$, $s_1 = 0.17$, $s_2 = 0.18$, $s_3 = 0.35$, $l_1 = 1$, $l_2 = 3.45$, $l_3 = 4.5$, $l_4 = 7.55$, $D = 0.3$ (unit: mm). Herein, the loaded quality factor (Q_L) of a filter is employed, which is associated with phase noise improvement [11]. The two standalone bandpass filters are plotted in Fig. 4(a) whose simulated frequency responses and loaded quality factor (Q_L) are presented in Fig. 4(b) and (c) in the red dashed line. The Q_L peak of 2-GHz filter located at 2.045 GHz is 58 with an IL of 5.3 dB. As for 3.1-GHz filter, the Q_L peak located at 3.1 GHz is 72 with an IL of 5.5 dB. By designing the oscillation frequencies at these two Q_L peaks, the low phase-noise DFO can be realized.

TABLE I
PERFORMANCE COMPARISONS WITH OTHER REPORTED DFOS

Ref.	f_o (GHz)	P_{out} (dBm)	PN (dBc/Hz)	FOM (dBc/Hz)	IM2 /IM3 (dB)	C./ S.
[2]	2.48 5.4	4.9 2.2	-114 -104 @1MHz	-177 -173.9 @1MHz	≤-4.8/ -18.7	C.
[3]	1.802 3.42	5.39 3.31	-140.24 -126.3 @1MHz	-191.6 -183.1 @1MHz	<-25/ -30	C.
[4]	4.18 5.49	-0.87 5.38	-134.2 -130.8 @1MHz	-193.6 -192.6 @1MHz	≤-24/ -35	C.
[5]	1.85 2.66	5.37 6.8	-120.84 -121.7 @1MHz	-172.6 -177.2 @1MHz	<-50	C.
[6]	2.675 3.77	5.33 10.83	-118 -113 @1MHz	-164.3 -159.5 @1MHz	n/a	S.
This work	**2.04 3.092**	**5.6 1.6**	**-129.7 -135.7 @1MHz**	**-181.1 -190.7 @1MHz**	**n/a**	**S.**

C.: Concurrent; S.: Switchable.

C. Circuit Implementation of Parallel-Feedback DFO

According to the schematic of DFO shown in Fig. 1, the 2-GHz filter and 3.1-GHz filter are used to implement the bandpass filters I and II, respectively. However, the loading effect will happen when two developed filters are associated with p-i-n diodes, which may deteriorate the filter frequency response. Thus, it is necessary to take the loading effect into consideration. Fig. 4(a) presents the switching filter layout for the analysis of the loading effect. When the p-i-n diodes D1 and D2 are "ON" state, D3 and D4 are "OFF" state, the frequency response and Q_L are obtained, as shown in Fig. 4(b) (in solid line). In the same way, the frequency response and Q_L are shown in Fig. 4(c) when D1 and D2 are "OFF" state and D3 and D4 are "ON" state. Due to the low IL of 0.25 dB and high isolation level of 30 dB of the used p-i-n diodes, the IL, *RL*, and Q_L of the switching filter show a slight difference when compared to the stand-alone 2-GHz filter and 3.1-GHz filter. Thus, the loading effect will have a little effect on the phase noise performance of the DFO.

To satisfy the oscillating condition (Barkhausen criteria) of the proposed DFO [16], the common part of the oscillating loops is fixed first by using the Keysight's Advanced Design System 2015 (ADS2015) software. Then, the length of the 50 Ω feeding line of the 3.1-GHz filter should be adjusted to make the loop phase at 3.1 GHz satisfy 0° or multiple of 360°. Finally, the loop phase at 2.045 GHz is also set as 0° or multiple of 360° by changing the length of the feeding line of 2-GHz filter. Thus, the DFO with detailed dimensions is developed and also fabricated using the PCB process for demonstration, as presented in Fig. 5(a). It should be noted that the p-i-n diodes are pasted onto the printed board by using electrically conductive Ag epoxy, while other elements are soldered by using SnPb solders.

III. MEASUREMENT RESULTS

The fabricated DFO is measured by using the Agilent's Spectrum Analyzer E4440A. The coil inductors L_b with 20 turns, bypass capacitors C_b with 100 pF, and resistors R_b with 100 Ω are chosen for diode bias. While the control

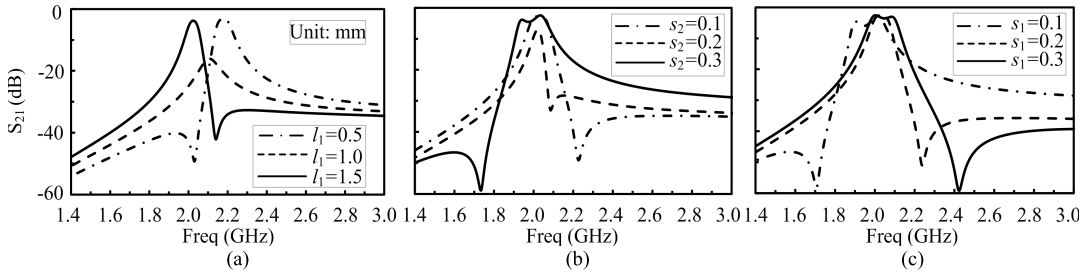

Fig. 3. Simulated frequency responses with (a) different l_1 when $s_1 = 0.15$, $s_2 = 0.16$, (b) different s_2 when $l_1 = 1.5$, $s_2 = 0.16$, and (c) different s_1 when $l_1 = 1.5$, $s_1 = 0.15$. (Unit: mm).

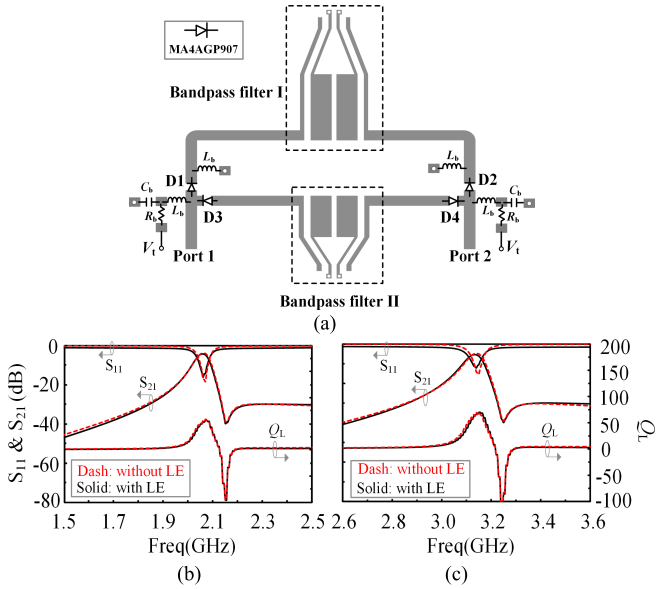

Fig. 4. Switching filter. (a) Layout. (b) Simulated frequency responses with and without LE for 2-GHz filter. (c) Simulated frequency responses with and without LE for 3.1-GHz filter. (LE: Loading effect).

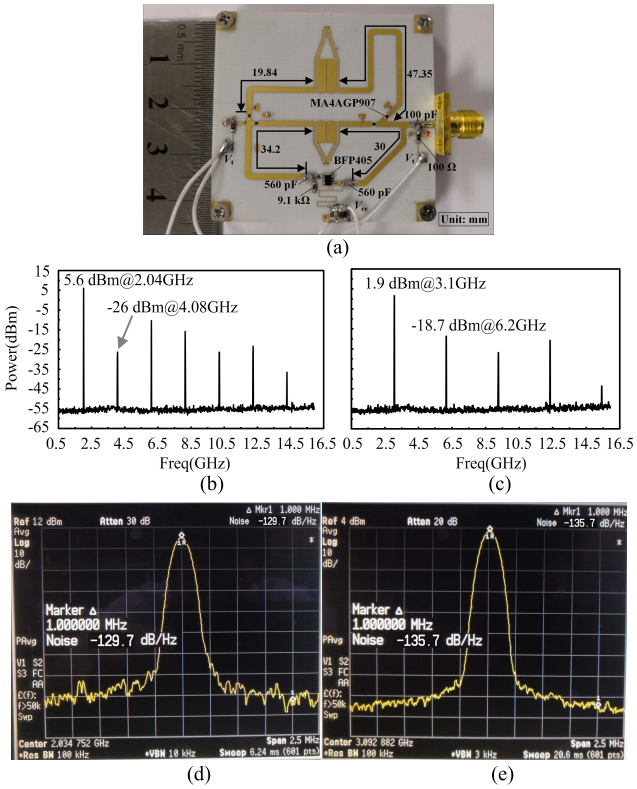

Fig. 5. Proposed DFO. (a) Photograph. (b) Output spectrum at $f_0 = 2.04$ GHz and (c) $f_0 = 3.092$ GHz. (d) Measured phase noise at $f_0 = 2.04$ GHz and (e) $f_0 = 3.092$ GHz.

voltage V_t is 1.8 V with a current of 10 mA and dc supply V_{cc} is 3 V with a current of 10 mA, the DFO oscillates at 2.04 GHz with an output power of 5.6 dBm, which is given in Fig. 5(b). The phase noises at 100 kHz and 1 MHz frequency offset are -108.5 and -129.7 dBc/Hz. By setting V_t as -1.8 V, the oscillation frequency is switched from 2.04 to 3.092 GHz with an output power of 1.9 dBm, as shown in Fig. 5(c). The corresponding phase noises at 100 kHz and 1 MHz frequency offset are -112.8 and -135.7 dBc/Hz. In Fig. 5(d) and (e), the measured phase noises of two oscillation frequencies at 1 MHz frequency offset are displayed. Moreover, over 17-dBc harmonic suppression is achieved in the output spectrum. Owing to the higher Q_L, the phase noise for 3.092 GHz is better than that for 2.04 GHz.

The figure-of-merit (FOM) used to evaluate the overall performance of an oscillator is given by [16]

$$\text{FOM} = L(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{\text{dc}}}{1\,\text{mW}}\right) \quad (1)$$

where $L(\Delta f)$ is the phase noise at Δf frequency offset, f_0 is oscillation frequency, and P_{dc} is dc power dissipation in mW. At the oscillation frequencies of 2.04 and 3.092 GHz, the respective FOMs are calculated as -181.1 and -190.7 dBc/Hz at 1 MHz frequency offset. Due to the extra dc power consumption generated by p-i-n diode switches, the FOMs are degraded. The performance comparison between the proposed DFO and other reported DFOs is also investigated, which is listed in Table I. The proposed DFO not only avoids the generation of IM products except for the harmonic products, but also achieves low phase noise as compared to the reported DFOs, which is preferable to the dual-band transceiver with high sensitivity. In the meantime, the developed switched parallel-feedback DFO based on the PCB process is also first realized.

IV. Conclusion

This letter presents a low phase-noise DFO using the filter switching technique. By utilizing the high-isolation p-i-n diodes with low IL, the two oscillation frequencies operate independently. As a result, there are no other spurious frequencies except for the harmonics of the oscillation frequency. The achieved low phase noise performance is due to the employment of the narrow-band bandpass filter with high GD and harmonic suppression. The measurement results of the state-of-art DFO have demonstrated the validity of the design method.

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