A multiply-by-two sample-and-hold amplifier (SHA) for the front-end stage of a 9-bit 5 MS/s analog-to-digital converter is required. The needed SHA design specifications are as follows:

- Technology: 0.18μm
- Power supply voltage: 1.8V
- Sampling frequency (fs): 5 MHz (Settling time < 100ns)
- Total settling error $< 2^{-10}$ V
- Maximum output swing > 1 V_{P-p}
- Feedback capacitor of the SHA: $C_1=C_2=0.5$ pF
- Load capacitance of the SHA: $C_L=1$ pF
- Power dissipation: as low as possible
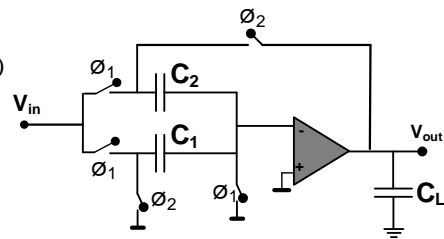
- The first phase of project is to design an open-loop operational amplifier suitable for this sample-and-hold. This opamp should then be employed in the mentioned sample-and-hold to ensure the reliable performance.

- Suggest the amplifier optimum topology as well as its compensation network. (Depending on your decision for lower power consumption, the opamp could be implemented as twostage or single-stage with or without gain-boosting structures).

- Only one ideal reference current source should be used and the biasing network as well as the needed switches should be real.

- Simulate your amplifier AC open-loop frequency characteristics.
- Simulate the closed-loop sample-and-hold transient response.

Documentation:
- Prepare your documentation file in two-column format included followings:
    o Introduction
    o Design procedure and calculations
    o Simulation results
        ▪ Frequency response of opamp
        ▪ Swing of opamp
        ▪ Transient response of SHA
        ▪ Output THD
    o Discuss on the effect of the non-idealities of the opamp and switches on the SHA performance metrics
    o Comments and conclusions