Analysis and Design of Wideband Injection-Locked Ring Oscillators With Multiple-Input Injection

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Abstract—In this paper, the locking range of the injection-locked ring oscillators is investigated. To improve the injection efficiency and the locking range for superharmonic frequency division, a multiple-injection technique is proposed. Using a 0.18- μ m CMOS process, a wideband frequency divider based on a three-stage ring oscillator is implemented for demonstration. With a tunable free-running frequency, the fabricated circuit provides 2:1 and 4:1 frequency division with a single-ended input signal ranging from 13 to 25 and 30 to 45 GHz, respectively. Compared with the case of the single-ended injection, the locking range of the frequency divider almost doubles when multiple-input injection with optimum phases is utilized. The experimental results exhibit good agreement with the theoretical derivation and the circuit simulation.

Index Terms—Injection-locked ring oscillators, locking range, multiple-input injection, superharmonic frequency dividers.

I. INTRODUCTION

N BOTH wireless and wire-line communication systems, the frequency divider is one of the most critical building blocks for the implementation of frequency synthesizers and phase-locked loops (PLLs). As the carrier frequency and the data rate increase due to the fast-growing market in personal communications services, it is desirable to fabricate the high-speed dividers using a cost-efficient CMOS technology. Conventionally, high-speed CMOS dividers are realized by current-mode-logic (CML) flip-flop stages [1]. Though a very wide input range is demonstrated, the maximum operating speed of the flip-flop-based frequency dividers is limited by the cut-off frequency (f_T) of the transistors. Alternatively, injection-locked frequency dividers [2]-[4] have been adopted to alleviate the limitation on f_T for applications at frequencies in the tens of gigahertz. Due to the use of inductors in the LC-tanks, the input locking range is typically bounded by the narrowband characteristics of the loads. In addition, the on-chip inductors required in the resonators occupy large chip area, especially when dividers are cascaded to provide a high division ratio, leading to a significant increase in the implementation

To overcome the design issues of the high-speed frequency dividers, a circuit topology based on the injection-locked ring

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oscillators [5]–[7] with multiple-input injection is proposed. The concept of multiple-input injection has been applied to a ring oscillator for precision quadrature generation [8], [9]. However, in this paper, the operation of the superharmonic injection-locked ring oscillator is investigated. In addition, detailed analysis on the locking range for various injection topologies and division ratios is presented to optimize the circuit performance. Using a standard 0.18- μ m CMOS process, a three-stage injection-locked ring oscillator is implemented for demonstration. Due to the absence of on-chip inductors in the proposed circuit, the chip area can be reduced for a minimum hardware cost. With optimum phases for the multiple-input injection, the fabricated divider exhibits a wide locking range for divide-by-two operations at the 20-GHz frequency band and for divide-by-four operations in the vicinity of 40 GHz.

The paper is organized as follows. Section II provides theoretical analysis on the locking range of an injection-locked ring oscillator with various injection topologies. The circuit design and the experimental results of the wideband CMOS frequency divider based on a three-stage injection-locked ring oscillator are presented in Sections III and IV, respectively. Finally, a conclusion is given in Section V.

II. ANALYSIS ON THE LOCKING RANGE OF THE INJECTION-LOCKED RING OSCILLATORS

A. Locking Range With Single-Ended Injection

A conceptual block diagram of an N-stage resistive-load ring oscillator is depicted in Fig. 1(a). For simplicity, ring oscillators with odd-number inverter stages are considered, while the same derivation procedure can be extended for an even number of differential stages with a cross-connected feedback provided. To satisfy the Barkhausen criteria for a sustained oscillation, the total phase of the loop should be multiple of 2π , which implies a phase shift of $-\pi/N$ from the load in each one of the inverter stages as shown in Fig. 1(b). The simplified illustration of the current phasor diagram for a free-running ring oscillator is shown in Fig. 1(c). As an injected fundamental signal I_{inj} is applied to the ring oscillator, the oscillation frequency deviates from its free-running value f_0 due to the injection locking [10], [11]. Assuming that loop gain is sufficiently large, the locking range is determined by the phase limitation in the loop. The equivalent circuit model and the current phasor diagram of a ring oscillator under locked condition are shown in Fig. 2. With a single-ended input injection at $f_{\rm in} = f_0 + \Delta f$, an additional phase shift of ϕ is introduced into the loop by the injected stage. For the injection-locked condition, the phase contributed by the loads of the individual stages deviates from its original value

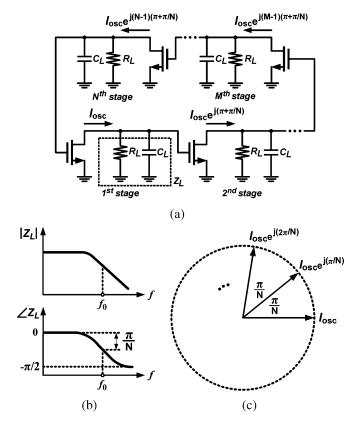


Fig. 1. N-stage resistive-load ring oscillator at free running. (a) Simplified model. (b) Phase shift at the load. (c) Current phasor diagram.

by θ . Again, to satisfy the criteria for a sustained oscillation, the required phase condition is given by

$$\left(\pi + \frac{\pi}{N} + \theta\right) \times N + \phi = 2k\pi \tag{1}$$

where k is an integer. The limitation imposed on the phase shift θ , which predetermines the locking range, can be expressed as

$$\theta = -\frac{1}{N}\phi. \tag{2}$$

Assuming the injection current $I_{\rm inj}$ is much smaller than the current components $I_{\rm osc}$ and $I_{\rm load}$

$$|I_{\text{load}}| \approx |I_{\text{osc}}| \gg |I_{\text{ini}}|$$
 (3)

the relation of the current phasors in Fig. 2(c) is given by

$$\sin \phi = \left| \frac{I_{\text{inj}}}{I_{\text{osc}}} \right| \times \sin(\alpha - \phi) = \left| \frac{I_{\text{inj}}}{I_{\text{osc}}} \right| \times (\sin \alpha \cdot \cos \phi - \sin \phi \cdot \cos \alpha).$$
(4)

For a small phase shift ϕ , the approximation $\sin \phi \approx \phi$ is valid, and the expression in (4) can be reduced to

$$\phi = \frac{|I_{\rm inj}| \sin \alpha}{|I_{\rm inj}| \cos \alpha + |I_{\rm osc}|}.$$
 (5)

By setting the first derivative of ϕ zero $(\partial \phi/\partial \alpha = 0)$, the maximum achievable phase shift for a given input injection is

$$\phi_{\text{max}} = \frac{|I_{\text{inj}}|}{\sqrt{|I_{\text{osc}}|^2 - |I_{\text{inj}}|^2}}.$$
 (6)

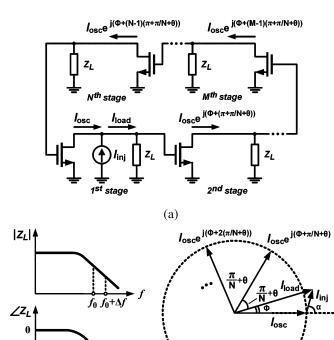


Fig. 2. Injection-locked ring oscillator with single-ended input injection. (a) Simplified model. (b) Phase shift at the load. (c) Current phasor diagram.

Under the condition as specified in (6), $I_{\rm inj}$ is orthogonal to $I_{\rm load}$. Note that the phase shift contributed by the *RC* network near the free-running frequency can be expressed as

$$\tan^{-1}\left(\frac{f}{f_0}\right) = \frac{\pi}{N} + \theta. \tag{7}$$

(c)

By applying the Taylor series to (7) in the vicinity of f_0 , the phase shift at the load is approximated by

$$\theta \approx \frac{\tan\frac{\pi}{N}}{1 + \tan^2\frac{\pi}{N}} \cdot \frac{\Delta f}{f_0}.$$
 (8)

The one-sided locking range for the single-ended injection at the fundamental frequency can be obtained by substituting (6) and (8) into (2):

$$\frac{\Delta f}{f_0} \le \frac{1}{N} \cdot \frac{1 + \tan^2(\pi/N)}{\tan(\pi/N)} \cdot \left| \frac{I_{\text{inj}}}{I_{\text{osc}}} \right| \cdot \left(1 - \left| \frac{I_{\text{inj}}}{I_{\text{osc}}} \right|^2 \right)^{-\frac{1}{2}}. \tag{9}$$

From (9), it is observed that, for a given injection efficiency $(|I_{\rm inj}/I_{\rm osc}|)$, the locking range $(\Delta f/f_0)$ decreases as the number of stages (N) increases.

B. Locking Range With Multiple-Input Injection

With a single-ended input injection, the locking-range of the ring oscillator is severely limited since the total phase shift in the loop contributed by the loads is compensated by only one injection current. Intuitively, the limitation can be effectively

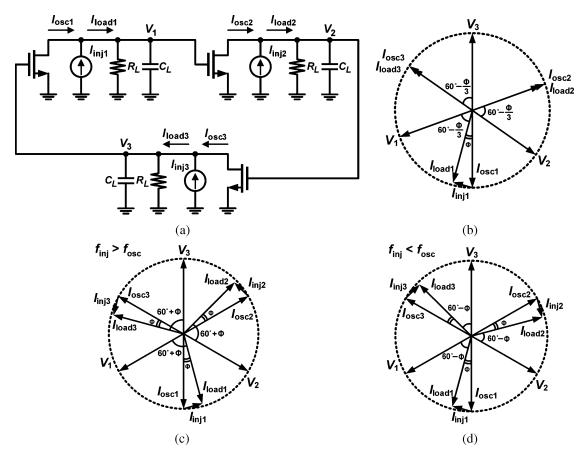


Fig. 3. (a) Simplified circuit model of the three-stage ring oscillator, and the current phasor diagrams with (b) singled-ended injection, (c) multiple-input injection for $f_{\rm inj} > f_{\rm osc}$, and (d) multiple-input injection for $f_{\rm inj} < f_{\rm osc}$.

alleviated if multiple input signals with proper phases are injected simultaneously. In this case, each one of the injected signals contributes to compensate for the total phase shift such that an enhanced locking range can be achieved [12]. To have a better understanding on the effect of the multiple-input injection, a three-stage ring oscillator is taken as an example. The simplified circuit model and the phasor diagrams of the ring oscillator under various injection conditions are shown in Fig. 3. Note that, as described in the case of the single-ended input injection, the locking range reaches its maximum value when each injected signal bears a phase difference such that $I_{\rm inj}$ is orthogonal to I_{load} at injection locking. For a three-stage ring oscillator, the phase difference between the consecutive inputs has to be $-4\pi/3$ (or $2\pi/3$) for a maximum input locking range as illustrated in Fig. 3(c) and (d). This condition also applies for multiple-input injection with an arbitrary number of inputs. Provided the optimum phase difference among M input injections, the overall phase shift is thus M times as large as that of the single-ended case with identical injection power. However, the locking range decreases or becomes even worse than the case for the single-ended one as the input phase difference departs from the optimum value.

C. Superharmonic Injection-Locked Ring Oscillator

The conclusion obtained from the analysis of the fundamental injection can be extended to predict the maximum locking range

of the ring oscillator operating as a superharmonic frequency divider. In this case, the ring oscillator is modeled as a regenerative frequency divider [5] where the frequency division is achieved by the multiplication operation provided by the mixer. Again, the analysis starts with the single-ended input injection. Fig. 4 shows the equivalent circuit model for a three-stage ring oscillator as a 2:1 frequency divider where the mixer is implemented by a CMOS differential pair. Assuming that the LO signal is sufficiently large such that the mixer is switched abruptly and the resulting high-order harmonics are filtered out by the succeeding low-pass stages, the output current of the mixer for the divide-by-two operation is derived as [13], [14]

$$I_o = |I_o|\cos(\omega t + \alpha + \phi(\alpha)) \tag{10}$$

where α represents the relative phase between the fundamental component and the second harmonic injection, and the phase introduced by the mixer is

$$\phi(\alpha) = -\tan^{-1}\left(\frac{2\eta\sin(2\alpha)}{3 + \eta\cos(2\alpha)}\right). \tag{11}$$

In this derivation, the injection ratio is defined as $\eta = I_{\rm inj}/I_{\rm osc}$. The total phase shift from the loads due to the frequency deviation for phase locking must satisfy

$$\theta = \frac{1}{3}\phi(\alpha) \le \frac{1}{3}\phi_{\text{max}} \tag{12}$$

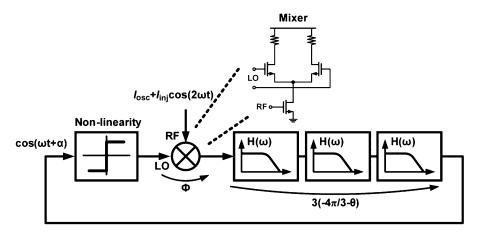


Fig. 4. Equivalent circuit model for a three-stage ring oscillator as a 2:1 frequency divider with single-ended injection.

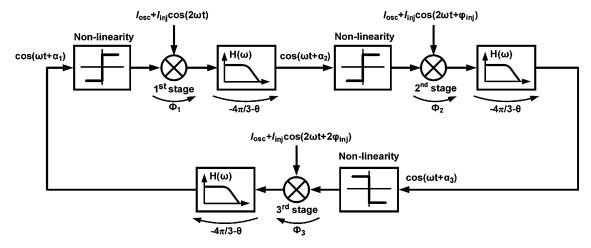


Fig. 5. Equivalent circuit model for a three-stage ring oscillator as a superharmonic frequency divider with multiple-input injection.

where $\phi_{\rm max}$ is the maximum achievable phase shift of the mixer by setting $\partial \phi / \partial \alpha = 0$. Thus, the one-sided locking range for the divide-by-two operation is approximated by

$$\frac{\Delta f}{f_0} \le \frac{4}{3\sqrt{3}} \tan^{-1} \left(\frac{2}{\sqrt{(3/\eta)^2 - 1}} \right).$$
(13)

In order to enhance the locking range for frequency division, the ring oscillator is injected by multiple inputs simultaneously. The derivations for the single-ended case are extended to evaluate the locking range with respect to the phase difference among the input injections. Fig. 5 shows the equivalent circuit model where the phase difference between the injected signals of the adjacent stages is specified as $\varphi_{\rm inj}$. The phases introduced by the individual mixer stages are

$$\phi_1 = -\tan^{-1}\left(\frac{2\eta\sin(2\alpha_1)}{3 + \eta\cos(2\alpha_1)}\right)$$
 (14)

$$\phi_2 = -\tan^{-1}\left(\frac{2\eta\sin(2\alpha_2 - \varphi_{\rm inj})}{3 + \eta\cos(2\alpha_2 - \varphi_{\rm inj})}\right)$$
(15)

$$\phi_2 = -\tan^{-1}\left(\frac{2\eta\sin(2\alpha_2 - \varphi_{\text{inj}})}{3 + \eta\cos(2\alpha_2 - \varphi_{\text{inj}})}\right)$$
(15)
$$\phi_3 = -\tan^{-1}\left(\frac{2\eta\sin(2\alpha_3 - 2\varphi_{\text{inj}})}{3 + \eta\cos(2\alpha_3 - 2\varphi_{\text{inj}})}\right).$$
(16)

In practical cases, the phase shifts ϕ_1 , ϕ_2 , and ϕ_3 are relatively small for $I_{\rm inj} \ll I_{\rm osc}$, and the phases of the fundamental com-

ponents at the inputs of the mixer stages can be approximated by

$$\alpha_1 = \alpha \tag{17}$$

$$\alpha_2 = \alpha_1 + \phi_1 - \left(\frac{4\pi}{3} + \theta\right) \approx \alpha - \frac{4\pi}{3} \tag{18}$$

$$\alpha_3 = \alpha_2 + \phi_2 - \left(\frac{4\pi}{3} + \theta\right) \approx \alpha - \frac{8\pi}{3}.$$
 (19)

By plugging (17)–(19) into (14)–(16), the total phase shift from the mixers is given by

$$\phi_T = \phi_1 + \phi_2 + \phi_3$$

$$= -\tan^{-1} \left(\frac{2\eta \sin(2\alpha)}{3 + \eta \cos(2\alpha)} \right)$$

$$-\tan^{-1} \left(\frac{2\eta \sin(2\alpha - 8\pi/3 - \varphi_{\text{inj}})}{3 + \eta \cos(2\alpha - 8\pi/3 - \varphi_{\text{inj}})} \right)$$

$$-\tan^{-1} \left(\frac{2\eta \sin(2\alpha - 16\pi/3 - 2\varphi_{\text{inj}})}{3 + \eta \cos(2\alpha - 16\pi/3 - 2\varphi_{\text{inj}})} \right). (20)$$

To sustain the phase locking within the loop, the phase shift of the loads due to frequency deviation must satisfy

$$\theta = \frac{1}{3}\phi_T \le \frac{1}{3}\phi_{T,\text{max}} \tag{21}$$

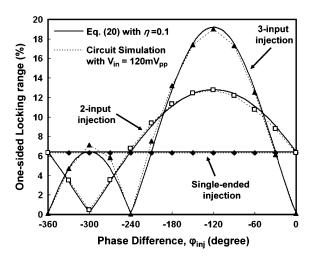


Fig. 6. Calculated and simulated locking range of the three-stage ring oscillator for divide-by-two operations.

where $\phi_{T, \rm max}$ is the maximum total phase shift of the mixer stages. Therefore, for a given $\varphi_{\rm inj}$, the locking range of the divide-by-two operation with multiple-input injection can be expressed as

$$\left| \frac{\Delta f}{f_0} \right| \le \frac{4}{3\sqrt{3}} \phi_{T,\text{max}}. \tag{22}$$

The locking range of the three-stage ring oscillator operated as a 2:1 frequency divider is shown in Fig. 6. It is noted that the calculated results obtained from the theoretical derivations show good agreement with the circuit simulation. Provided an optimum phase difference of $-2\pi/3$, the resultant locking range is enhanced by a factor of 2.02 and 3.01 for two- and three-input injections, respectively, compared with the single-ended case.

In order to evaluate the multiple-injection technique for the 4:1 frequency division, similar derivations can be carried out by replacing the input injections with a frequency at the fourth harmonic. Note that, in this case, the multiplication of the input injection and the fifth harmonic resulted from the nonlinearity of the individual stages should be taken into account for the fundamental component at the mixer output. Consequently, the total phase shift contributed by the mixer stages is defined as

$$\phi_{T} = \phi_{1} + \phi_{2} + \phi_{3}$$

$$= -\tan^{-1} \left(\frac{4\eta \sin(4\alpha)}{15 - \eta \cos(4\alpha)} \right)$$

$$-\tan^{-1} \left(\frac{4\eta \sin(4\alpha - 16\pi/3 - \varphi_{\text{inj}})}{15 - \eta \cos(4\alpha - 16\pi/3 - \varphi_{\text{inj}})} \right)$$

$$-\tan^{-1} \left(\frac{4\eta \sin(4\alpha - 32\pi/3 - 2\varphi_{\text{inj}})}{15 - \eta \cos(4\alpha - 32\pi/3 - 2\varphi_{\text{inj}})} \right). (23)$$

For a given phase difference $\varphi_{\rm inj}$ among the inputs, the locking range of the divide-by-four operation can be expressed by plugging (23) into (22). Fig. 7 shows the locking range for 4:1 frequency division as a function of $\varphi_{\rm inj}$. Note that, in the calculation, η is decreased from 0.1 to 0.025 to account for the higher loss at the drain node of the injected transistor and the degraded conversion gain at the fourth harmonic frequency. It is indicated that the optimum phase difference among the input in-

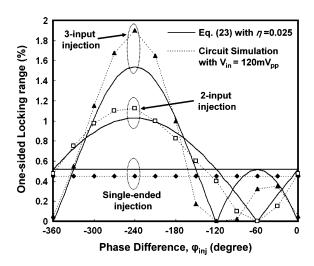


Fig. 7. Calculated and simulated locking range of the three-stage ring oscillator for divide-by-four operations.

jections is $-4\pi/3$ for the three-stage ring oscillator to perform 4:1 frequency division. Provided the optimum phase difference, the simulated locking ranges for two-and three-input injections are enhanced by a factor of 2.4 and 4.2, respectively, compared with the case for single-ended injection. In order to apply the multiple-injection technique for divider designs, a simplified approach to define the optimum input phase difference is presented in the Appendix.

III. DESIGN OF THE WIDEBAND FREQUENCY DIVIDER

Fig. 8(a) shows the schematic of the three-stage injectionlocked ring oscillator where two identical inverters with resistive loads are used as the first and second stages and the third stage is realized by an inverter with tunable active loads. To employ the proposed multiple-injection technique for an enhanced locking range, both tail transistors $M_{\rm CLK1}$ and $M_{\rm CLK2}$ are adopted for signal injection. In consideration of high-speed operations, the first two stages are designed to provide a sufficient voltage gain with a minimum gate delay. The wideband operation of the ring oscillator is achieved by the variable delay of the third stage. As V_{ctrl} increases, the tail current of the third inverter stage increases. Due to the use of the replica circuit, the load resistance of M_{P1} and M_{P2} decreases, leading to a reduced gate delay and a higher free-running frequency. Fig. 8(b) shows a simplified small-signal model of the proposed ring oscillator to evaluate the frequency tuning range. In the circuit model, R_T is a variable resistor, representing the equivalent resistance of the non-saturated load transistors \mathcal{M}_{P1} and \mathcal{M}_{P2} . Assuming $R_T = \beta \cdot R_L$, the free-running frequency of the ring oscillator can be derived from the Barkhausen criteria, and is given by

$$f_0 = \frac{1}{2\pi \cdot R_L C_L} \left(\sqrt{\frac{2}{\beta} \cdot \frac{C_L}{C_T}} + 1 \right). \tag{24}$$

In this particular design, $C_T \approx 2C_L$ and the resistance ratio β ranges from 0.5 to 3 as the controlled voltage $V_{\rm ctr1}$ varies, resulting in a frequency tuning range of 40% for wideband operations.

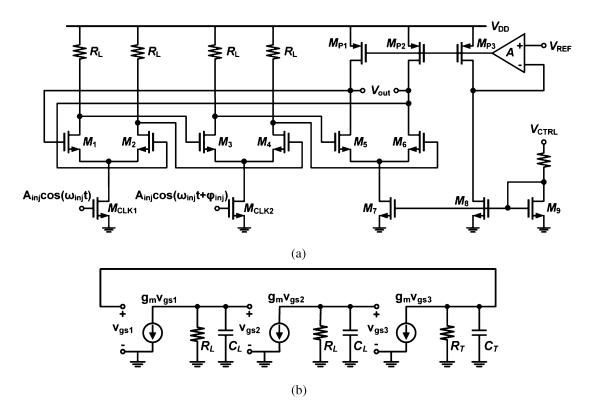


Fig. 8. (a) Schematic and (b) equivalent small-signal model of the proposed wideband injection-locked ring oscillator.

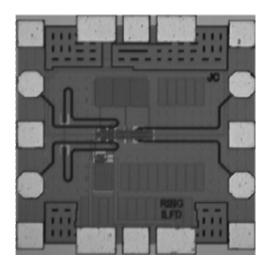


Fig. 9. Microphotograph of the fabricated three-stage injection-locked ring oscillator.

From the above analysis, a large tuning range for the variable resistance R_T is desirable to maximize the input range of the frequency divider. However, the resulting nonuniform gate delay of the third stage complicates the condition for optimum injection phases as derived in the previous section. In order to alleviate the nonuniform characteristics, the gate delays of the three stages are selected to be identical in the center of the frequency tuning range. As a result, a constant phase difference for input injections can be applied to enhance the locking range of the frequency divider over the entire operating bandwidth.

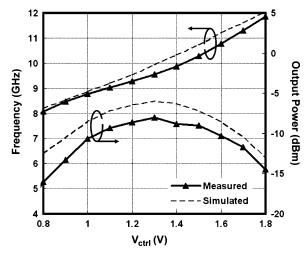


Fig. 10. Measured and simulated tuning characteristics of the three-stage ring oscillator.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The injection-locked ring oscillator is designed and implemented in a 0.18- μ m CMOS technology. Fig. 9 shows the die photo of the fabricated circuit. The oscillator output is buffered by a two-stage cascaded differential amplifier to drive the 50- Ω external loads. The tuning characteristics of the free-running oscillator are depicted in Fig. 10, indicating a frequency tuning range of 4 GHz and a maximum output power of -9 dBm. The frequency division functionality was tested through on-wafer probing with a single-ended input injection. By tuning the free-

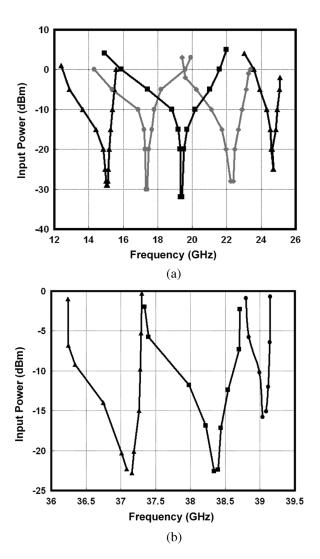


Fig. 11. Measured locking ranges of the wideband frequency divider at various free-running frequencies with single-ended injection. (a) Divide-by-two and (b) divide-by-four operations.

running frequency through the controlled voltage $V_{\rm ctrl}$, the fabricated circuit performs 2:1 and 4:1 frequency division for an input frequency ranging from 13 to 25 GHz and 30 to 45 GHz, respectively. Operating at a free-running frequency of 9.5 GHz, the locking ranges for 2:1 and 4:1 frequency division are 7 and 1.4 GHz, respectively. Fig. 11 shows the input sensitivity curves of the ring oscillator at various free-running frequencies.

To investigate the effect of the multiple-injection technique and the associated phases on the locking range of the frequency divider, the input signals are provided through a hybrid coupler and two phase shifters. The measurement setup is illustrated in Fig. 12. Since the passive components in the setup present significant losses at frequencies beyond 20 GHz, measuring the entire locking range with an arbitrary injection phase becomes extremely difficult. Instead, the minimum required injected power versus the input phase difference for the locked condition in the vicinity of free-running frequency was tested as shown in Fig. 13. For an input frequency of 19 GHz, the optimum injection efficiency for 2:1 frequency division is achieved with a -120° phase difference between the injected signals. On the

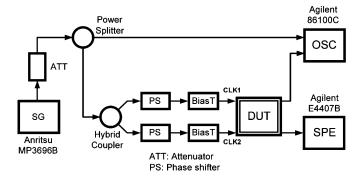


Fig. 12. Measurement setup for multiple-input injection with controlled phases.

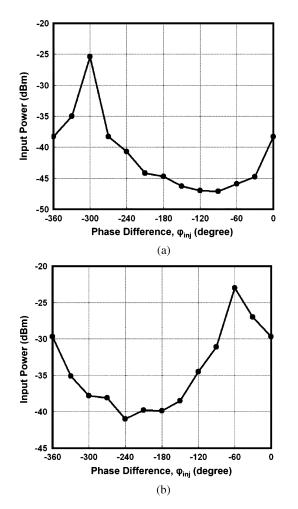


Fig. 13. Measured minimum required input power for injection locking as a function of the input phase difference. (a) Divide-by-two and (b) divide-by-four operations.

other hand, the 38-GHz input signals for 4:1 frequency division exhibit the best injection efficiency with a phase difference of -240° . The measured optimum phase conditions in the multiple-injection technique agree closely with the theoretical derivation and the simulation results. In addition, the measured input sensitivity curves of the injection-locked ring oscillator for divide-by-two and divide-by-four operations are shown in Fig. 14(a) and (b), respectively. Though the measurement on the full locking range of the frequency divider is limited by the

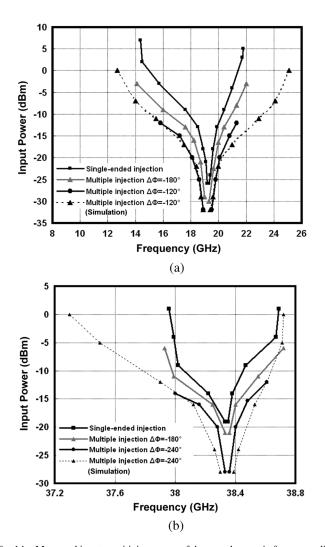


Fig. 14. Measured input sensitivity curves of the superharmonic frequency divider. (a) Divide-by-two and (b) divide-by-four operations.

input injected power and the excess losses from the setup, it is still evident that the injection efficiency is drastically enhanced by the proposed technique at a reduced power level. Circuit simulations indicate that the locking range of the three-stage ring oscillator can be almost doubled by multiple signal injections with the optimum input phases for both 2:1 and 4:1 frequency division compared with the case when single-ended injection is provided.

In addition to the tuning behavior and the locking range, the close-in phase noise of the ring oscillator at a free-running frequency of 9.5 GHz is shown in Fig. 15. At low offset frequencies, the output phase noise is 5.8 dB lower than the input signal source for 2:1 frequency division, while a phase noise reduction of 11.4 dB is achieved for 4:1 frequency division, agreeing closely with the theoretical values of 6 and 12 dB, respectively. However, the phase noise at high offset frequencies is dominated by the ring oscillator itself, leading to degraded performance in both operation modes. Fig. 16 shows the measured input and output waveforms of the fabricated circuit for 2:1 and 4:1 frequency division.

Due to the absence of on-chip inductors, the active area of the divider is only $60\times50~\mu\mathrm{m}^2$. Operated at a 1.8-V supply voltage,

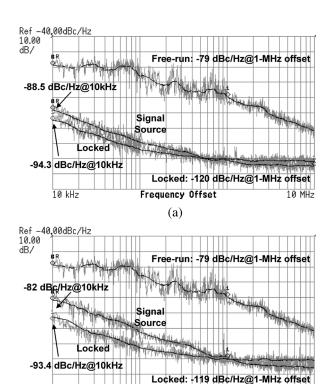


Fig. 15. Measured close-in phase noise of the superharmonic frequency divider. (a) Divide-by-two and (b) divide-by-four operations.

Frequency Offset

(b)

10 kHz

the power consumption of the ring oscillator core varies from 12 to 24 mW within the entire frequency tuning range. The circuit performance of the fabricated circuit is summarized in Table I along with results from the state-of-the-art CMOS frequency dividers for comparison.

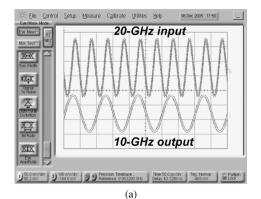
In the proposed circuit technique, multiple-input injection with a specific phase difference is required to maximize the locking range of the dividers. Typically, the input injections can be generated by multi-phase oscillators or delay stages in a fully integrated system. Based on the measurement results in Fig. 13, it is observed that injection efficiency is not very sensitive to the phase error in the vicinity of the optimum condition. Therefore, enhanced circuit performance for superharmonic frequency division can still be achieved even if exact phase control is not available in practical circuit implementations.

V. CONCLUSION

The locking range of the injection-locked ring oscillator with various injection topologies is investigated. By providing an optimum input phase condition in the multiple-injection technique, the locking range of the frequency dividers is effectively enhanced for high-speed applications. To verify the proposed technique, a wideband frequency divider based on a three-stage injection-locked ring oscillator is implemented in a standard CMOS process. Good agreements between the theoretical analysis and the experimental results are demonstrated at frequencies in the tens of gigahertz.

Ref	[2]	[3]	[4]	[15]	[16]	[17]	[18]	This
Technology	0.35-μm CMOS	0.13-µm CMOS	0.18-µm CMOS	0.2-μm CMOS	0.13-µm CMOS	90-nm CMOS	0.18-μm C M OS	0.18-μm CMOS
Function	1:2	1:2	1:4	1:2	1:2	1:4	1:3	1:2/1:4
Input Frequency	19 GHz	40 GHz	40 GHz	55 GHz	38 GHz	70 GHz	18 GHz	20 / 40 GHz
Bandwidth	1.35 GHz	1.5 GHz	2.3 GHz	3.2 GHz	3.5 GHz	8.7 GHz	3.2 GHz	12 / 15 GHz
Supply	1.2 V	1.5 V	2.5 V	1.0 V	1.8 V	0.5 V	1.8 V	1.8 V
P _{diss}	1.2 mW	3 mW	30.8 mW	10.1 mW	12 mW	2.75 mW	4.6 mW	< 24 mW

TABLE I
PERFORMANCE SUMMARY OF THE CMOS INJECTION-LOCKED RING OSCILLATORS



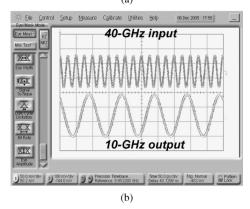


Fig. 16. Measured input and output waveforms of the superharmonic frequency divider. (a) Divide-by-two and (b) divide-by-four operation. (horizontal scale: 50 ps/div., vertical scale: 100 mV/div. for the input and 50 mV/div. for the output)

APPENDIX

From (20) and (23), the optimum input phase differences to achieve the maximum locking range for 2:1 and 4:1 frequency division in a three-stage ring oscillator are $-2\pi/3$ and $-4\pi/3$, respectively. The phase difference is equivalent to the product of the division ratio and the phase shift contributed by the individual stages without input injections. This relationship can be further extended for general cases with higher division ratios. For example, the optimum input phase difference for the three-stage ring oscillator to perform 6:1 frequency division can be presented as $6 \times (-4\pi/3)$ or equivalently -2π , which agrees

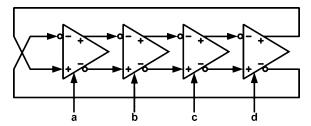


Fig. 17. Simplified circuit schematic of the four-stage injection-locked ring oscillator.

TABLE II
SIMULATED LOCKING RANGE OF THE FOUR-STAGE RING OSCILLATOR

2:1 Frequency Division (V_{in} = 120 m V_{pp})										
a	b	c	d	Locking Range (%)	Normalized					
0	-	-	-	5.83	1					
0	$-\pi/2$	-	-	11.50	1.97					
0	-	-π	-	11.33	1.94					
0	$-\pi/2$	-π	-	16.58	2.84					
0	$-\pi/2$	-π	$-3\pi/2$	21.42	3.67					
0	$+\pi/2$	$+\pi$	$+3\pi/2$	2.75	0.47					
4:1 Frequency Division (V_{in} = 120 m V_{pp})										
a	b	c	d	Locking Range (%)	Normalized					
0	-	-	-	1.125	1					
0	$-\pi/2$	-π	$-3\pi/2$	0.01	0.01					
0	-	0	-	2.42	2.15					
0	-π	0	-π	5.33	4.74					

with the results from circuit simulation. The similar conclusion also applies to the four-stage ring oscillator as shown in Fig. 17. Circuit simulation indicates that the optimum phase differences for 2:1 and 4:1 frequency division are $2 \times (-5\pi/4)$ and $4 \times (-5\pi/4)$, respectively. Table II shows the simulation results of the four-stage ring oscillator for various input injection topologies, demonstrating consistent results with the prediction.

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