A Hybrid Method to Eliminate Leakage Current and Balance Neutral Point Voltage for Photovoltaic Three-Level T-Type Inverter

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***Abstract*- Nowadays, neutral point voltage (NPV) balancing control and leakage current (LC) reduction methods are considered to improve the reliability of transformerless three-level T-type ($3LT^2$) inverter. MVPWM method can control the inverter operation to eliminate the LC; however, is powerless to balance the NPV. Alternatively, DPWM methods can be implemented to balance the NPV. In this paper, a hybrid method for transformerless $3LT^2$ inverter is proposed to simultaneously minimize the LC and accomplish balancing control in case of NPV unbalancing. The proposed method applies MVPWM switching patterns to eliminate LC while the NPV is balanced. If the NPV becomes unbalanced, it applies specific switching patterns of the DPWM methods as alternative patterns to balance the NPV with minimal LC. Accordingly, the proposed method not only maintains the LC elimination advantage of the MVPWM method but also realizes the NPV balancing capability without any topology modification or adding electrical components. Noteworthy, even the NPV balancing is accomplished with minimal flow of the LC. The proposed method is carrier-based PWM, which shortens execution time and simplifies practical implementation. Experimental tests have been accomplished and results demonstrate the effectiveness of the proposed method on adding the NPV balancing capability with minimal LC to the MVPWM method.[1]**

***Index Terms*—PV, Three-level T-type inverter, Leakage current elimination, Common-mode voltage, Neutral point voltage balancing, carrier-based PWM, MVPWM, DPWM.**

I. INTRODUCTION

Nowadays, renewable energy sources are widely utilized considering economic benefits, environmental issues, and energy security [1]. Among renewable energy sources, the photovoltaic (PV) systems have attracted much attention due to the appropriate size, noiseless performance, and simple installation capability in the AC power system [2].

The PV system employs a power conversion apparatus to be integrated into the AC power system. This power conversion apparatus, which so-called PV inverter, converts the DC output of the PV array into AC form with utility frequency. PV inverters are categorized into stand-alone and grid-connected types [3]. Stand-alone inverters draw electrical power from batteries charged by PV arrays to supply the off-grid power system. The grid-connected inverter that does not interact with any battery converts the PV-generated electrical power to inject into the AC grid directly. Among grid-connected PV inverters, multiple-level inverters are preferred because of reducing total harmonic distortion (THD) and requiring a smaller output filter. Multilevel inverters are classified into cascaded H-bridge inverters, flying capacitor inverters, and Neutral-Point-Clamped (NPC) inverters [4]-[6]. Of these, the three-level NPC inverters are the most employed in large-scale applications from hundreds of KW to several MW. Recently, three-level advanced NPC inverters, which are known as three-level T-type ($3LT^2$) inverter, are introduced to apply in small-scale applications with high-performance requirements [7]. Noteworthy, that the $3LT^2$ inverter is a well-accepted PV inverter of grid-connected type due to outstanding performance in medium switching frequencies and applications of tens KW [8]-[10]. Indeed, the $3LT^2$ inverter is used to synergize the advantages of the three-level NPC inverter and two-level inverter in terms of efficiency increase and THD reduction [11], [12].

The DC-link of the $3LT^2$ inverter consists of two capacitors in series to provide a neutral voltage point. If the upper capacitor's voltage of the DC-link is not equal to the lower capacitor's voltage, the neutral point voltage (NPV) becomes unbalanced. The NPV unbalance may occur due to the difference between the DC-link capacitor considering the manufacturing process, the difference between switching device characteristics, the effect of different switching states on the NPV [13]. The NPV unbalance shortens the DC-link capacitor's lifetime [14], [15], increases the THD of output current, and causes extra voltage stress on switching devices [16]. Moreover, it may trigger predesigned over-voltage protection [17], which leads the inverter operation to fail. Consequently, various pulse width modulation (PWM) methods for the NPV balance were proposed which can be categorized into carrier-based PWM (CB-PWM) [18]-[20] and space vector PWM (SV-PWM) [21], [22].

The NPV balancing methods of SV-PWM or CB-PWM type utilize the dwell time recalculating of voltage vectors or injecting appropriate zero-sequence voltage to balance the NPV respectively. Practically, CB-PWM methods are preferred to shorten the execution time and facilitate practical implementation. Among CB-PWM methods, the methods

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based on discontinuous pulse width modulation (DPWM) have attracted much attention since they can provide NPV balancing capability and loss reduction simultaneously [20]. The DPWM methods are categorized into 30°-DPWM, 60°-DPWM, and 120°-DPWM according to the width of discontinuous pulses [23]. Literature [20] proposed an NPV balancing method based on 60°-DPWM in which the width of the positive and negative discontinuous pulses is modified considering the NPV condition. When the NPV should be increased, this method increases the positive discontinuous pulses to more than 60° and decreases the negative pulses to less than 60°. The reverse trend holds when the NPV should be decreased. To avoid complex and time-consuming calculations of modifying discontinuous pulses, [24] proposed a hybrid method for balancing the NPV based on the concept of the 60°-DPWM and redundant state vectors. This method does not use the complex calculation for modifying discontinuous pulses, and it only passes switching signals through a conditional block to redistribute small voltage vectors considering the NPV state. The NPV balancing method can be even more simplified if the 120°-DPWM of DPWMMAX and DPWMMIN types are used in a hybrid manner [25]. The DPWMMAX and DPWMMIN respectively cause the NPV to increase and decrease without any requirement of discontinuous pulses modification or using conditional block. Moreover, the DPWMMAX and DPWMMIN can provide a faster dynamic response for NPV balance recovery as compared to 60°-DPWM based methods. Note, that DPWMMAX extends the width of the positive discontinuous pulses to 120° and the negative of those to zero. As a result, increasing the NPV is accomplished as fast as possible. Likewise, the DPWMMIN implementation can decrease the NPV faster since it lengthens the width of the negative discontinuous pulses to 120° and the positive of those to zero.

After considering the unbalanced NPV problem in the DC-link of the $3LT^2$ inverter and suggesting the proper solution to that, the possible challenges in the AC-side of the $3LT^2$ inverter should be investigated. The AC side of the $3LT^2$ inverter can be connected to the grid by a transformer interface or transformerless. The transformer interface steps up the output voltage of the inverter to adapt to the AC grid; moreover, it isolates the PV system from the AC grid which, in turn, prevents DC components injection into the AC grid. Despite the advantages of the transformer interface, the transformerless connection is recently taken into consideration to increase efficiency and decrease cost, size, and weight [26]. However, the transformerless connection causes the PV system is subjected to the leakage current (LC) due to the lack of galvanic isolation of the transformer [27]. The LC causes electromagnetic inferences problems, output current distortion, conduction losses increase and safety problems [28], [29]. Furthermore, the LC specifically decreases output power and lifetime of PV panels in the PV generation systems [30]. Accordingly, the RMS value of the LC has been limited to 300 mA by the standard of the PV systems integration [31].

Noteworthy, the LC flows into the ground because of the voltage difference between the PV panel and the PV grounded frame [32]. The LC amount depends on the common-mode voltage (CMV) which refers to the voltage difference between the neutral point of the inverter DC-link and the ground of the AC system [33]. The CMV amount is changed by different states of the inverter switches that, in turn, cause the CMV to include an AC component [34]. Importantly, the AC component that is so-called CMV ripple leads the LC to flow. The higher the amplitude of the CMV ripple is, the greater the LC flow. Literature [35] proposed an NPV balancing method with reduced CMV, in which the zero vectors of [PPP] and [NNN] type are removed to limit the CMV magnitude to one-third of DC-link voltage. However, it does not distinguish and modify the switching sequences which cause high amplitude CMV ripple. As a result, although the CMV amount is limited, the LC could stay large since the LC amplitude is proportional to CMV ripple amplitude, not only the CMV amplitude.

Generally, the LC reduction methods have been proposed based on modifying the topology or PWM method of the $3LT^2$ inverter [36]-[42]. In [36], [37], The LC reduction was simply accomplished by connecting neutral points of the DC-link and output filter. This connection provides a bypass path to reduce the LC that flows to the ground. Nevertheless, this method only is practicable for inverters with shunt capacitors in the output filter. In another method, the neutral points of the DC-link connected to the neutral point of the AC grid to provide constant CMV and eliminate the LC [38]. However, the connection between the neutral points is practically accomplished through a parasitic inductance that may cause voltage oscillation with high frequency, and the LC exceeds the standard value [39].

PWM-based methods for LC reduction are categorized into the CB-PWM and SV-PWM methods. In [40], an SV-PWM method was proposed to reduce the LC by using the large, medium, and zero voltage vectors. This method interacts with an auxiliary PWM method that uses the large, medium, and small vectors to balance the NPV. However, this method only decreases the LC to half as compared to the conventional SV-PWM that uses all types of vectors to generate the output voltage. In [2] and [41], an SV-PWM method was presented by using only the medium voltage vectors to eliminate the CMV ripple and LC completely. However, this method restricts the minimum output voltage of the inverter and it may disturb the synchronization of inverter output voltage and AC system voltage in Low voltage ride through (LVRT) condition. Subsequently, the medium vector PWM (MVPWM) method of SV-PWM type was proposed which composes output voltage by using the medium vectors and one zero vector to eliminates the LC without any limitation for the minimum output voltage. This SV-PWM method can transform into an equivalent CB-PWM method to simplify implementation. Literature [42] proposed the MVPWM method of CB-PWM type to completely suppress the CMV ripple and the LC. However, this method is powerless to balance the NPV that is an effective factor of inverter performance and components' lifetime. As a result, the MVPWM method should be developed by employing an appropriate NPV balancing method to qualify as a proper modulation method. Accordingly, Literature [43] proposed a balancing control of NPV for MVPWM-controlled $3LT^2$

inverter with minimal flow of the LC. Noteworthy, that the present paper is the complete and detailed version of [43] while the CMV and NPV analysis based on 3LT^2 inverter topology, description of MVPWM and DPWM methods of CB-PWM type, the limitation of the proposed method, a comprehensive experimental validation, and experimental results analysis and discussion are also included.

In this paper, a hybrid modulation method, which is called developed medium vector PWM (DMVPWM), is proposed based on integrating well-known MVPW and DPWM methods. The proposed method maintains the LC elimination advantage of the MVPWM method; moreover, it realizes the NPV balancing capability with minimal flow of the LC by employing the DPWM method of DPWMMAX and DPWMMIN types. This method controls the inverter operation in the normal and unbalanced modes as follows.

Normal operating mode: The proposed method applies the switching patterns of the MVPWM to eliminate the LC while the NPV is balanced (steady-state period). In this mode, the output voltage of the inverter is composed by using the equivalent switching states of one zero (V_0[OOO]) and six medium voltage vectors to avoid the CMV ripple and flow of the LC.

Unbalanced operating mode: If the NPV becomes unbalanced, certain switching patterns of the MVPWM replace with specific switching patterns of the DPWMMAX or DPWMMIN method. These specific switching patterns, which cause the low-amplitude CMV ripple, are recognized considering CMV analysis of the DPWMMAX or DPWMMIN balancing method to reduce the LC even during the NPV balancing process (transient period).

Experimental tests and simulation studies have been accomplished and their results were compared with the results of conventional methods. The comparison of results demonstrates the effectiveness of the proposed method in providing the capabilities of LC minimization and NPV balancing simultaneously.

Considering the hybrid proposed method, the following can be expressed as contributions of the current paper.

1) The proposed method is introduced based on integrating MVPWM and DPWM well-known methods and due to that, it is easy to understand. Moreover, this method is a CB-PWM type that shortens execution time and simplifies practical implementation.

2) The proposed method simultaneously provides the capability of LC suppression and NPV balancing without any topology modification or adding electrical components. As a result, the proposed method can be easily implemented as an alternative method in existing PV generation systems.

3) The proposed method prevents the NPV unbalance which is the cause of switches and dc-link capacitors failure. Therefore, it increases the lifetime of the 3LT^2 inverter.

4) The proposed method not only eliminates the flow of LC while the NPV is balanced (steady-state period) but also suppresses the LC during the NPV balancing process (transient period). Consequently, it particularly causes the LC of the PV system to minimize which, in turn, leads the lifetime of PV panels to extend.

5) The proposed method authorizes the transformerless topology to apply due to the LC minimization. Hence, it causes the efficiency and power density of the PV system to increase.

The rest of this paper is organized as follows. In section II, CMV and NPV are described and analyzed based on 3LT^2 inverter topology. In section III, the MVPWM method of carrier-based type, which can eliminate the LC, is explained. Furthermore, the DPWMMAX and DPWMMIN methods, which can be used for NPV balancing, are described. In section IV, the hybrid proposed method, which includes normal and unbalanced operating modes, is introduced. In section V, the simulation and experimental results are presented and compared with conventional methods. Finally, the paper is concluded in Section VI.

II. CMV AND NPV ANALYSIS BASED ON THE 3LT^2 INVERTER TOPOLOGY

In this section, CMV and NPV are introduced considering the topology of the transformerless 3LT^2 inverter. Moreover, the CMV and NPV are analyzed for all switching states of the 3LT^2 inverter.

A. The CMV analysis

Fig.1 shows the transformerless 3LT^2 inverter in which parasitic capacitor (C_{PV}) and leakage resistor (R_g) model leakage paths between the DC-link of the inverter and the ground. The amount of the LC is proportional to the CMV which is a zero sequence component. The CMV refers to a voltage difference between the grounded nods of an interconnected system. According to Fig.1, the CMV and LC can be calculated as follows [44].

$$V_{CM} = V_{go} = \frac{V_{ao}+V_{bo}+V_{co}}{3} \tag{1}$$

$$I_{LC} = \frac{-3}{Z_f + 3Z_{leakage}} V_{gN} = \frac{-3}{Z_f + 3Z_{leakage}} \left(V_{CM} + \frac{V_{dc}}{2}\right) \tag{2}$$

Where V_{CM} is the CMV and Z_{leakage} is the combined impedance of C_{PV} and R_g. Z_f and I_{LC} are impedance of output filter and total LC respectively.

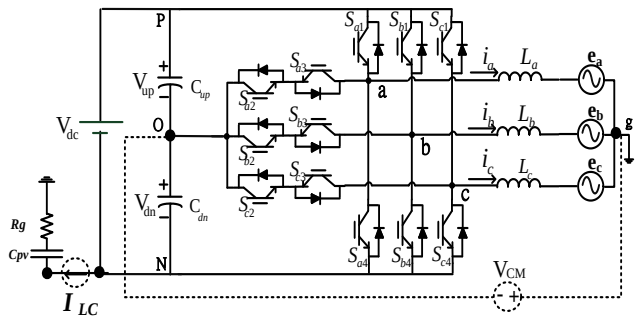


Fig. 1. 3LT^2 inverter of transformerless type

In SV-PWM methods, the command voltage can be composed of voltage vectors of zero, small, medium, and large types that are listed in Table I. The switching state, which generates each of the voltage vectors, leads to an amount of the CMV. Therefore, the CMV amount changes depending on switching patterns of the PWM method that, in turn, causes CMV ripple. The higher the amplitude of the CMV ripple is, the greater the LC flow. Table II lists the CMV amount of all switching states regarding the $3LT^2$ inverter. According to Table I and Table II, the existence of the CMV ripple is unavoidable when the $3LT^2$ inverter operates based on conventional SV-PWM methods since these methods generally use all possible types of voltage vectors to compose the command voltage.

B. The NPV analysis

NPV unbalanced refers to a voltage difference between the upper and lower capacitors of the inverter. The voltage vectors, which are applied to generate the command voltage, affect the voltage of the upper and lower capacitors that, in turn, may unbalance the NPV [44].

The switching state of the large vectors is powerless to change the NPV due to generate the same voltage variation across the upper and lower capacitors. The switching state of the medium voltage vectors affects the NPV depending on AC grid balancing. When a three-phase balanced AC grid is considered, there is no current flow into the neutral point since the equivalent circuit is symmetrical. As a result, the medium voltage vectors are unable to change the NPV of the inverter that is connected to the balanced three-phase grid. The switching state of the zero vectors does not form a loop that includes the DC-link capacitors and the three-phase output of the inverter. Therefore, the zero vectors are powerless to change the NPV.

The switching state of the P-type small vectors reduces the upper capacitor voltage and increases the lower capacitor voltage. The switching state of the N-type small vectors affects the DC-link capacitor voltages conversely. Fig.2 indicates the circumstance of the NPV variation for the switching state of P-type and N-type small vectors.

The dwell time of the P-type and N-type small vectors is directly proportional to the amount of NPV change. If the dwell time of the P-type small vectors is longer than that of the N-type small vectors, the upper capacitor voltage is decreased and the lower capacitor voltage is increased and vice versa. As a result, modifying the dwell time of the P-type and N-type small vectors can control the voltage of the upper and lower capacitors.

TABLE I
THE VOLTAGE VECTORS AND SWITCHING STATES FOR THE $3LT^2$ INVERTER

Vector	Magnitude	Switching pattern	
Zero vector	0	V_0 [PPP] [OOO] [NNN]	
Small vector	$\frac{1}{3}V_{dc}$	P-type	N-type
		V_{1p}[POO]	V_{1n} [ONN]
		V_{2p} [PPO]	V_{2n} [OON]
		V_{3p} [OPO]	V_{3n} [NON]
		V_{4p} [OPP]	V_{4n} [NOO]
		V_{5p} [OOP]	V_{5n} [NNO]
		V_{6p} [POP]	V_{6n} [ONO]
Medium vector	$\frac{\sqrt{3}}{3}V_{dc}$	V_7 [PON], V_8 [OPN], V_9 [NPO], V_{10} [NOP] V_{11} [ONP], V_{12} [PNO]	
Large vector	$\frac{2}{3}V_{dc}$	V_{13} [PNN], V_{14} [PPN] V_{15} [NPN], V_{16} [NPP] V_{17} [NNP], V_{18} [PNP]	

TABLE II
THE CMV AMOUNT FOR THE SWITCHING STATES OF THE $3LT^2$ INVERTER

V_{CM}	Switch state
$-\frac{1}{2}V_{dc}$	V_0 [NNN]
$-\frac{1}{3}V_{dc}$	V_{1n} [ONN] V_{3n} [NON] V_{5n} [NNO]
$-\frac{1}{6}V_{dc}$	V_{2n} [OON] V_{4n} [NOO] V_{6n} [ONO] V_{13} [PNN] V_{15} [NPN] V_{17} [NNP]
0V	V_0 [OOO] V_7 [PON] V_8 [OPN] V_9 [NPO] V_{10} [NOP] V_{11} [ONP] V_{12} [PNO]
$\frac{1}{6}V_{dc}$	V_{1p}[POO] V_{3p} [OPO] V_{5p} [OOP] V_{14} [PPN] V_{16} [NPP] V_{18} [PNP]
$\frac{1}{3}V_{dc}$	V_{2p} [PPO] V_{4p} [OPP] V_{6p} [POP]
$\frac{1}{2}V_{dc}$	V_0 [PPP]

III. CONVENTIONAL METHODS

In this section, the conventional methods of MVPWM and DPWM types are described. These methods are employed to introduce the proposed hybrid method.

A. MVPWM method

The MVPWM method has been proposed to zero the CMV and eliminate the LC [2]. This method generates the output voltage by using two medium-voltage vectors and one zero vector voltage (V_0 [OOO]) during each switching period.

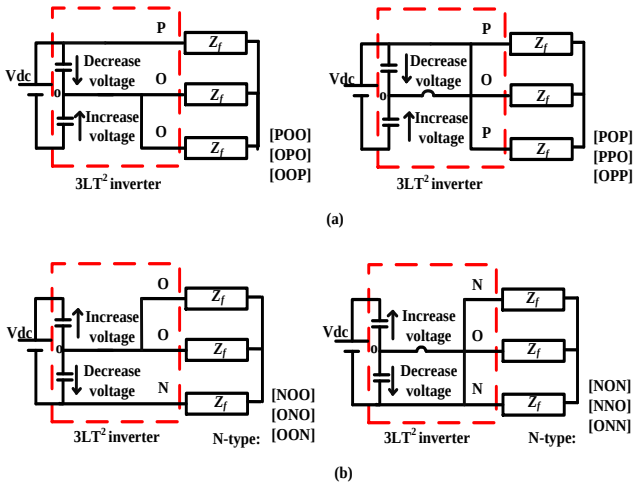


Fig. 2. The NPV variation depending on the switching state of small vectors

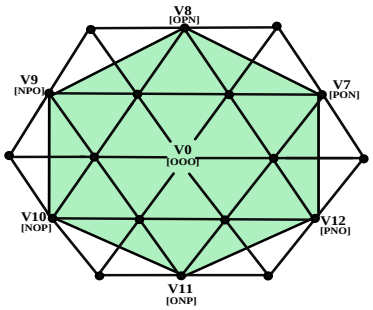


Fig. 3. The MVPWM method space vector diagram

Fig.3 and Fig.4 show the space vector diagram and block diagram of the MVPWM method respectively. It can be seen in Fig.4 that, the input of the comparator block is a three-phase balanced command voltage. This block selects the maximum and minimum values of the command voltage to generate $Vmax$ and $Vmin$ signals as expresses in equation (3).

$$\begin{cases} Vmax = max\,(Va^*, Vb^*, Vc^*) \\ Vmin = min\,(Va^*, Vb^*, Vc^*) \end{cases} \quad (3)$$

Where the $Vmax$ and $Vmin$ signals are the maximum and minimum of the three-phase command voltage respectively.

In addition to the three-phase command voltage, the generated signals by the intersection of two out-of-phase carrier waves with the $Vmax$ and $Vmin$ signals compose the input signals of the phase selector block. The switching signals of the $3LT^2$ inverter are generated by the phase selector block in the MVPWM block [42].

B. DPWM methods

The DPWM methods have been proposed to achieve various goals such as NPV balancing and switching losses reduction. This method reduces switching losses considering the intervals in which the output of each leg is clamped to the positive or negative rail of the inverter's DC-link. Moreover, the DPWM implementation includes a secondary consequence that is the existence assurance of the P-type and N-type small vectors during each switching period. In DPWM methods, the dwell time of the P-type and N-type small vectors can be regulated by modifying the clamping duration of the output legs to the positive or negative rail of DC-link respectively. Therefore, this method can be implemented to balance the NPV since the switching state of the P-type and N-type small vectors cause the NPV to increase and decrease respectively.

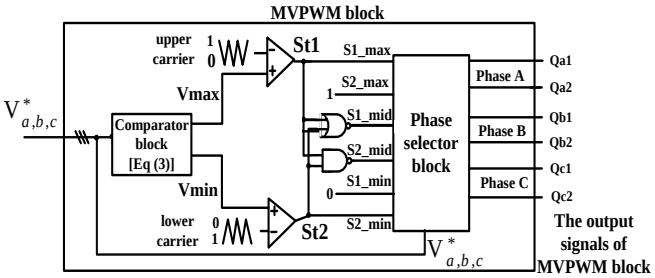


Fig. 4. The block diagram of the MVPWM method

The DPWM methods are categorized into 30°-DPWM, 60°-DPWM, and 120°-DPWM considering that the clamping duration of the output legs to the positive or negative rail [23]. The 30°-DPWM, 60°-DPWM, and 120°-DPWM respectively cause 30°, 60°, and 120° discontinuous intervals to become visible in output phase voltages of the inverter. In 30°-DPWM and 60°-DPWM methods, the discontinuous intervals are typically consistent and equal in the positive and negative half cycles of phase voltage. If the NPV becomes unbalance, the clamping duration to the positive and negative rail of the DC-link is modified to balance the NPV [20]. As a result, the modification of the clamping duration leads the width of discontinuous intervals in the positive and negative half cycles of the output voltage to transiently become inconsistent during the NPV balancing process.

If the DPWM methods are used only as an NPV balancer method, The 120°-DPWM of DPWMMAX and DPWMMIN types can be used in a hybrid manner to avoid complex calculations of modifying the clamping duration and improve the dynamic response for NPV balance control. The DPWMMAX extends the clamping duration so that the width of the positive discontinuous intervals reaches 120° and the negative of those to zero. As a result, only the switching state of P-type small vectors are existence in switching patterns, and increasing the NPV is accomplished as fast as possible. Likewise, the DPWMMIN implementation can decrease the NPV faster since it lengthens the width of the negative discontinuous pulses to 120° and the positive of those to zero.

Fig.5 shows the space vector diagram for the DPWM method of DPWMMAX and DPWMMIN types. Subspaces

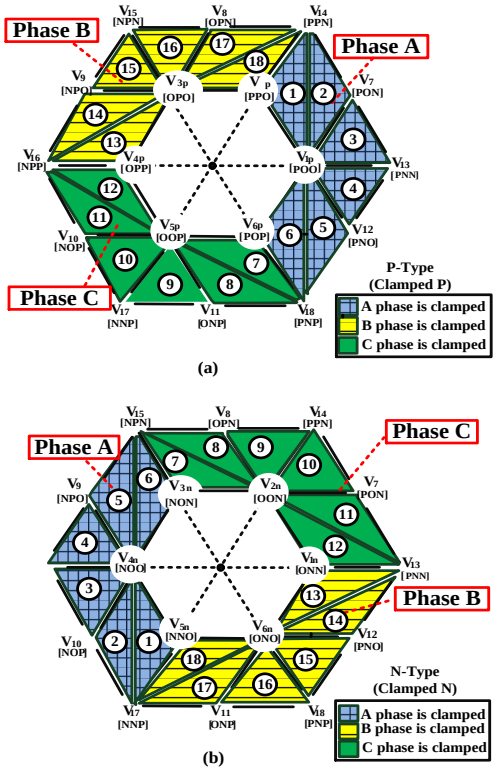


Fig. 5. Space vector diagram of the DPWM methods. (a) DPWMMAX. (b) DPWMMIN.

number 1 to 18 have been distinguished according to the switching patterns of the DPWMMAX and DPWMMIN methods. For example, subspace 1 is considered as a separate subspace in Fig.5(a) since the switching patterns of the DPWMMAX method include ([PPN], [PPO], [POO]) switching sequence. It is worth mentioning that the DPWMMAX and DPWMMIN methods cause the NPV to increase and decrease respectively.

Fig.6 shows the block diagram of the DPWM method that is established by the zero-sequence injection strategy. If the DPWM method is used to balance the NPV, the DPWM injection block generates the zero-sequence wave considering the voltage level of the upper and lower capacitors. Equation (4) express a mathematical relationship to generate the proper zero-sequence wave to balance the NPV [45].

$$V_z = \begin{cases} 1 - V_{max} \; if \; V_{up} > V_{dn} \\ -1 - V_{min} \; if \; V_{up} < V_{dn} \\ 0 \qquad if \; V_{up} = V_{dn} \end{cases} \tag{4}$$

Where V_z is the zero-sequence wave and V_{max} and V_{min} are the maximum and minimum values of command voltage respectively.

In the DPWMMAX and DPWMMIN methods, the command voltage is composed of small, medium, and large voltage vectors. Switching states that generate these types of voltage vectors lead to different CMV amounts that, in turn, cause the CMV ripple to exist. The CMV amount for subspaces 1 to 6 of the DPWMMAX and DPWMMIN space vector diagrams, which are shown in Fig.5, are respectively listed in Table III and Table IV. According to Table III and Table IV, the amplitude of the CMV ripple for subspaces 3 and 4 is twice as much as that of subspaces 1, 2, 5, and 6. Likewise, the CMV analysis is accomplished to determine subspaces with the high-amplitude ripple of CMV. The high-amplitude CMV ripple subspaces are subspaces number 3,4,9,10,15 and 16 for the DPWMMAX and DPWMMIN methods.

TABLE III
THE CMV ANALYSIS FOR SUBSPACES 1 TO 6 OF THE DPWMMAX SPACE VECTOR DIAGRAM

Subspace (switching sequence) number	The First state of switches	CMV amount V_{CM}	The second state of switches	CMV amount V_{CM}	The third state of switches	CMV amount V_{CM}	amplitude of CMV ripple
1	[PPN]	$\frac{1}{6}V_{dc}$	[PPO]	$\frac{1}{3}V_{dc}$	[POO]	$\frac{1}{6}V_{dc}$	$\frac{1}{6}V_{dc}$
2	[PPN]	$\frac{1}{6}V_{dc}$	[PON]	0	[POO]	$\frac{1}{6}V_{dc}$	$\frac{1}{6}V_{dc}$
3	**[PNN]**	$\mathbf{-\frac{1}{6}V_{dc}}$	**[PON]**	**0**	**[POO]**	$\mathbf{\frac{1}{6}V_{dc}}$	$\mathbf{\frac{2}{6}V_{dc}}$
4	**[PNN]**	$\mathbf{-\frac{1}{6}V_{dc}}$	**[PNO]**	**0**	**[POO]**	$\mathbf{\frac{1}{6}V_{dc}}$	$\mathbf{\frac{2}{6}V_{dc}}$
5	[PNP]	$\frac{1}{6}V_{dc}$	[PNO]	0	[POO]	$\frac{1}{6}V_{dc}$	$\frac{1}{6}V_{dc}$
6	[PNP]	$\frac{1}{6}V_{dc}$	[POP]	$\frac{1}{3}V_{dc}$	[POO]	$\frac{1}{3}V_{dc}$	$\frac{1}{6}V_{dc}$

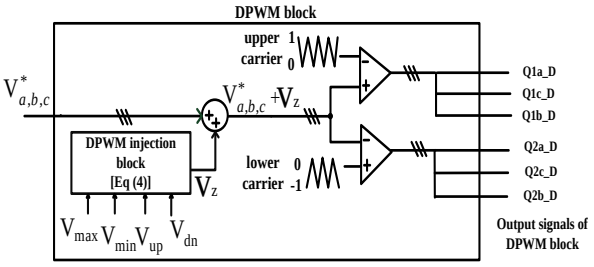


Fig. 6. The block diagram of the DPWM methods

IV. PROPOSED METHOD

In this section, considering the strengths of the conventional MVPWM and DPWM methods a hybrid modulation method is introduced. The MVPWM benefits the LC elimination; however, it suffers from the deficiency of NPV balancing capability. On the other hand, the DPWM methods can be implemented to balance the NPV. Accordingly, the hybrid DMVPWM method is proposed to synergize the strengths of MVPWM and DPWM methods and overcome the drawback of the MVPWM method.

A. Proposed method description

Fig.7 shows the flowchart of the hybrid proposed method. At first, the upper and lower capacitors are compared in terms of voltage magnitude. When the voltage of the upper and lower capacitors is equal (the NPV is balanced), the proposed method applies the switching patterns of the conventional MVPWM method to suppress the CMV ripple which, in turn, causes the LC to eliminate (normal operating mode). The space vector diagram for normal operating mode is the same as the MVPWM space vector (see Fig.3).

If the voltage of the upper and lower capacitors becomes unequal (the NPV is unbalanced), the certain switching patterns of the MVPWM replace with the low-amplitude CMV ripple

TABLE IV
THE CMV ANALYSIS FOR SUBSPACES 1 TO 6 OF THE DPWMMIN SPACE VECTOR DIAGRAM

Subspace (switching sequence) number	The First state of switches	CMV amount V_{CM}	The second state of switches	CMV amount V_{CM}	The third state of switches	CMV amount V_{CM}	amplitude of CMV ripple
1	[NPN]	$-\frac{1}{6}V_{dc}$	[NON]	$-\frac{1}{3}V_{dc}$	[NOO]	$-\frac{1}{6}V_{dc}$	$\frac{1}{6}V_{dc}$
2	[NPN]	$-\frac{1}{6}V_{dc}$	[NPO]	0	[NOO]	$-\frac{1}{6}V_{dc}$	$\frac{1}{6}V_{dc}$
3	**[NPP]**	$\mathbf{\frac{1}{6}V_{dc}}$	**[NPO]**	0	**[NOO]**	$\mathbf{-\frac{1}{6}V_{dc}}$	$\mathbf{\frac{2}{6}V_{dc}}$
4	**[NPP]**	$\mathbf{\frac{1}{6}V_{dc}}$	**[NOP]**	0	**[NOO]**	$\mathbf{-\frac{1}{6}V_{dc}}$	$\mathbf{\frac{2}{6}V_{dc}}$
5	[NNP]	$-\frac{1}{6}V_{dc}$	[NOP]	0	[NOO]	$-\frac{1}{6}V_{dc}$	$\frac{1}{6}V_{dc}$
6	[NNP]	$-\frac{1}{6}V_{dc}$	[NNO]	$-\frac{1}{3}V_{dc}$	[NOO]	$-\frac{1}{6}V_{dc}$	$\frac{1}{6}V_{dc}$

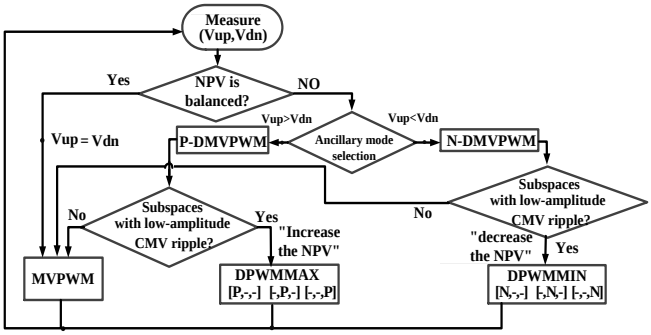


Fig. 7. The flowchart of the proposed method

switching patterns of the DPWMMAX or DPWMMIN method to accomplish the NPV balancing process with minimal LC (unbalanced operating mode). In this regard, the unbalanced operating mode can be divided into the following ancillary modes.

1) P-DMVPWM ancillary mode: When the upper capacitor voltage is greater than the lower one, the low-amplitude CMV ripple switching patterns of the DPWMMAX are replaced with the MVPWM patterns to compose the command voltage. This replacement causes the switching state of the P-type small vectors to exist among switching patterns. The switching state of the P-type small vectors causes the upper capacitor voltage to decrease and the lower capacitor voltage to increase. The P-type developed medium vector PWM (P-DMVPWM) title is selected to mention the ancillary operating mode in which the integration of the DPWMMAX and MVPWM is specifically accomplished. Fig.8(a) shows the space vector diagram for the P-DMVPWM ancillary operating mode graphically.

2) N-DMVPWM ancillary mode: When the lower capacitor voltage is greater than the upper one, switching patterns of the MVPWM replaces with the low-amplitude CMV ripple switching patterns of the DPWMMIN. This replacement leads the switching state of the N-type small vectors to occur in switching patterns. The switching state of the N-type small vectors causes the voltage of the upper and lower capacitors to increase and decrease respectively. The N-type developed medium vector PWM (N-DMVPWM) title is selected to mention the ancillary operating mode in which the integration of the DPWMMIN and MVPWM is specifically performed. Fig.8(b) shows the space vector diagram for the N-DMVPWM ancillary operating mode graphically.

B. Proposed method block diagram

Fig.9 shows the block diagram of the proposed hybrid method. The function of the comparator block, phase selector block, and DPWM injection block have been explained in section III based on conventional methods. The subspace determiner block, signal selector block, and integrator block realize the MVPWM and DPWM method integration to achieve the proposed hybrid method as follows.

The inputs of the subspace determiner block include the command voltage and zero-sequence voltage signal. The zero-sequence voltage signal is the same as the signal which is generated by equation (4) in section III. The output signal of the subspace determiner block is generated based on equation (5).

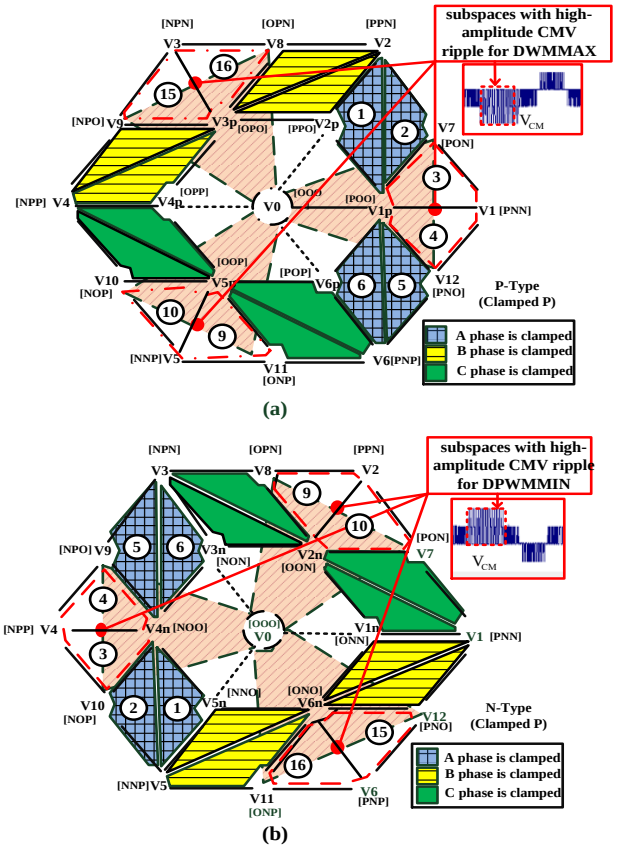


Fig. 8. Space vector diagram for unbalanced operating mode of the proposed method. (a) P-DMVPWM ancillary mode. (b) N-DMVPWM ancillary mode.

$$V_{sub} = mid(V^*{}_{abc} + V_z) \tag{5}$$

Equation (5) selects the middle phase signal among $V^*{}_a + V_z$, $V^*{}_b + V_z$, and $V^*{}_c + V_z$ signals to generate the V_{sub} signal. For example, the V_{sub} is equal to the $V^*{}_a + V_z$ throughout the time that the magnitude of the $V^*{}_a + V_z$ is between the $V^*{}_b + V_z$ and $V^*{}_c + V_z$ signals. Likewise, the V_{sub} can be equal to the $V^*{}_b + V_z$ or $V^*{}_c + V_z$ throughout the time that the $V^*{}_b + V_z$ or $V^*{}_c + V_z$ is the middle signal in terms of magnitude. The inputs of the signal selector block include the V_{sub} and the voltage of the upper and lower capacitors. The signal selector block generates V_{sel} signal based on equation (6).

$$V_{sel} = \begin{cases} 1 \ if \quad ; \ V_{up} = V_{dn} \\ 0 \ if \ \ V_{sub} > 0 \ ; \ V_{up} > V_{dn} \\ 1 \ if \ \ V_{sub} > 0 \ ; \ V_{up} < V_{dn} \end{cases} \tag{6}$$

Where V_{up} and V_{dn} are the voltage of the upper and lower capacitors respectively. Equation (6) is a function defined by three sub-functions and each sub-function is applied for a certain condition of the main function's conditions.

The integrator block generates switching signals according to the V_{sel} signal. Whenever the V_{sel} is equal to 1 the switching signals are generated based on the MVPWM method.

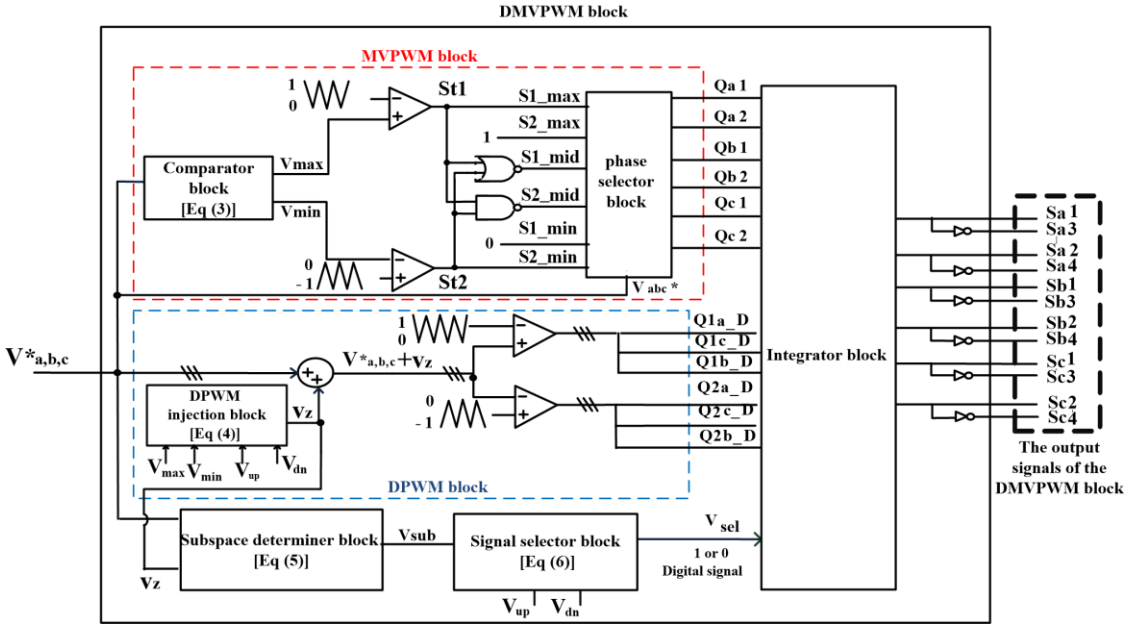


Fig. 9. The block diagram of the DMVPWM proposed method

Whenever the V_{sel} is equal to zero the switching signals are generated based on the DPWMMAX or DPWMMIN method. Accordingly, the proposed method is organized as follows.

The V_{sel} is equal to 1 for the condition ($V_{up} = V_{dn}$) of equation (6), which leads the integrator block to implement the MVPWM method. This condition organizes the normal operating mode to eliminate LC. Conditions ($V_{sub} > 0$; $V_{up} > V_{dn}$) and ($V_{sub} > 0$; $V_{up} < V_{dn}$) organize the P-DMVPWM and N-DMVPWM ancillary modes of the unbalanced operating mode.

1) Condition ($V_{sub} > 0$; $V_{up} > V_{dn}$): The V_{sel} is equal to zero for the condition ($V_{sub} > 0$; $V_{up} > V_{dn}$) of equation (6), which causes the integrator block to specifically implement the DPWMAX or DPWMMIN method to achieve balancing control of the NPV. In this condition, the switching patterns with low-amplitude CMV ripple of the DPWMMAX or DPWMMIN method are implemented considering the voltage state of the upper and lower capacitors. Note, that selecting among the DPWMMAX and DPWMMIN methods as the necessary balancer method has been accomplished by adjusting the zero-sequence signal which is used to generate the V_{sub} signal.

2) Condition ($V_{sub} > 0$; $V_{up} < V_{dn}$): The V_{sel} is equal to one for condition ($V_{sub} > 0$; $V_{up} < V_{dn}$) of the (6), which leads the integrator block to implement the MVPWM method. Although the NPV is unbalanced in this condition, the MVPWM is implemented during the balancing process to reduce the LC. In other words, this condition of the (6) prevents the switching patterns with high-amplitude CMV ripple of the DPWMMAX and DPWMMIN methods to be applied during the NPV balancing process.

Noteworthy, that the command three-phase voltage is the input of the proposed method block according to Fig.9. This command voltage is determined by a power transmission controller to properly deliver the generated power of PV arrays to the AC grid. Fig.10 shows the power transmission controller. It can be seen that the instantaneous power theory [46] is used to calculate the command three-phase output current ($i^*_{(ca,cb,cc)}$) based on the command active power and the three-phase voltage at the AC grid. After calculating the command current, predictive current control is applied to calculate the command three-phase output voltage ($V^*_{(a,b,c)}$). Finally, the command three-phase output voltage is sent as the input of the modulation method.

Fig.11 shows the internal block diagram owned by the predictive current control. when the actual inverter output current does not reach the command value, the command output voltage and subsequently the actual output voltage is changed so that the injected current to the AC grid modify. The three-phase voltage at the AC grid side ($e_{(a,b,c)}$) is constant and determined by upstream. Note, that the predictive current controller uses a proportional gain that determines based on the filter inductance and the sampling frequency of the digital signal processor (DSP) [47].

C. CMV and NPV analysis for the proposed method

In this part, the CMV and NPV of the 3LT^2 inverter are investigated considering the switching patterns of the normal and unbalanced operating modes of the proposed method.

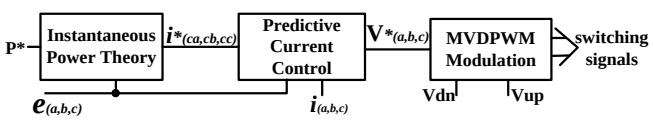


Fig. 10. The block diagram of the power transmission controller

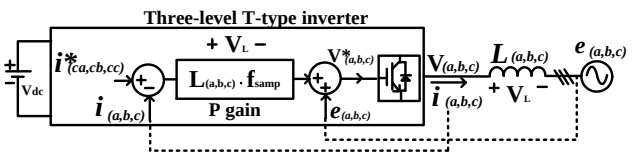


Fig. 11. The internal block diagram owned by the predictive current control

1) CMV analysis: The normal operating mode of the proposed method generates the output voltage by using voltage vectors of medium and zero types. According to the CMV analysis in section II (refer to Table II), the switching states that generate the medium voltage vectors and zero vector (V_0 [OOO]) cause the CMV to experience a constant value and equal to zero. Consequently, the normal operating mode causes the amplitude CMV to zero and CMV ripple to eliminate.

In the P-DMVPWM and N-DMVPWM ancillary modes of the proposed method, the command voltage is composed of zero (only V0 [OOO]), small, medium, and large voltage vectors. Although switching states that generate these types of voltage vectors cause different CMV amounts the switching patterns are organized so that minimize the CMV ripple. The CMV amount for subspaces 1 to 6 of the P-DMVPWM and N-DMVPWM space vector diagrams, which are shown in Fig.8, are respectively listed in Table V and Table VI. It can be seen that the CMV ripple amplitude for subspaces 3 and 4 are is zero. Likewise, the CMV ripple amplitude can be calculated for other subspaces of the ancillary modes space vector diagrams. The subspaces with zero CMV ripple including subspaces number 3,4,9,10,15 and 16 for the P-DMVPWM and N-DMVPWM ancillary modes of the proposed method. By comparing Table V and Table III and also Table VI and Table IV, it can be noted that the P-DMVPWM and N-DMVPWM ancillary modes remove the switching sequence with the high-amplitude CMV ripple of the DPWMMAX and DPWMMIN methods. Accordingly, the P-DMVPWM and N-DMVPWM ancillary modes cause the CMV ripple amplitude limited below one-sixth of the DC-link voltage. Moreover, the maximum amplitude of the CMV is limited to one-third of the DC-link voltage since the switching states of the V0 [NNN] and V0 [PPP] types do not exist in switching patterns.

2) NPV analysis: The normal operating mode of the proposed method composes the command voltage during each switching period by using two medium and one zero vector. This operating mode causes the dwell time of the P-type and N-type small vectors, which are effective in the NPV condition, to equal zero. Accordingly, the voltage of the upper and lower capacitors is not affected in the normal operating mode. In other words, after passing a transient period for the NPV balancing process, the normal operating mode does not cause the NPV unbalanced unless the NPV becomes unbalanced due to a reason except for the PWM method.

The P-DMVPWM ancillary mode of the proposed method composes the command voltage during each switching period by using three voltage vectors that surely involve the P-type small vector, except for the subspaces number 3,4,9,10,15 and 16. This ancillary mode causes the dwell time of the P-type small vectors to increase while the dwell time of the N-type small vectors is zero. Therefore, the NPV is increased when the P-DMVPWM ancillary mode is activated.

On the other hand, the N-DMVPWM ancillary mode composes the command voltage during each switching period by applying three voltage vectors that surely involve the N-type small vector, except for the subspaces number 3,4,9,10,15 and 16. This ancillary mode increases the dwell time of the N-type small vectors while the dwell time of the P-type small vectors is zero. Consequently, the NPV experiences a decrease when the N-DMVPWM ancillary mode is switched on.

D. Power loss analysis for the proposed method

The proposed method includes the normal and unbalanced operating modes according to the proposed method description part. However, the unbalanced operating mode is activated to balance the NPV during transient periods. Therefore, the analysis of the power losses for the proposed method is only performed considering the normal operating mode that controls the $3LT^2$ inverter operation ordinarily (the steady-state period).

The power losses for the $3LT^2$ inverter are mainly caused by power losses of the three-level bridge and output filter. The bridge losses highly depend on the number of switching

TABLE V
THE CMV ANALYSIS FOR SUBSPACES 1 TO 6 OF THE SPACE VECTOR DIAGRAM OF THE P-DMVPWM ANCILLARY MODE

Subspace (switching sequence) number	The First state of switches	CMV amount V_{CM}	The second state of switches	CMV amount V_{CM}	The third state of switches	CMV amount V_{CM}	amplitude of CMV ripple
1	[PPN]	$\frac{1}{6}V_{dc}$	[PPO]	$\frac{1}{3}V_{dc}$	[POO]	$\frac{1}{6}V_{dc}$	$\frac{1}{6}V_{dc}$
2	[PPN]	$\frac{1}{6}V_{dc}$	[PON]	0	[POO]	$\frac{1}{6}V_{dc}$	$\frac{1}{6}V_{dc}$
3	**[PON]**	**0**	**[PNO]**	**0**	**[OOO]**	**0**	**0**
4	**[PON]**	**0**	**[PNO]**	**0**	**[OOO]**	**0**	**0**
5	[PNP]	$\frac{1}{6}V_{dc}$	[PNO]	0	[POO]	$\frac{1}{6}V_{dc}$	$\frac{1}{6}V_{dc}$
6	[PNP]	$\frac{1}{6}V_{dc}$	[POP]	$\frac{1}{3}V_{dc}$	[POO]	$\frac{1}{3}V_{dc}$	$\frac{1}{6}V_{dc}$

TABLE VI
THE CMV ANALYSIS FOR SUBSPACES 1 TO 6 OF THE SPACE VECTOR DIAGRAM OF THE N-DMVPWM ANCILLARY MODE

Subspace (switching sequence) number	The First state of switches	CMV amount V_{CM}	The second state of switches	CMV amount V_{CM}	The third state of switches	CMV amount V_{CM}	amplitude of CMV ripple
1	[NPN]	$-\frac{1}{6}V_{dc}$	[NON]	$-\frac{1}{3}V_{dc}$	[NOO]	$-\frac{1}{6}V_{dc}$	$\frac{1}{6}V_{dc}$
2	[NPN]	$-\frac{1}{6}V_{dc}$	[NPO]	0	[NOO]	$-\frac{1}{6}V_{dc}$	$\frac{1}{6}V_{dc}$
3	**[NPO]**	**0**	**[NOP]**	**0**	**[OOO]**	**0**	**0**
4	**[NPO]**	**0**	**[NOP]**	**0**	**[OOO]**	**0**	**0**
5	[NNP]	$-\frac{1}{6}V_{dc}$	[NOP]	0	[NOO]	$-\frac{1}{6}V_{dc}$	$\frac{1}{6}V_{dc}$
6	[NNP]	$-\frac{1}{6}V_{dc}$	[NNO]	$-\frac{1}{3}V_{dc}$	[NOO]	$-\frac{1}{6}V_{dc}$	$\frac{1}{6}V_{dc}$

commutations and the amount of current at the switching instant. On the other hand, the higher the harmonic distortion of output current is the greater the eddy current losses of the filter are.

The number of switching commutations for the normal operating mode of the proposed method is 16 as compared to 12 of that for the conventional SVPWM method. Furthermore, the normal mode of the proposed method causes greater THD as compared to the SVPWM [2] method which, in turn, leads to higher power loss in the filter. Consequently, the power losses for the proposed method are expected to be higher than the conventional method.

In [48], the detailed results of power losses and overall efficiency for the normal mode of the proposed method (MVPWM method) and conventional methods have been compared for the $3LT^2$ inverter. Literature [48] demonstrates that the additional losses due to the implementation of the MVPWM method have a very low impact on the overall efficiency (less than 0.5%). Conversely, the transformerless topology that becomes applicable by the proposed method can increase the overall efficiency by nearly 2% [49]. Moreover, the proposed method minimizes the leakage current to avoid the potential induced degradation (PID) mechanism of PV panels. Note that the PID mechanism greatly decreases the output of PV panels (increase the power loss to 32%) [30]. Accordingly, it can be concluded that the proposed method implementation can increase the overall efficiency effectively.

E. Limitation of the proposed method

The proposed method limitation can be investigated considering the propitious power factor and maximum modulation index of the proposed method.

1) Modulation index: According to the proposed method description part, the proposed method includes the normal and unbalanced operating modes. Fig.3 and Fig.8 respectively illustrate the space vector diagram of the normal and unbalanced operating modes. It can be seen that the maximum magnitude of the reference vector, $v_{ref,max}$, for both operating modes is reduced considering the MVPWM switching patterns. Accordingly, the $v_{ref,max}$ should be calculated based on the radius of the largest inscribed circle within the colored hexagon shown in the normal operating mode space vector (see Fig.3). Since the length of the colored hexagon side equals the magnitude of the medium voltage vector $(\frac{\sqrt{3}}{3} * v_{dc})$, the $v_{ref,max}$ can be derived as follows.

$$v_{ref,max} = \frac{\sqrt{3}}{3} * v_{dc} * \frac{\sqrt{3}}{2} = \frac{v_{dc}}{2} \quad (7)$$

On the other hand, the modulation index (m_a) can be found from

$$m_a = \sqrt{3} * \frac{v_{ref}}{v_{dc}} \quad (8)$$

The maximum modulation index is determined by Substituting (7) into (8).The maximum modulation indexes $(m_{a,max})$ of the proposed method is 86.6% of that of the conventional SVPWM method. Therefore, the dc-link voltage utilization is decreased as compared to the SVPWM method. The decrease of the dc-link voltage utilization is the inherited limitation of MVPWM based methods, which causes MVPWM based methods to require higher DC-link voltage as compared to the SVPWM method.

Noteworthy, that it is possible to modify the proposed method by removing the MVPWM switching patterns to maximize utilization of DC-link voltage and operate the $3LT^2$ inverter beyond the 0.866 modulation index. However, the proposed method switching patterns approaches the DPWM methods switching patterns and the LC increases so that the advantages of the proposed method in terms of increasing the PV lifetimes and using the transformerless topology are lost.

2) Propitious power factor: The proposed hybrid method is introduced assuming that the transformerless $3LT^2$ inverter delivers the generated power by PV arrays at a high power factor (more than 0.8). The high power factor is generally considered to extract more active power from the PV arrays and decrease the electricity supply cost. However, the PV inverter operation in low power factor is required during LVRT. The LVRT refers to the capability of the PV generation system to stay connected during voltage dip. Since the voltage dip is caused by the shortage of power generation in the distribution system, tripping the photovoltaic generation system during the voltage dip leads the voltage to drop further and may result in chain tripping of other generation systems as well [50]. Consequently, the photovoltaic inverter should be able to properly operate while the low amounts of maximum modulation index and power factor are required.

The proposed method can control the $3LT^2$ inverter to ride through the dip voltage since it does not restrict the minimum modulation index. In other words, the proposed method does not restrict the minimum output voltage of the $3LT^2$ inverter and as a result, it can decrease the output voltage amplitude to become adapted with voltage dip.

Note, that the phase difference of output voltage and current in the low power factor condition causes the neutral point current direction for small vectors to change which, in turn, leads the effect of small vectors on the NPV to change(as compared to the high power factor condition) [35]. If the power factor gets less than a certain amount, the DC-link capacitor voltage may decrease, when it is expected to increase considering the type of applied small vector and vice versa. Consequently, the NPV balancing capability of the proposed method is disturbed during the LVRT due to the low power factor and the unbalanced operating mode of the proposed method should be deactivated temporarily. After the grid fault clearance, NPV balancing can be quickly achieved by activated the unbalanced operating mode. Accordingly, although the NPV balancing capability may be transiently destroyed during RTLV the continuous operating of the $3LT^2$ inverter decrease the risk of the chain reaction of the generation system. Noteworthy, that finding the exact amount of critical power factor and adapting the operating mode of the proposed method for LVRT is beyond the scope of this paper, and LVRT discussion has been considered to address the future scope of the paper.

V. Simulation Study and Experimental Validation

In this section, the parameters of the test system that have been used for experiments and simulation study are introduced. Afterward, the simulation and experimental results for the proposed method are presented and compared with the result of conventional methods. Then, the experimental results for the proposed and conventional method are analyzed comprehensively. Finally, a discussion is provided based on experimental results to introduce specific aspects of the proposed methods.

A. Test system

The experiments and simulations were performed on the PV grid-connected 3LT^2 inverter of transformerless type. Table VII lists parameters of the 3LT^2 inverter and AC grid that have been used for experiments and simulation study. To be more illustrative, Fig.12 shows the prototype of the experimental set-up built for the experimental validation.

The 3LT^2 inverter delivers power to the AC grid at unity power factor, whether for the simulation study or experiments. According to Fig.10 (refer to section IV), the power transmission controller continuously modifies the command voltage of the 3LT^2 inverter to properly deliver power to the AC grid. Consequently, the maximum modulation index is not constant; however, a short-range modulation index can be determined considering that the inverter delivers 2KW at unity power factor to the AC grid. The maximum modulation index is changed between 75% and 80% in simulations and experiments.

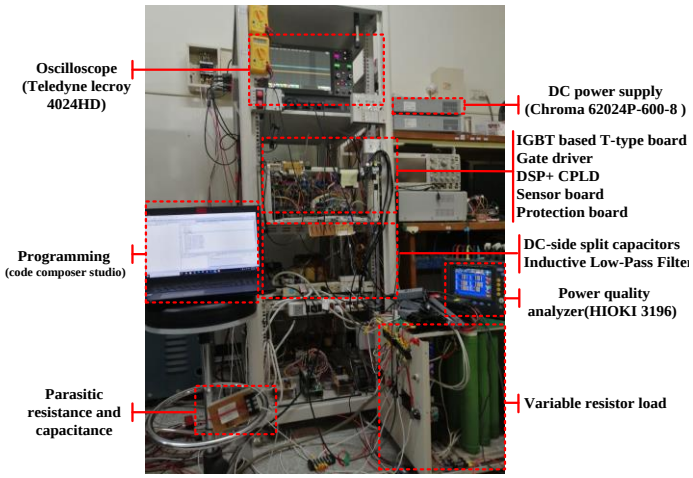


Fig. 12. The prototype of the 3LT^2 inverter

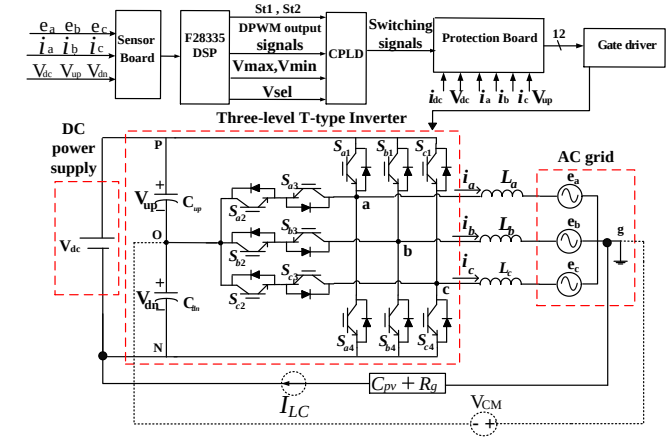


Fig. 13. The Hardware configuration diagram of the experimental set-up

Fig.13 shows the Hardware configuration diagram of the experimental set-up including the 3LT^2 inverter, filter inductors, and switch driver circuit. Furthermore, it demonstrates the respective measurement points of the CMV and LC in experiments. The IGBT switches of the K40T1202 type were used in the 3LT^2 inverter. Chroma 62024P 600-8 DC power supply was connected to the DC-link of the inverter in parallel to operate as an equivalent device to the PV cell array. The HIOKI3196 power quality analyzer measured and analyzed the experiments. The characteristics of the switch driver, output filter, and DC-link capacitors of the 3LT^2 inverter can be expressed as follows.

1) Switch driver circuit: In the switch driver circuit, the TMS320F28335 DSP and Lattice MachXO2 complex programmable logic device (CPLD) cooperated to generate the switching signals. Generally, the following sequence can be mention to clarify signal processing in the switch driver circuit. First, the sensor board measures the actual value of three-phase output voltage and current, input DC voltage, and upper and lower capacitor voltages. Moreover, it scales the measured values to the acceptable range for the analog to digital (ADC) converter of the DSP. Second, the DSP receives the measured analog values and converts them to digital to calculate modulation signals including V_{min} , V_{max} , $V^*_{abc} + V_z$. The calculated modulation signals are sent to the enhanced pulse width modulator (ePWM) module to be compared with carrier waves. Furthermore, the DSP generates the V_{sel} which MVPWM and DPWM methods are integrated based on (see the equation (6)). Finally, the V_{sel} and output signals of the ePWM module (output signals of the DPWM block and St1 and St2 signals from MVPWM block) are sent to CPLD to generate the switching signals. The CPLD performs the required logical operation on signals and sends the required switching signals to the gate driver based on the V_{sel} . Besides, it considers the switching dead time while calculating the complementary of

TABLE VII
THE PARAMETERS OF 3LT^2 INVERTER, AC GRID FOR EXPERIMENTS AND SIMULATION STUDY.

Parameters	Description		Value
E_{abc}	3 Φ line to line voltage (RMS)		220V
f_{fun}	fundamental frequency		60 Hz
f_{sw}	Switching frequency		10kHz
V_{dc}	DC-link voltage		400V
C_{up},C_{dn}	DC-link capacitors	For simulation	560 µF
		For experiments	2240 µF
L_{abc}	Output filter inductor		2mH
P_{out}	The output power of the inverter		2kW
R_g	Parasitic resistance		5Ω
C_{pv}	Parasitic capacitance		10nF

switching signal. Noteworthy, that the protection board uses electromagnetic contactors to disconnect the inverter and the AC grid circuit, and also it cuts off the switching signal to avoid circuit damage and experiment hazards caused by continued operation under faulty circuits.

2) Output filter: The filter is constituted of series inductors to provide a low pass filter. According to the IEEE standard for transmitting electricity to the grid, the THD should be limited to under 5 % [51]. In addition to THD, the inductor voltage drop is also considered to design the filter and, the value of the output filter inductor should be set so that causes a voltage drop of less than 3% of the AC grid voltage [52]. Accordingly, a 2 mH inductor is used as the filter inductance to fulfilling the filter design conditions.

3) DC-link capacitors: The DC-link capacitors of the $3LT^2$ inverter provide a low impedance path for high-frequency currents and stiffen the DC-link (remove the DC voltage fluctuations). The DC-link capacitors are typically dimensionalized based on capacitor ripple current, maximum DC Voltage, and required capacitor ripple voltage [53]. In the test system, the worst-case of the capacitor ripple current equal 2.65 A while the $3LT^2$ inverter injects 2KW to a 220-V(RMS) three-phase electric power at 0.612 modulation index and unity power factor (refer to Appendix I). Accordingly, the electrolytic capacitors of 560 µF / 450V of JAMICON LSW561M2WQ45M type that provide 3.35 A ripple current rating at 120 Hz are connected in series to provides the ripple current rating higher than the worst-case and the DC voltage rating higher than the maximum DC-link voltage. The simulation results indicate that the voltage ripple of the dc-link capacitors is limited under 1.25% of DC-link voltage (5volt) by using the capacitors with 560-µF capacitance. However, the above-mentioned type of capacitors was used in parallel to provide two 2240 µF capacitors for constructing the DC-link of the $3LT^2$ inverter in the experimental set-up. The great capacitance of electrolytic capacitors in the experimental set-up is used to increase the stored energy in the inverter DC-link. This increase of stored energy guarantees the safe operation of the experimental set-up if the output power of the $3LT^2$ inverter is changed. For example, it compensates for the DC-link energy reduction that is caused due to the dynamic response difference between the DC power supply and the $3LT^2$ inverter in the experimental setup.

B. Simulation results

In this part, the simulation results for the proposed and conventional method are presented to highlight the NPV balancing capability with minimal flow of LC. In this regard, the simulation results of the P-DMVPWM and N-DMVPWM ancillary modes of the proposed method are compared with DPWMMAX and DPWMMIN results respectively. Furthermore, the effect of the above-mentioned ancillary modes of the proposed method and conventional methods on the maximum amplitude of the CMV and CMV ripple is investigated graphically. Noteworthy, that the simulation schematic and respective measurement points of the CMV and LC have been shown in Fig.1 in section II and the simulation is run in PSCAD software as follows.

Firstly, the NPV is balanced, and the inverter operation is controlled based on the switching patterns of the MVPWM method. After T0 second, a 100 Ω capacitor connects in parallel to the upper or lower capacitor to increase or decrease the NPV respectively. The NPV unbalancing process takes from T0 second to T1 second and the MVPWM switching patterns are still applied during the unbalancing period. At T1 second, the parallel resistor to the upper or lower capacitor is disconnected and the NPV balancing process is started. Finally, the NPV balance is achieved at T2 second, and the MVPWM switching patterns are again applied after T2 second. The simulation results can be categorized based on the voltage state of DC-link capacitors (NPV voltage) as follows.

1) ($V_{up} > V_{dn}$) state: Fig.14 and Fig.15 show the NPV balancing process based on the P-DMVPWM ancillary mode of the proposed method and DPWMMAX method respectively. It can be seen in Fig.14 that the peak value of the LC reached 1.334A for the DPWMMAX method. Remarkably, The NPV balancing with P-DMVPWM ancillary mode cause the peak value of the LC to decrease to 1.048A in Fig.15.

Fig.16 demonstrate the V_z, V_{sub}, and V_{sel} signals, and graphically compare CMV for the P-DMVPWM ancillary mode and DPWMMAX method. The maximum CMV amplitude is the same for P-DMVPWM ancillary mode and DPWMMAX and equal $\frac{1}{3}V_{dc}$. Importantly, the maximum CMV amplitude ripple is $\frac{1}{3}V_{dc}$ for DPWMMAX and the P-DMVPWM ancillary mode decrease it to $\frac{1}{6}V_{dc}$ to minimize the flow of LC during the NPV balancing process.

2) ($V_{up} < V_{dn}$) state: Fig.17 and Fig.18 show the performance of the N-DMVPWM ancillary mode and DPWMMIN method regarding the NPV balancing process respectively. Fig.17 indicates that the LC peak value reached 1.334A for the DPWMMIN method. The P-DMVPWM

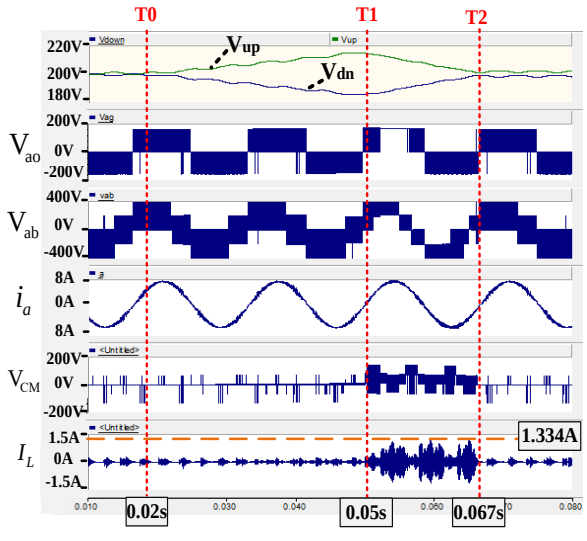


Fig. 14. The NPV balancing process for DPWMMAX method

ancillary mode reduced the LC peak value to 1.048A as shown in Fig.18.

Fig.19 shows the V_z, V_{sub}, V_{sel} signals, and graphically compare CMV for the N-DMVPWM ancillary mode and DPWMMIN method. It can be seen that the maximum CMV amplitude ripple decreased to $\frac{1}{6}V_{dc}$ by the N-DMVPWM ancillary mode, although the maximum CMV amplitude is equal to $\frac{1}{3}V_{dc}$ for both N-DMVPWM ancillary mode and DPWMMIN method.

Noteworthy, that the phase voltage THD variation versus the linear range of modulation index is presented in appendix II for the proposed and conventional methods. The analysis of the THD for the proposed method is only performed considering the MVPWM switching patterns since these switching patterns are applied to controls the $3LT^2$ inverter operation during the steady-state period. More analytical results have been presented regarding THD versus modulation index in [48].

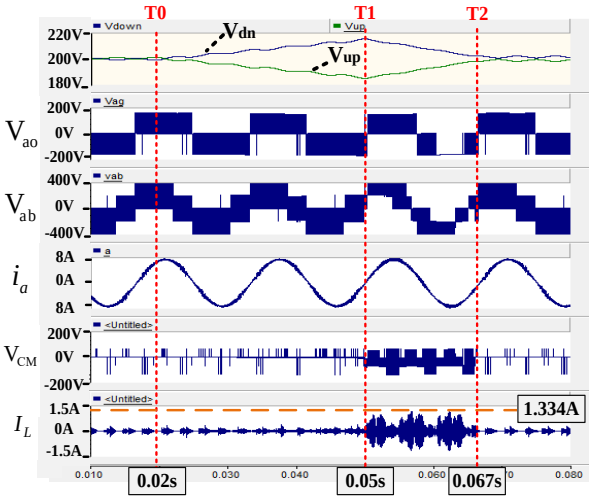


Fig. 17. The NPV balancing process for DPWMMIN

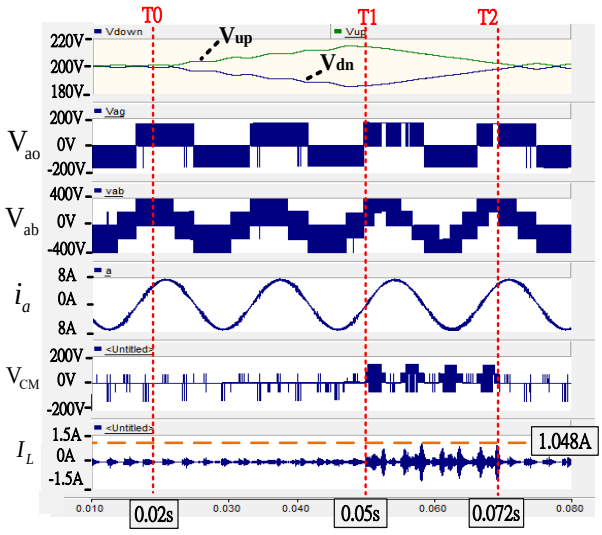


Fig. 15. The NPV balancing process for P-DMVPWM ancillary mode of the proposed method.

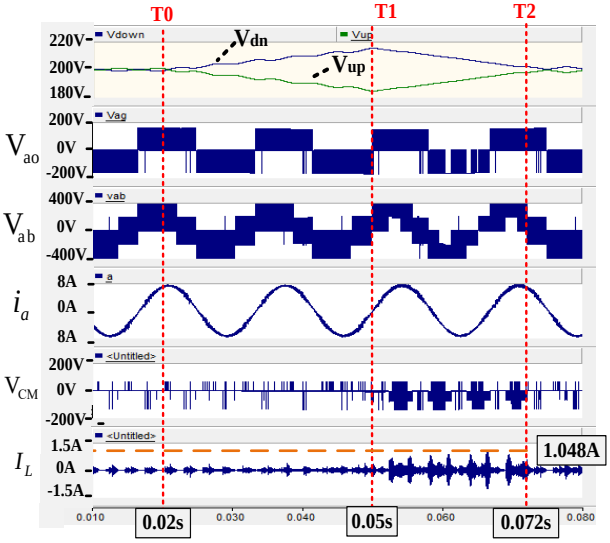


Fig. 18. The NPV balancing process for N-DMVPWM ancillary mode of the proposed method.

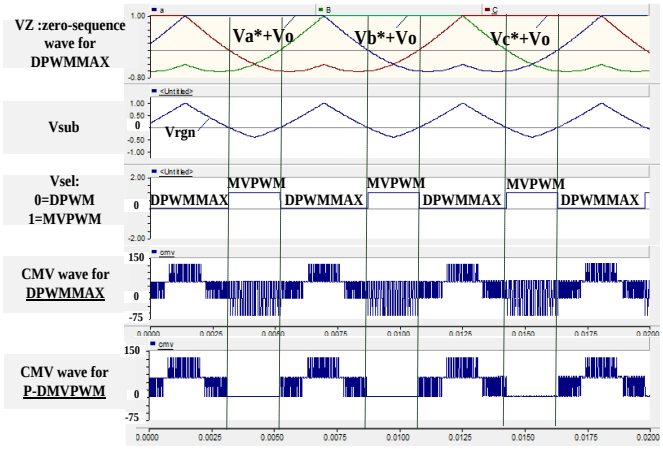


Fig. 16. The signals of control blocks and CMV wave for the P-DMVPWM ancillary mode and DPWMMAX

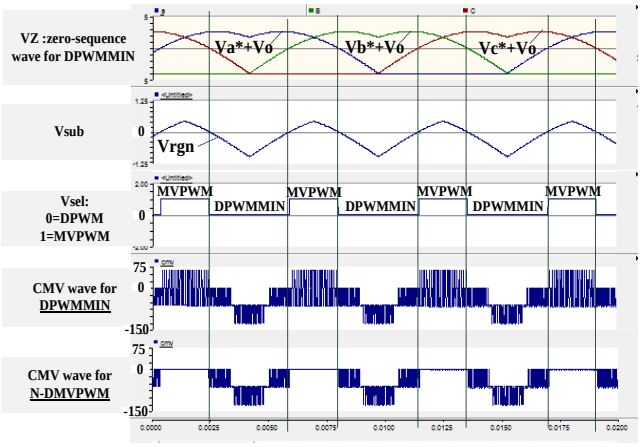


Fig. 19. The signals of control blocks and CMV wave for the N-DMVPWM ancillary mode and DPWMMIN

C. Experimental results

In this part, the DMVPWM proposed method capability for LC minimization and NPV balancing is investigated experimentally. In this regard, three scenarios are considered to achieve the experimental validation as follows. The first scenario considers the balanced NPV state to evaluate the LC elimination capability of the proposed method. In this state, the normal operating mode of the proposed method is implemented and the results of the normal operating mode and opposite disposition PWM (PODPWM) method are compared. The second scenario considers the unbalanced NPV state to prove the NPV balancing with minimal LC capability of the proposed method. Accordingly, the unbalanced operating mode of the proposed method is implemented and the results of this operating mode and DPWMMAX and DPWMMIN methods are compared. The third scenario, which involves periods of unbalanced and balanced NPV state, is considered to demonstrate the proposed method can switch to the normal operating mode automatically, after accomplishing the NPV balancing control. In other words, the third scenario proves the automatic switch capability of the proposed method between unbalanced and normal operating modes.

1) Scenario 1: In this scenario, the DMVPWM proposed method capability for LC elimination is investigated when the NPV is balanced. When V_{up} is equal to V_{dn} , the proposed method operates in normal mode to eliminate the LC. The experimental results of DMVPWM normal operating mode and PODPWM methods are compared. It is worth mentioning that as compared to conventional CB-PWM methods, which generate command voltage by applying all types of voltage vectors, the PODPWM causes the lowest LC to flow [54], [55]. Fig.20 and Fig.21 show phase voltage, CMV, and LC for the DMVPWM normal operating mode and PODPWM methods respectively. The peak and RMS values of the LC for the PODPWM method implementation equaled 1.239A and 219.4mA respectively. The proposed method implementation reduced the peak and RMS values of the LC to 0.902A and 92.9mA respectively. Fig.22 shows the line voltage and current when the inverter operates based on the normal mode of the DMVPWM method.

Table VIII lists the harmonic amounts i_a regarding the MDVPWM and PODPWM methods. Accordingly, the proposed method caused a larger THD amount as compared to the PODPWM method. However, according to the IEEE 1547 standard [51], $3LT^2$ inverters that are operated based on The DMVPWM method are allowed to interconnect the PV system with the AC grid since the DMVPWM implementation causes the THD to remain less than 5%.

TABLE VIII
THE HARMONIC ANALYSIS FOR THE DMVPWM AND PODPWM METHODS

THD% analysis		Phase A harmonic Fast Fourier transform (FFT%)							Total harmonic
Harmonic order		1th	2th	3th	4th	5th	6th	7th	THD%
PODPWM	i_a	**100**	**0.20**	**0.38**	**0.03**	**0.48**	**0.05**	**0.21**	**0.80**
DMVPWM	i_a	**100**	**0.27**	**0.46**	**0.09**	**1.97**	**0.09**	**1.01**	**2.57**

2) Scenario 2: In this scenario, the capability of the DMVPWM proposed method for NPV balancing is investigated; moreover, the experimental results of the DMVPWM and DPWM methods are compared. The unbalanced NPV is generated in experiments by connecting a 5k Ω resistor across the upper or lower capacitors. If the 5k Ω resistor connects in parallel to the upper capacitor, the NPV is increased. Conversely, the parallel connection of the 5k Ω resistor and lower capacitor cause the NPV to decrease.

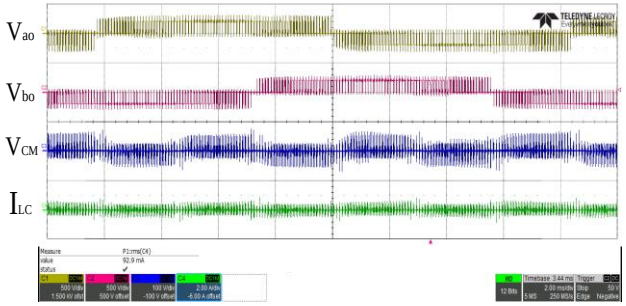


Fig. 20. The phase voltage, CMV, and LC for normal operating mode of the proposed method

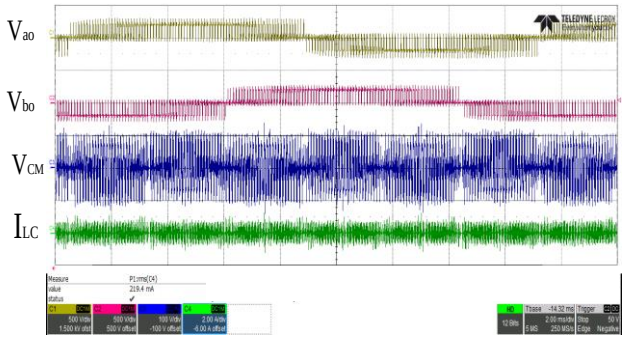


Fig. 21. The phase voltage, CMV, and LC for the PODPWM method

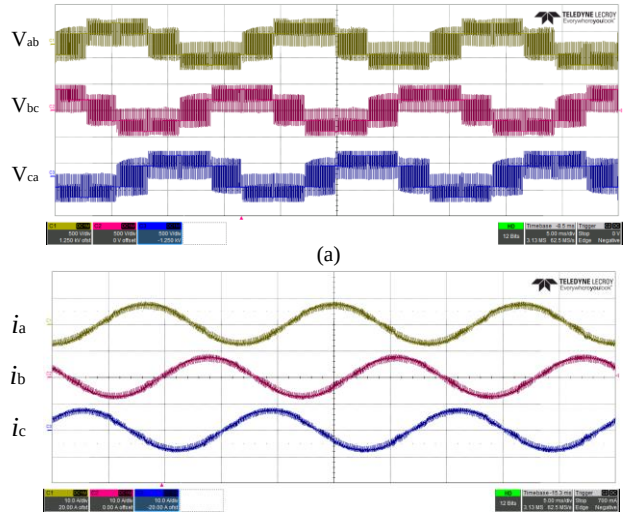


Fig. 22. The output voltage and current for normal operating mode of the proposed method. (a) Line voltages. (b) Line currents.

When V_{up} is greater than V_{dn} , the proposed method switches on the P-DMVPWM ancillary operating mode to accomplish balancing control. The P-DMVPWM ancillary operating mode applies the low-amplitude CMV switching patterns of the DPWMMAX method to increase the NPV. The voltage of the DC-link capacitors and CMV during NPV balancing for P-DMVPWM and DPWMMAX are shown in Fig.23 and Fig.24 respectively.

The phase voltage and LC for the P-DMVPWM mode of the proposed method and DPWMMAX method are shown in Fig.25 and Fig.26 respectively. Remarkably, the peak and RMS values of the LC reached 1.353A and 179.3mA for the DPWMMAX method. The peak and RMS values of the LC decreased to 1.054A and 155.4mA by implementing the P-DMVPWM respectively.

When V_{up} is less than V_{dn} , the proposed method switches on the N-DMVPWM ancillary operating mode to achieve balancing control. The N-DMVPWM ancillary operating mode decreases the NPV by applying the low-amplitude CMV switching patterns of the DPWMMIN method. Fig.27 and Fig.28 show the NPV balancing process for the N-DMVPWM and DPWMMIN respectively.

The phase voltage and LC for the N-DMVPWM mode of the proposed method and the DPWMMIN method are shown in Fig.29 and Fig.30 respectively. Remarkably, the peak and RMS values of the LC reached 1.302A and 179.6mA for the DPWMMIN method and they decreased to 1.058A and 155.7mA by implementing the N-DMVPWM respectively.

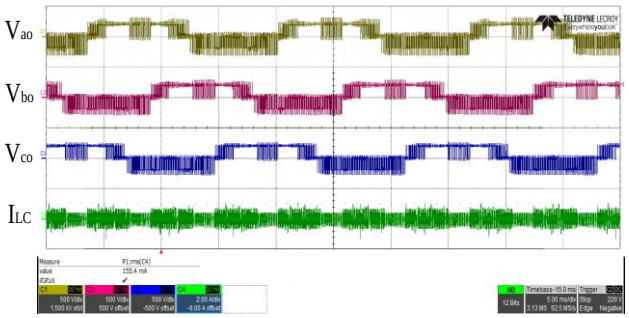


Fig. 25. The Phase voltage and LC for the P-DMVPWM mode of the proposed method.

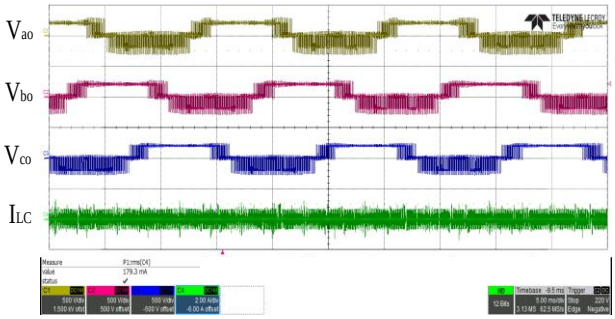


Fig. 26. The phase voltage and LC for the DPWMMAX method.

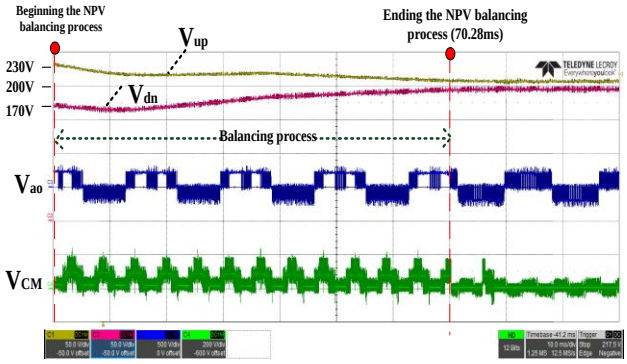


Fig. 23. The NPV balancing process for the P-DMVPWM operating mode of the proposed method.

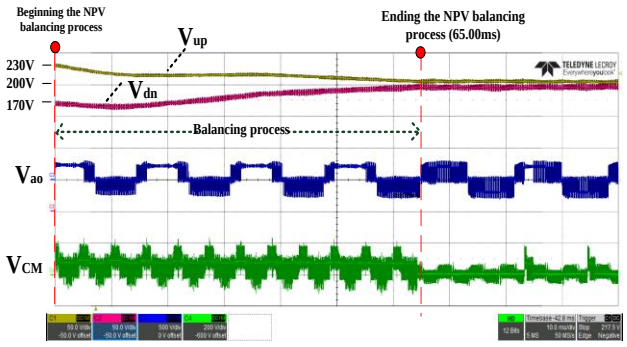


Fig. 24. The NPV balancing process for the DPWMMAN method.

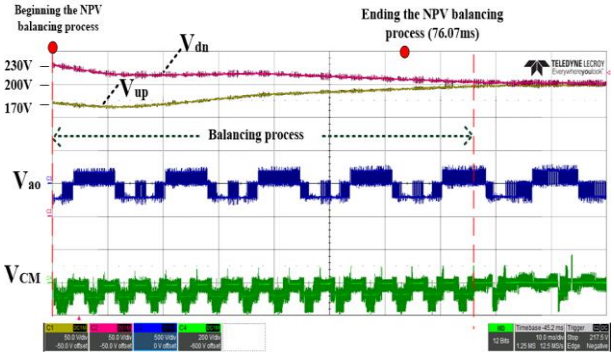


Fig. 27. The NPV balancing process for the N-DMVPWM operating mode of the proposed method.

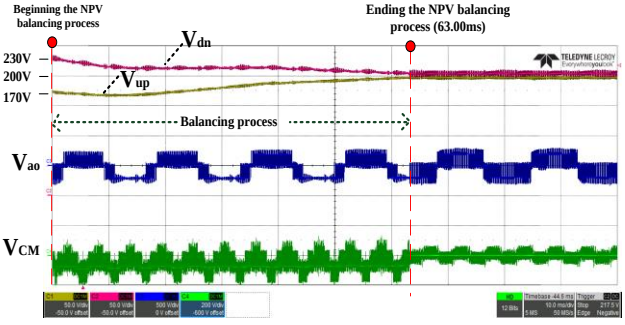


Fig. 28. The NPV balancing process for the DPWMMIN method.

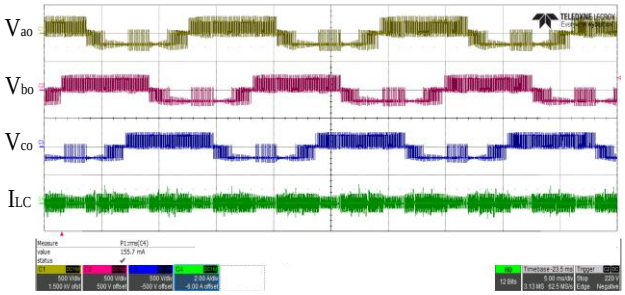


Fig. 29. The Phase voltage and LC for the N-DMVPWM mode of the proposed method.

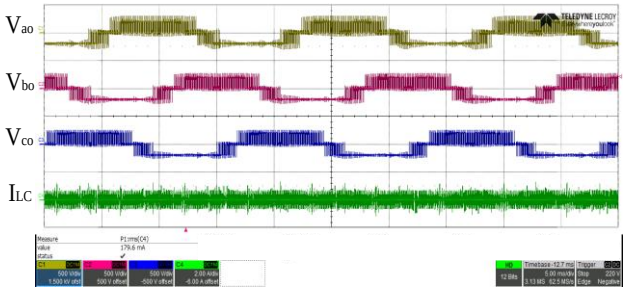


Fig. 30. The phase voltage and LC for the DPWMMIN method.

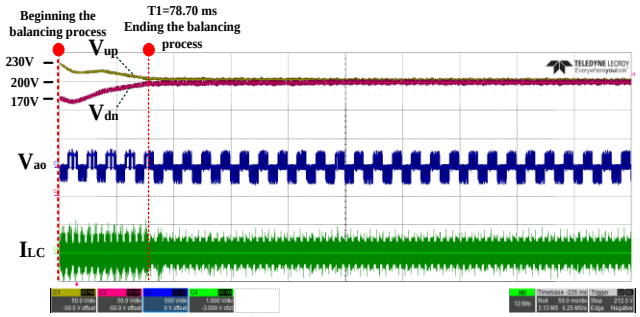
3) Scenario 3: In this scenario, the automatic switch capability of the DMVPWM proposed method between unbalanced and normal operating modes is investigated. Fig.31 shows the voltage of the DC-link capacitors, the phase output voltage V_{ao} and the LC for the normal and unbalanced operating mode of the proposed method. Accordingly, it can be seen that the NPV became balanced at T1 by switching on the P-DMVPWM or N-DMVPWM ancillary mode of the proposed method. The P-DMVPWM and N-DMVPWM ancillary modes balanced the NPV. After accomplishing the NPV balancing process at T1, the DMVPWM method applied the normal operating mode.

D. Analysis of experimental results

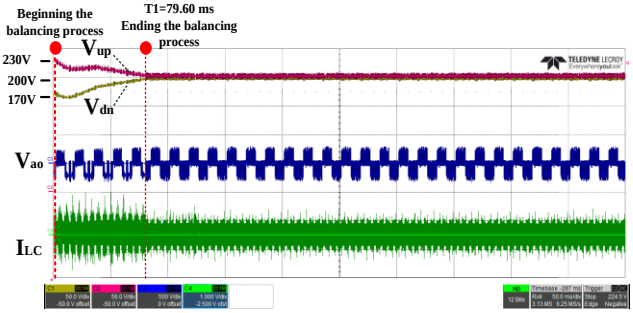
In this section, the experimental results of the previous part scenarios are analyzed.

1) Scenario 1 analysis: The DMVPWM method applies the conventional MVPWM switching patterns to generate command voltage in the normal operating mode. In other words, the DMVPWM method uses the switching state of six medium vectors and one zero vector to generate the command voltage when the NPV is balanced. On the other hand, the PODPWM method generates the output voltage by the switching state of the large, medium, small, and zero vectors. Considering the switching states and switching patterns of the proposed and PODPWM methods, the experimental results can be analyzed as follows.

According to Fig.21, the PODPWM method implementation caused the significant CMV ripple since the switching state of the large, medium, small, and zero vectors cause different amounts of the CMV to exist. Subsequently, the considerable flow of the LC was justified since the higher the amplitude of the CMV ripple is, the greater the leakage current flow.



(a)



(b)

Fig. 31. The automatic switch between unbalanced and normal operating modes of the proposed method. (a) Between the P-DMVPWM and normal modes. (b) Between the N-DMVPWM and normal modes.

According to Fig.20, the proposed method reduced the CMV ripple effectively since the switching state of six medium vectors and zero vector ([OOO]) cause an equal amount of the CMV to exist. However, negligible CMV rises were observed at switching moments. These CMV rises were originated from the undesirable switching states that occurred due to switching dead time. For example, although the next switching state of [NOP] is [ONP] according to the DMVPWM switching sequence, the [OOP] undesirable state was switched during the dead time. The undesirable switching states caused CMV to arise at the switching moments. These CMV rises justified the negligible flow of the LC, which is visible in Fig.20.

Considering Table VIII, it is worth mentioning that the power quality analyzer takes into account up to the 40th order of harmonics to calculate the THD in experiments. On the other hand, the simulation software considers all harmonics for THD calculation. Therefore, the simulation results for THD were greater than the experimental results (refer to Appendix II). However, the calculated THD up to 100th order of harmonics was zero in simulation results (FFT analysis). Accordingly, the following statements can be mentioned considering that the low-order harmonics were zero in simulation results. First, the observed low-order harmonics in experiments mainly refer to circuit imperfection and noise, and the proposed and conventional methods almost do not cause any low-order harmonics. Second, the greater harmonic amount caused in simulation origin from high-order harmonics which can be removed by the low pass output filter easily.

2) Scenario 2 analysis: The NPV of the 3LT^2 inverter is affected by different switching states. The dwell time of small vector switching states is directly proportional to the amount of NPV change. Consequently, the experimental results are analyzed considering the switching states and switching patterns of the proposed and DPWMMAX and DPWMMIN methods.

The proposed method applied the specific switching patterns of the DPWMMAX or DPWMMIN method during the NPV balancing process, in addition to the MVPWM switching patterns. These specific switching patterns, which caused a low-amplitude CMV ripple, assured the existence of the small vector switching states. However, the remaining MVPWM switching patterns shortened the dwell times of the small vector for the proposed method as compared to the DPWMMAX and DPWMMIN methods. Consequently, the NPV balancing process by the proposed method took longer than the DPWMMAX and DPWMMIN methods. The duration of the balancing processes is shown in Fig.23, Fig.24, Fig.27, and Fig.28.

An unexpected voltage drop of capacitors can be seen at beginning of the NPV balancing process (see Fig.23, Fig.24, Fig.27, and Fig.28.). This voltage drop refers to the sudden reduction of energy stored in capacitors because of injecting energy into the AC grid. The sudden reduction of the capacitors' energy is caused due to the faster response of the 3LT^2 inverter than the DC power supply. Indeed, the rectifier inbuilt the DC power supply responds to change of energy slower. As a result, the DC power supply cannot charge the DC-link capacitor energy as fast as it is consumed by the 3LT^2 inverter at the beginning of the NPV balancing experiments.

The line voltage and output currents for the P-DMVPWM ancillary operating mode are shown in Fig.32. In Fig.32(b), the V_{sel} signal waveform highlights the intervals in which the proposed method replaced the switching patterns of the MVPWM with the specific patterns of the DPWMMAX to achieve the P-DMVPWM ancillary mode. It can be seen that an insignificant distortion of output current was observed at the moments of DPWMMAX and MVPWM methods replacement. Fig.33 shows line voltage and output currents for the N-DMVPWM ancillary operating mode. In Fig.33(b), The V_{sel} signal waveform highlights the intervals in which the DPWMMIN method was integrated into the MVPWM to achieve the N-DMVPWM ancillary mode. The DPWMMIN and MVPWM integration caused an insignificant distortion of output current.

The P-DMVPWM and N-DMVPWM ancillary modes of the proposed method are only applied for NPV balancing during a transient period. Therefore, generated harmonic distortion by these ancillary modes is ignorable for THD calculation of the proposed method. Nevertheless, the THD of output current (i_a) generated by the switching patterns of these ancillary modes are interesting to evaluate since they cause the positive and negative half-cycles of the phase voltages to asymmetrical. Moreover, the THD evaluation result for ancillary modes can be compared with the THD amounts generated by DPWMMAX and DPWMMIN switching patterns to investigate the integration effect of DPWM and MVPWM on THD of output current.

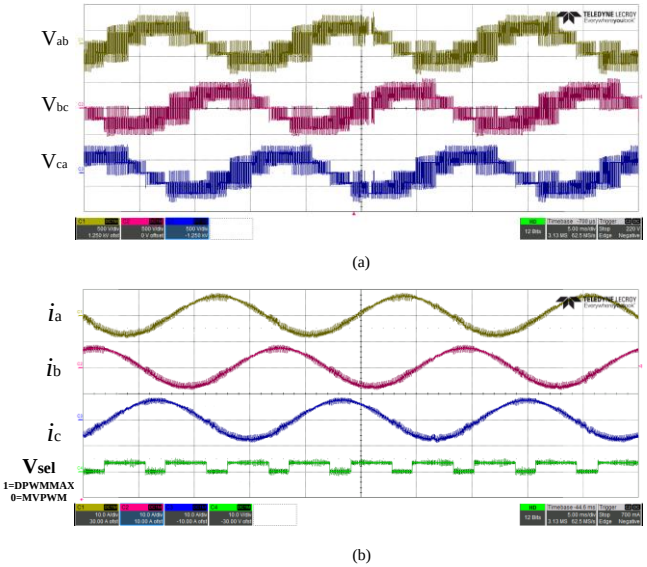


Fig. 32. The output voltage and current for P-DMVPWM operating mode of the proposed method. (a) Line voltages. (b) Line currents.

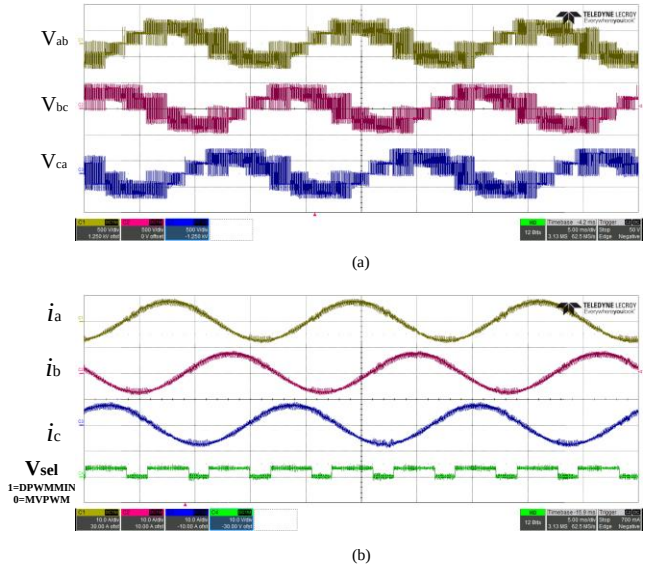


Fig. 33. The output voltage and current for N-DMVPWM operating mode of the proposed method. (a) Line voltages. (b) Line currents.

The THD amount for switching patterns of DPWMMAX and DPWMMIN is 1.6% (if they implemented in balanced NPV condition). The THD increase to 3.1% for the P-DMVPWM and N-DMVPWM ancillary modes since the switching patterns of ancillary modes are a combination of two MVPWM and DPWM different methods. Besides, it can be noted that although the phase voltage generated by DPWMMAX and DPWMMIN methods and also ancillary modes of the proposed method are asymmetrical (see Fig.23 to Fig.26) they don't cause intolerable THD for output current during the transient period. Accordingly, it can be mention that the higher harmonic distortion during the balancing process is mainly caused by the

unbalanced NPV not the switching patterns of the proposed or conventional methods.

Note, that although the experiments have been accomplished on a $3LT^2$ inverter with 2KW output power the $3LT^2$ inverter is a well-accepted power conversion for the application of tens of KW. Generally, the following improvements are achieved in experimental results if the output power of the $3LT^2$ inverter is increased to reach the accepted range. First, the increase of output power causes the fundamental component amplitude of output current to increase. Accordingly, the increase of output power effectively decreases the THD since the THD is inversely proportional to the fundamental component of output current. As result, the power quality of out is improved and the output filter can be selected smaller. Second, the increase of output power causes the three-phase current magnitude to increase. The larger the three-phase current and subsequently the neutral point current is the DC-link capacitor's charge or discharge is faster. Consequently, the dynamic response of the NPV balancing process is improved.

E. Discussion

In this paper, it is supposed that the $3LT^2$ inverter is practically operated based on the normal mode of the proposed method since the NPV is ordinarily situated in a balanced state. Moreover, if the NPV becomes unbalanced inadvertently, the proposed method is able to balance the NPV during a transient period. Accordingly, this part presents a discussion of the proposed method performance in terms of the LC reduction, NPV balancing control, and THD of output. Table IX presented a summary of the experimental results for proposed and conventional methods. Moreover, it can simplify the understanding of the comparative results, which are reported in the discussion.

1) LC reduction: The experimental results indicate that the proposed method effectively maintains the LC elimination advantage of the MVPWM method. According to Table IX, the normal operating mode of the proposed method, which is active ordinarily and operates as same as the conventional MVPWM method, respectively reduced the peak and RMS values of the LC by 27.2% and 57.66% as compared to the conventional PODPWM method.

2) NPV balancing: The experiential results demonstrate that the proposed method not only effectively accomplished the NPV balancing control but also reduced the LC during the balancing process. The unbalanced operating mode of the proposed method, which only switches on for transient periods in case of NPV unbalancing, respectively suppressed the peak and RMS values of the LC by almost 22.1% and 13.33% as compared to the DPWM conventional methods.

3) THD of output: The THD value of output current should be investigated for the normal operating mode of the proposed method since the inverter is operated based on ordinarily. The normal operating mode causes the THD to equal 2.57%. Consequently, the proposed method is qualified to interconnect the PV system with the AC grid according to the IEEE 1547 standard [51].

VI. CONCLUSION

In this paper, a hybrid modulation method is introduced by synergizing the strengths of the conventional MVPWM and DPWM methods. The MVPWM benefits the LC elimination; however, it suffers from the deficiency of NPV balancing capability. Accordingly, the DPWM and MVPWM methods are specifically integrated to overcome the MVPWM method drawback. In this regard, the certain switching patterns of MVPWM replaces with the low-amplitude CMV ripple patterns of the DPWM method to accomplish balancing control in case of NPV unbalancing. The experimental tests have been accomplished and compared for proposed and conventional methods. The comparison of results demonstrates that the proposed method effectively maintained the LC elimination advantage of the MVPWM method. Moreover, it indicates that the proposed method respectively reduced the RMS and peak values of the LC during the NPV balancing process by almost 22.1% and 13.33% as compared to the DPWM conventional method.

TABLE IX
THE SUMMARY OF THE EXPERIMENTAL RESULTS FOR PROPOSED AND CONVENTIONAL METHODS

Method	Operating mode		LC peak value	LC RMS value	Maximum amplitude of CMV	Maximum amplitude of CMV ripple	Capability of	
							NPV balancing	LC elimination
DMVPWM (Proposed method)	Normal		0.902A	92.9mA	0	0	YES	YES
	Unbalanced	P-DMVPWM	1.054A	155.4mA	$\frac{1}{3}v_{dc}$	$\frac{1}{6}v_{dc}$		
		N-DMVPWM	1.058 A	155.7mA	$\frac{1}{3}v_{dc}$	$\frac{1}{6}v_{dc}$		
MVPWM	No options available		0.902A	92.9mA	0	0	NO	YES
PODWM	No options available		1.239A	219.4mA	$\frac{1}{6}v_{dc}$	$\frac{1}{3}v_{dc}$	NO	NO
DPWM	DPWMMAX		1.353A	179.3mA	$\frac{1}{3}v_{dc}$	$\frac{1}{3}v_{dc}$	YES	NO
	DPWMMIN		1.302 A	179.6mA	$\frac{1}{3}v_{dc}$	$\frac{1}{3}v_{dc}$		

APPENDIX I

DC-link capacitor selection: The worst-case ripple current of the capacitors is firstly calculated considering the phase current, modulation index, and power factor [56].

$$I_{c,RMS} = \sqrt{\left(\left(\frac{3{I_N}^2 m_a}{4\pi}\right) * \left(\sqrt{3} + \left(\cos 2\varphi * \frac{2}{\sqrt{3}}\right)\right)\right) - \left(\frac{9}{16} * (I_N * m_a)^2 * (\cos\varphi)^2\right)}$$

Where m_a is the modulation index, I_N is the output phase current and φ is the phase difference between phase voltage and current. Afterward, a capacitor that simultaneously provides a ripple current rating higher than the worst-case and the DC voltage rating higher than maximum DC-link voltage is selected. Finally, the simulation is run to ensure that the selected capacitor satisfy the voltage ripple requirement of DC-link capacitors (to ensure that the DC-link is enough stiff).

APPENDIX II

Graph of THD versus modulation index: The phase voltage THD variation for the linear range of modulation index has been plotted while the switching frequency is constant and equal to 10 kHz. The THD of phase current depends on voltage THD and inductance of the load. Since the simulation has been run for PF=1, the amount of THD variation with change in MI is as same as that of the phase voltage THD. The simulation software used the following equation to calculate the THD amount.

$$THD(\%) = \frac{\sqrt{{v_{Rms}}^2 - {v_{1,Rms}}^2}}{V_{1,RMS}} * 100$$

Where the v_{Rms} is the amplitude of the phase voltage RMS value and $V_{1,RMS}$ is the amplitude of the fundamental component of phase voltage (RMS volts).

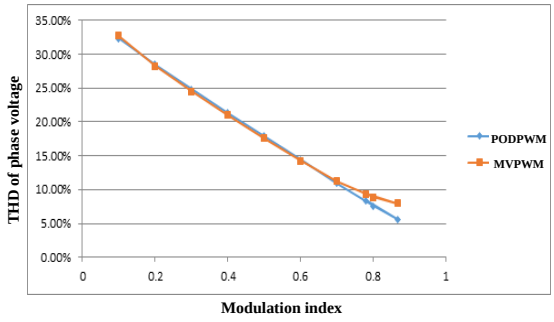


Fig. 34. THD versus modulation index for the proposed and conventional methods

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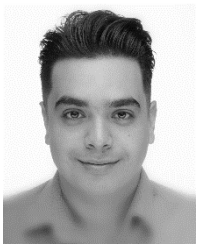

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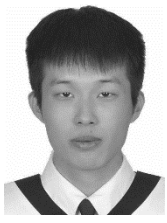

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