A Fully Differential Low-Power Divide-by-8 Injection-Locked Frequency Divider Up to 18 GHz

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***Abstract*—A low power divide-by-8 injection-locked frequency divider is presented. The frequency divider consists of four current-mode logic (CML) D-latches connected in the form of a four-stage ring with the differential input signal injected into the clock terminals of the latches. The output signals can be taken from the data terminals of any of the four latches. The proposed frequency divider has higher operating frequency and lower power dissipation compared with conventional static frequency dividers. Compared with existing injection-locked frequency dividers, the proposed fully differential frequency divider presents wider locking range with the center frequency independent of injection amplitude. The frequency divider is implemented in TSMC 0.18 μm CMOS technology. It consumes around 3.6 mW power with 1.8 V supply. The operating frequency can be tuned from 4 GHz to 18 GHz. The ratio of the locking range over the center frequency is up to 50% depending on the operating frequency and biasing conditions.**

***Index Terms*—Divide by eight, injection-locked frequency divider, low-power frequency divider.**

I. Introduction

PHASE-LOCKED loops (PLLs) are widely used in modern communication systems. With ever-increasing demand for larger bandwidth, the required operation frequency of the PLLs keeps getting higher. On the other hand, more and more communication chipsets are used in mobile devices, which require PLLs with low power dissipation to achieve longer battery life. In PLLs, most of the power is consumed by the VCO and the frequency dividers which operate at a much higher frequency compared with other components within the loop. It remains a challenging task to design high frequency dividers with low power dissipation.

Current-mode logic (CML) static frequency dividers are widely used in high-speed PLLs due to simple design and robust operation. However, they consume significant amount of power with high incoming frequencies. Injection-locked frequency dividers (ILFD) are gaining popularity in recent years because they can dissipate less power for the same operating frequency. Unlike static frequency dividers which can operate with incoming frequencies approaching DC, ILFD performs frequency division correctly only when the incoming frequency stays within a range, denoted as the locking range. Various ILFD structures have been reported in existing literatures [1]–[3]. However, the existing solutions suffer from various problems, e.g., the locking range is too narrow and it shifts with the input signal amplitude. Also, the existing structures use either single-ended input or pseudo-differential input, which limits their application in high-performance low-noise systems that requires fully differential signals throughout the entire system.

To address these issues, a fully differential ILFD structure with low power dissipation is proposed in this work. The ILFD structure implements a division ratio of eight to produce 8-phase output signals that are 45 degrees apart from each other. Furthermore, the proposed topology can be easily modified to implement other even division ratios. Section II gives a brief introduction of the existing solutions of ILFD structures and compares their advantages and drawbacks. Section III presents the proposed ILFD structure, explains the locking mechanism and performs characterization of the locking range, sensitivity and phase error. Section IV analyzes the measurement results. Section V draws conclusions from this paper.

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II. Conventional Frequency Dividers

A. CML Static Frequency Divider

CML static frequency dividers are widely used in multi-gigahertz PLLs to divide the high frequency signal from the VCO into a signal with frequency lower enough to be handled by the following programmable frequency dividers implemented in CMOS logic. The basic CML static frequency divider is a divide-by-2 cell which consists of a CML D-flip-flop (DFF) with the Q terminals connected back to the D terminals in reversed polarity. The term "static" refers to the storage cells (latches) which can store logic states for infinite time. It is used to differentiate from dynamic frequency dividers where logic states are stored on parasitic capacitance for just a short while. The RUN cells can be cascaded to implement higher division ratios. A divide-by-8 CML static frequency divider is shown in Fig. 1. The first DFF in the divider chain toggles at half the input frequency; the second one toggles at a quarter of the input frequency; the third one toggles at one-eighth of the input frequency. Thus, the maximum input frequency of the entire frequency divider is limited by the maximum toggling frequency of the first DFF in the chain. Assuming that the maximum toggling frequency of a CML DFF in a given process is $f_{t-\max}$, the maximum input frequency of a CML static frequency divider will be around $2f_{t-\max}$. There is no lower limit to the input frequency for CML static frequency dividers. High-speed CML static frequency dividers are usually power hungry because the DFFs of the first stages have to handle very high frequencies.

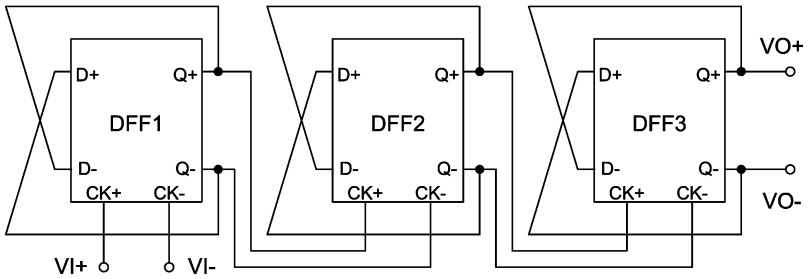

Fig. 1. Conventional divide-by-8 CML static frequency divider.

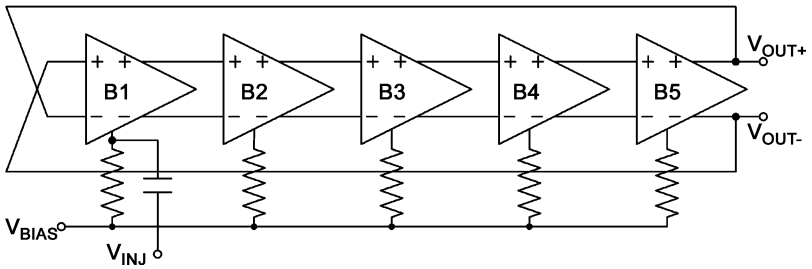

Fig. 2. Ring-oscillator-based ILFD proposed in [1].

B. Injection-Locked Frequency Divider

An injection-locked frequency divider (ILFD) usually consists of an oscillator with one or more terminals for signal injection. If no input signal is injected (i.e., with only DC input bias applied), the oscillator operates at its free-running frequency. When the input signal is injected, the phase of the output signal is locked to the phase of the input signal while the frequency of the output signal stays at a sub-multiple of the input frequency. An ILFD can lock to the input signal only when the input frequency is within the locking range of the ILFD. Since an ILFD operates at the free-running frequency with DC input, it is not able to achieve lock when the input frequency is close to DC. Thus, the lower limit of the locking range of an ILFD is usually significantly higher than DC.

An ILFD based on a five-stage *RC*-type ring oscillator was proposed in [1] and its schematic is shown in Fig. 2. The input signal $V_{\rm inj}$ is injected into the bias terminal of the differential pair of the first stage via AC coupling. The ILFD implements a division ratio of 8. It has a locking range of 25 MHz with 1 GHz input frequency when the injected power is equal to 0 dBm. However, the locking range of this ILFD is too small to be used in most practical applications.

A single-ended divide-by-2 ILFD was proposed in [2]. The schematic of the ILFD is shown in Fig. 3. It is based on a three-stage ring of nMOS inverters with pMOS active load. The input signal is injected into the gate terminal of a nMOS switch (M7) sitting across the output nodes of the second and third stage. When the switch is turned on, the output nodes of the second and third stages are shorted and $V_{\rm out+}$ and $V_{\rm out-}$ are forced to be equal. If $V_{\rm out+} - V_{\rm out-}$ is defined as the differential output voltage, the positive peaks of the input signal will be locked to the zero-crossing points of the differential output voltage in locked state. When the ILFD is locked, the output frequency is equal to half of the input frequency since there is one

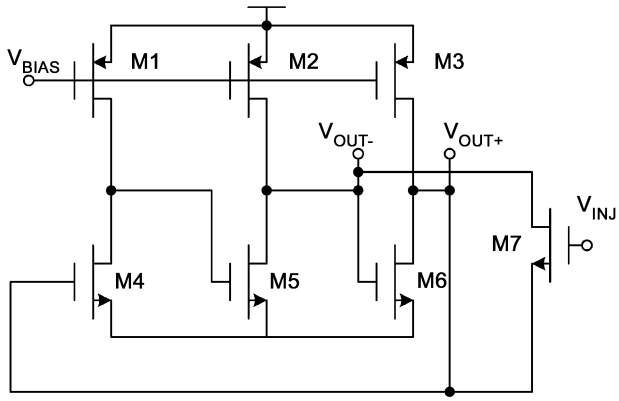

Fig. 3. Single-ended divide-by-2 ILFD proposed in [2].

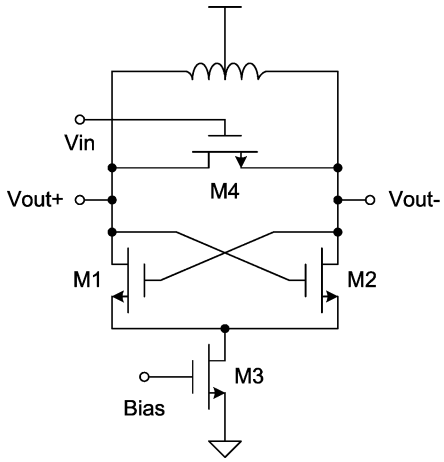

Fig. 4. Divide-by-2 ILFD based on *LC* oscillator proposed in [3].

peak point per input period and two zero-crossing points per output signal. This ILFD consumes 43 μW and has a locking range from 2.1 G to 4.3 G with 0.7 V supply. However, the

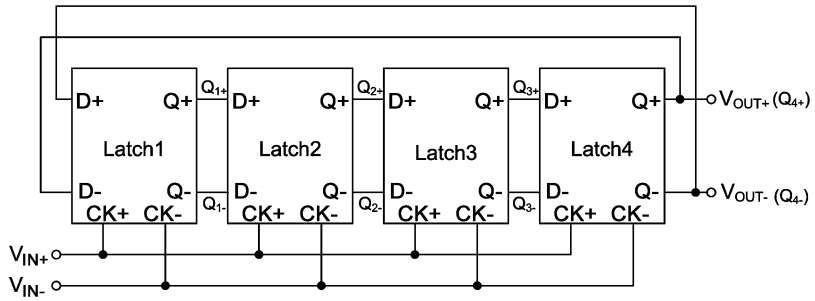

Fig. 5. Schematic of the proposed divide-by-8 LILFD.

two output signals provided by this ILFD are actually far from real differential signals as verified by simulation results, which makes it unsuitable for applications requiring true fully differential outputs. Also, this ILFD is sensitive to power supply variations and common-mode noise interferences since it is based on single-ended nMOS inverters.

A divide-by-2 ILFD based on an *LC* oscillator was proposed in [3]. The schematic of the ILFD is shown in Fig. 4. The locking mechanism is similar to the ILFD based on an inverter chain proposed in [2]. The input signal is injected via the gate terminal of the nMOS switch M3. When the nMOS switch is turned on, the two output terminals are shorted. Therefore, the positive peaks of the input signal are locked to the zero-crossing points of the differential output signal when the ILFD achieves lock. Similar to the ILFD based on an inverter chain, this ILFD also implements a division ratio of two. Due to the high quality-factor of *LC* oscillator, this locking range of this ILFD is relatively narrow (3% around 50 GHz and 19% around 15 GHz).

III. Proposed Divide-by-8 ILFD

A. Structure of the Proposed ILFD

To overcome the issues associated with the existing ILFD solutions, a fully differential divide-by-8 ILFD based on latches (LILFD) is proposed. The schematic is shown in Fig. 5. It consists of a four-stage ring of latches. The output of the last latch is connected to the input of the first latch with inverted polarity to achieve extra phase-shift of 180°. The clock terminals of the four latches are tied together and used to inject the differential input signal. The output frequency is equal to one-eighth of the input frequency. The output signal can be taken from the Q terminals of any of the four latches. The schematic of the latch is shown in Fig. 6. It is a CML latch with pMOS active load biased by VBP. VBP is used to tune the operating frequency of the LILFD.

The locking mechanism of the LILFD can be explained qualitatively as follows. It is assumed that the injected signal is large enough so that the latches stay hard-switched. When the injected signal ($V_{\rm in}$) is low, the latches preserve the current logic state. When the injected signal is high, the latches work like a differential amplifier; the ILFD operates like a ring oscillator and the oscillation signal (Q) propagates from one stage to the next like a pipeline. If we assume that the oscillation signal propagates

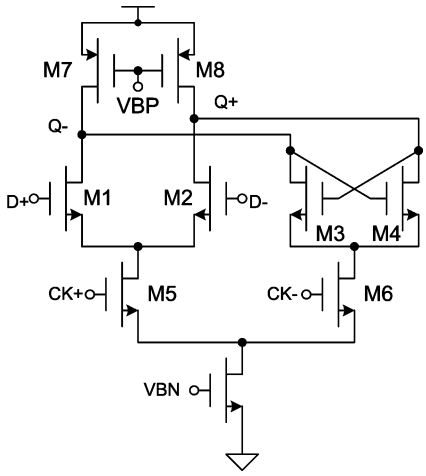

Fig. 6. D-Latch cell used in each stage of the LILFD.

by only one stage during the half period when $V_{\rm in}$ is high, it propagates by only one stage during one full input period since the logic states are preserved during the half period when $V_{\rm in}$ is low. For a four-stage ring oscillator, the phase shift provided by each stage is 45° if all the stages are symmetrical. Thus, one full input period (360°) is equal to 45° phase shift of the oscillation signal in terms of time length. That means the input and oscillation signal (output) have a frequency ratio of 8:1. Because the latches toggle only after $V_{\rm in}$ becomes high, the transition edges of the output signal are locked to the rising edges of the input signal with a certain amount of delay. An illustrative timing diagram of the input and output waveforms is shown in Fig. 7. The transition edges of Q1–Q4 are delayed by t_{ck-q} from the rising edge of $V_{\rm in}$. t_{ck-q} is the time for the latch to toggle state after $V_{\rm in}$ becomes high; $T_{\rm in}$ is the period of the input signal.

When the input frequency becomes low enough so that the oscillation signal is able to propagate by more than one stage during the half period when $V_{\rm in}$ is high, the LILFD is no longer able to lock at a frequency ratio of 8 to 1. The timing diagram illustrating the lower limit of the locking range is shown in Fig. 8(a). t_{q1-q2} is defined as the time it takes for the signal transition to propagate from one stage to the next when $V_{\rm in}$ is high. At the lower limit, the output of the next stage ($\rm Q_2$) just fails to cross zero level before the falling edge of $V_{\rm in}$. After $V_{\rm in}$ becomes low, $\rm Q_2$ reverts to the original level due to the positive

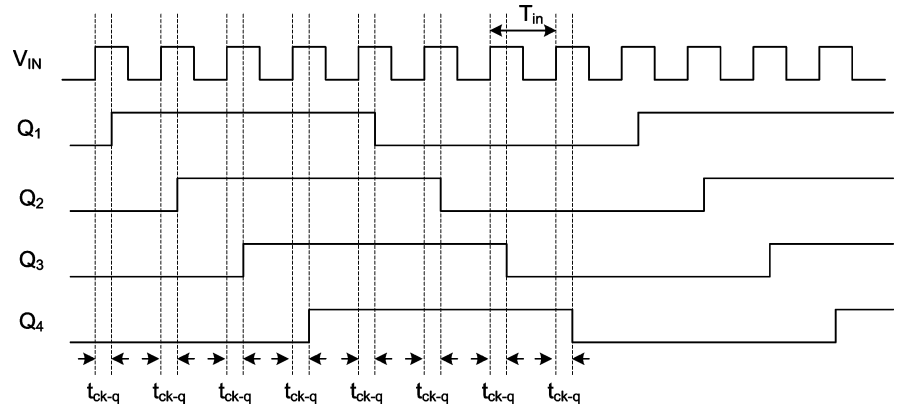

Fig. 7. Timing diagram of the input and output signals of the LILFD.

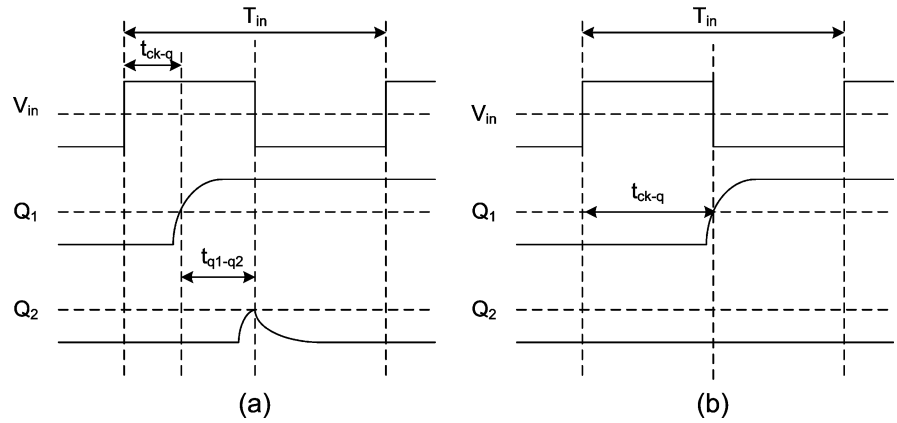

Fig. 8. Timing diagrams at the boundaries of the locking range. (a) Lower limit of the locking range. (b) Higher limit of the locking range.

feedback of the latch. Thus, the condition to reach the lower limit of the locking range can be expressed as

$$\frac{T_{\rm in}}{2} < t_{ck-q} + t_{q1-q2}. \tag{1}$$

On the other hand, when the input frequency becomes very high, the oscillation signal does not have enough time to propagate by one stage during the half period when $V_{\rm in}$ is high. Thus, the LILFD is not able to achieve lock. The timing diagram illustrating the higher limit of the locking range is shown in Fig. 8(b). Q_1 crosses zero just before the falling edge of $V_{\rm in}$. Thus, the upper limit of the locking range can be expressed as

$$\frac{T_{\rm in}}{2} > t_{ck-q}. \tag{2}$$

Combining (1) and (2), a rough approximation for the locking range is obtained as

$$\frac{1}{2t_{ck-q}} > f_{\rm in} > \frac{1}{2(t_{ck-q} + t_{q1-q2})} \tag{3}$$

where $f_{\rm in}(= 1/T_{\rm in})$ is the frequency of the input signal. As a rough approximation, both t_{ck-q} and t_{q1-q2} are proportional to the *RC* time constant at the output node of the latch in tracking mode. More accurate values of these two delays values have to be determined from simulations due to strong nonlinearities of the circuit. The nonlinearities mainly come from the positive-feedback transistors in the latch. The input differential pair of the latch also introduces strong nonlinearity when the oscillation amplitude is large. When the operating frequency goes very high, the latch does no have enough time to fully switch like a digital cell due to the parasitic capacitance. In that case, the actual locking range may be significantly smaller than what is predicated by (3).

It is worthy of pointing out that the LILFD is able to lock at division ratios other than eight (e.g., 4, 7, 16). However, the locking ranges associated with other ratios are much smaller as verified by simulations and thus not discussed here in detail. The actual division ratio at which the LILFD operates is determined by the input frequency. It does not depend on the initial states of the latches, as verified by numerous simulations. Only when the input frequency is not inside any locking ranges for all the possible ratios, the LILFD stays unlocked. When the LILFD is not locked, the output signal contains two frequency components competing with each other, i.e., the input frequency component and the self-oscillating frequency component.

Since the LILFD is based on an *RC* ring oscillator, its locking range is expected to be much larger than the ILFD based on an *LC* oscillator proposed in [3] due to lower quality factor (Q). When the quality factor is very high, it is hard for the ILFD to oscillate at frequencies far from the free-running frequency determined by the *LC* resonator. On the other hand, the input

signal is injected into all the four stages instead of only one stage like the ILFD proposed in [1]. Therefore, the LILFD is expected to have a much larger locking range than the ILFD proposed in [1] because of larger injection efficiency. Furthermore, the LILFD has full differential input signals and output signals, which makes it especially suitable for low-noise high-performance applications. In addition, the LILFD is able to produce evenly-spaced 8-phase output signals, which can be readily used to drive building blocks expecting multiple-phase clocks such as phase interpolators or half-rate phase frequency detectors.

Another important advantage of the LILFD is low power dissipation. All the latches in the four-stage ring only need to toggle at a frequency equal to one-eighth of the input frequency. The transistor size and bias current used in these latches can be much smaller than the latches used in a CML static frequency divider with the same input frequency. Therefore, the LILFD consumes significantly less power compared with static frequency dividers when handling the same incoming frequency. On the other hand, when the same transistor dimension and bias current are used for the latches, the LILFD is able to handle significantly higher input frequency compared with static frequency dividers. As a matter of fact, the LILFD does introduce double input capacitance compared with CML static frequency dividers. When used in a PLL, it increases the load of the VCO and may limit the tuning range of the VCO to some extent.

The LILFD can be easily modified to achieve other frequency division ratios. The four-stage ring can be changed into an n-stage ring and achieves a division ratio of $2n$ under the same locking mechanism. Thus, the LILFD is flexible and suitable to be used in high-speed frequency synthesizers and clock multipliers. In comparison, the ILFDs reported in [2], [3] can only implement a division ratio of 2 and do not have the same flexibility.

B. Locking Range

The locking range of an ILFD is defined as the input frequency range in which the ILFD is able to divide properly the frequency of the incoming signal by the desired ratio. To extract the locking range, the LILFD was simulated by injecting a sinusoidal signal with specified amplitude and frequency. Fig. 9 shows the simulated locking range of the LILFD versus the differential amplitude of the injected signal when VBP is set to 0.3 V (see Fig. 6). As seen from the figure, the locking range increases with the increase of the amplitude of the injected signal. The center frequency of the locking range is almost constant and very close to the free-running frequency of 12.3 GHz. This property makes it much easier to design the LILFD for a particular operating frequency regardless of input signal's amplitude. In comparison, the center frequency of the ILFD reported in [2] is shifted by a large amount with the increase of the input amplitude. For the LILFD, when the amplitude of the injected signal is small, the locking range is almost linearly related to the amplitude of the injected signal. When the amplitude of the injected signal becomes pretty large, the locking range increases more slowly and approaches an upper limit. The underlying reason is that when the amplitude of the injected signal is larger

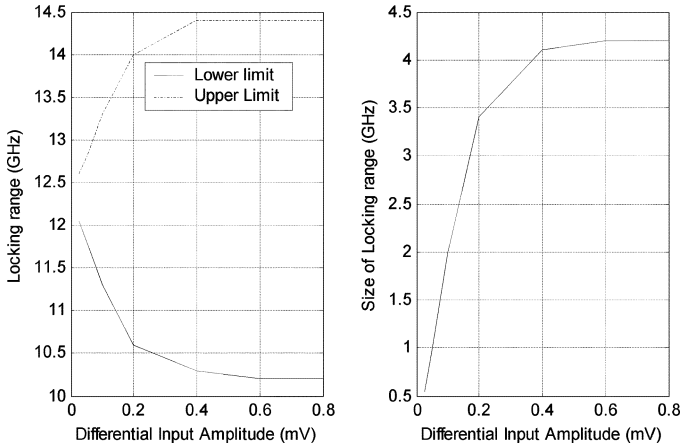

Fig. 9. Simulated locking range versus differential input amplitude when VBP $=$ 0.3 V.

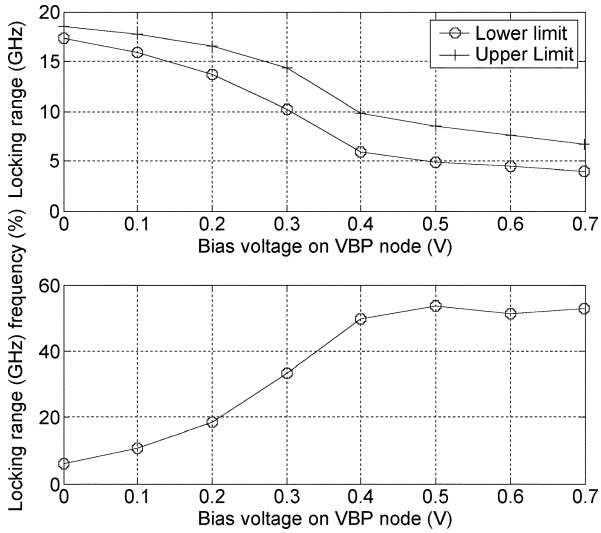

Fig. 10. Locking range of the LILFD under different bias conditions.

than twice the saturation voltage (V_{dsat}) of the differential pair (M5–M6 in Fig. 6), the differential pair is fully switched to one side or the other. Therefore, further increase of the amplitude of the injected signal has little effect on the circuit operation and the locking range reaches a maximum value.

The operating frequency of the LILFD can be tuned by changing the bias voltage VBP. Fig. 10 shows the simulated locking range of the LILFD while VBP is swept from 0 to 0.8 V. Both the lower and upper limit of the locking range decrease with the increase of VBP since the free-running frequency of the LILFD decreases with the increase of the load impedance provided by the pMOS transistors. When VBP is higher than 0.4 V, the ratio of the locking range over the center frequency (LROCF) is relatively constant and stays around 50%, as shown in Fig. 10. When VBP is lower than 0.3 V, the LROCF drops rapidly with the increase of operational frequency.

C. Sensitivity

The sensitivity of an ILFD is defined as the minimum input amplitude that must be applied for the ILFD to lock to the input

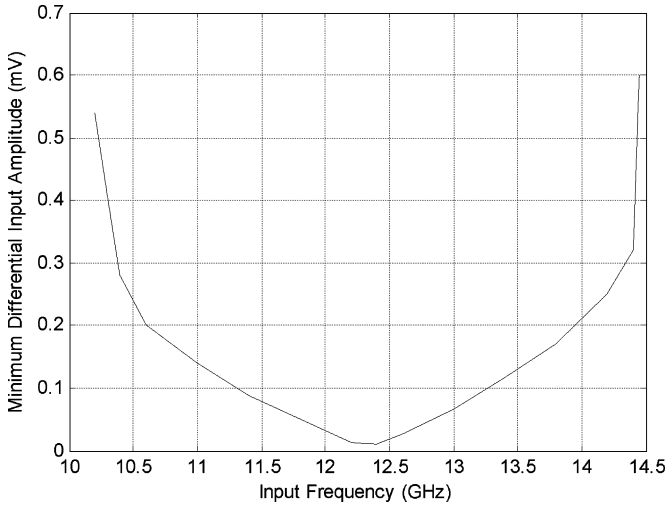

Fig. 11. The input sensitivity of the LILFD versus input frequency when VBP $= 0.3$ V.

signal with a particular frequency. Fig. 11 shows the simulated input sensitivity of the LILFD with the change of the input frequency when VBP is set to 0.3 V. The ILFD achieves minimum input sensitivity when the input frequency is near the free-running frequency, which is equal to 12.3 GHz in this case. If the input frequency is close to the free-running frequency, the sensitivity is almost linearly related to the frequency difference between the input frequency and the free-running frequency. The sensitivity is nearly symmetric on two sides around the free-running frequency; it increases when the input frequency deviates from the free-running frequency until the ILFD loses ability to lock when it goes out of the locking range.

D. Phase Error

When the LILFD is locked, the input signal and output signal can be represented by the following expressions:

$$\begin{cases} V_{\text{in}} = A_{\text{in}} \sin(8\omega t + \varphi) \\ V_{\text{out}} = A_{\text{out}} \sin(\omega t) \end{cases} \tag{4}$$

where φ is the phase error between the input signal and output signal. The phase error in the locked state was extracted from simulations over the entire locking range of the LILFD with VBP $= 0.3$ V. The simulated curve is shown in Fig. 12, where the phase error has been normalized to 2π for simplicity ($\varphi_{\text{norm}} = \varphi/2\pi$). At the lower limit of the locking range, the normalized phase error is about 0.3. That means the transition edge of the output signal is delayed by $0.3T_{\text{in}}$ from the rising edge of the input signal. The normalized phase error increases from 0.3 to 0.5 when the input frequency goes from the lower limit to the higher limit. Thus, the phase error is a monotonic function of the frequency of the injected signal. In this sense, the LILFD closely resembles a type-I PLL in which the steady-state phase error is a function of the input frequency [4].

IV. Measurement Results

The LILFD was manufactured in TSMC 0.18 μm CMOS processing technology through the MOSIS educational program.

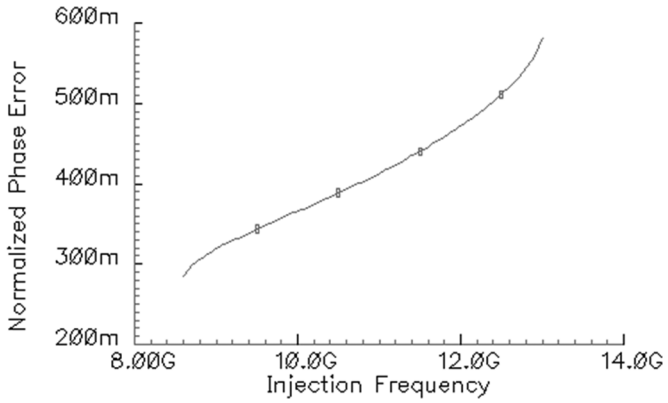

Fig. 12. Normalized phase error versus input frequency for the LILFD.

The test setup to characterize the chip is shown in Fig. 13. A single-ended synthesized sweeper is used to generate the input signal. Unfortunately, it is very difficult to generate fully differential input signals with baluns due to the broadband nature of the system under test. Therefore, a low-pass filter consisting of a large resistor and a large capacitor is placed on-chip between the two injection terminals ($V_{\text{IN}+}$ and $V_{\text{IN}-}$); the input signal is applied to $V_{\text{IN}+}$ while $V_{\text{IN}-}$ only gets the DC level from the input signal due to the low-pass filter. The AC injected signal is generated by the sweeper while the DC input level (about 1.4 V) is provided by a DC power supply via an external high-frequency bias-T component. Fig. 14 shows the measured locking range of the ILFD with large input power (3 dBm) under different biasing conditions. The operating frequency of the ILFD goes from 3 GHz to 18 GHz when the bias voltage VBP is swept from 0 to 0.7. Similarly to the simulation results, the ILFD has larger locking range when VBP is high and the free-running frequency is low. If VBP is higher than 0.4, the locking range is around 50% of the center frequency. If the operating frequency goes above 10 GHz, the LROCF drops rapidly with the decrease of VBP. For VBP $= 0$, the LROCF is about 4%. The measured locking range is a bit smaller than the simulation results at low frequencies while considerably smaller than the simulation results at high frequencies. There are several reasons leading to the reduction of locking range in measurement. Firstly, the test setup uses single-ended injection which is less efficient than fully differential injection. Secondly, the noise on the power supply and the internal phase noise of the LILFD can prevent the LILFD to lock to the input signal properly at critical conditions (i.e., near the boundary of the simulated locking ranges). This is especially significant when the oscillating signal has small amplitude and is very sensitive to noise perturbation at high frequencies. Lastly, high-frequency attenuation and impedance mismatch in the test setup and on the PCB decreases the actual available power injected into the chip at high frequencies.

Fig. 15 shows the measured spectrum of the output signal within 2 MHz frequency offset when the LILFD is locked to 3 dBm input signal at 17.6 GHz. The phase noise plot from 1 kHz to 100 MHz is given in Fig. 16. The measured phase noise at 1 MHz offset from the center frequency of 2.2 GHz is -112.9 dBc/Hz. The measured phase noise is very small because the output phase noise is mainly determined by the input phase noise for an ILFD in locked state [5]. In contrast, when the

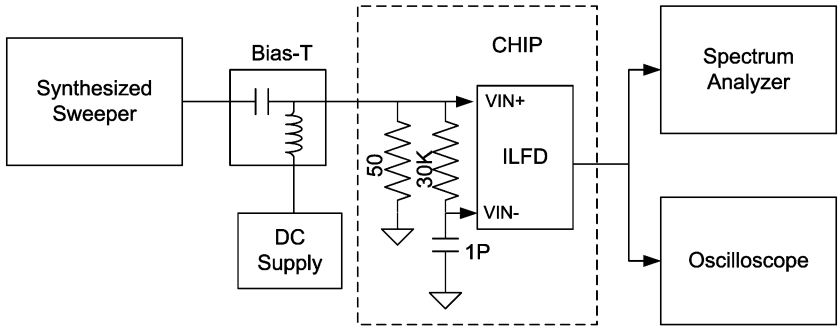

Fig. 13. Test setup of ILFD chip.

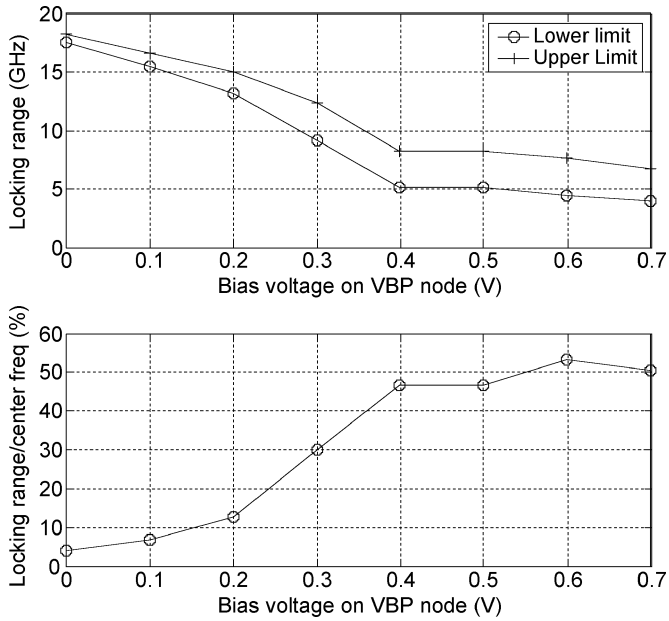

Fig. 14. Measured locking range of the LILFD with 3 dBm input power under different bias conditions.

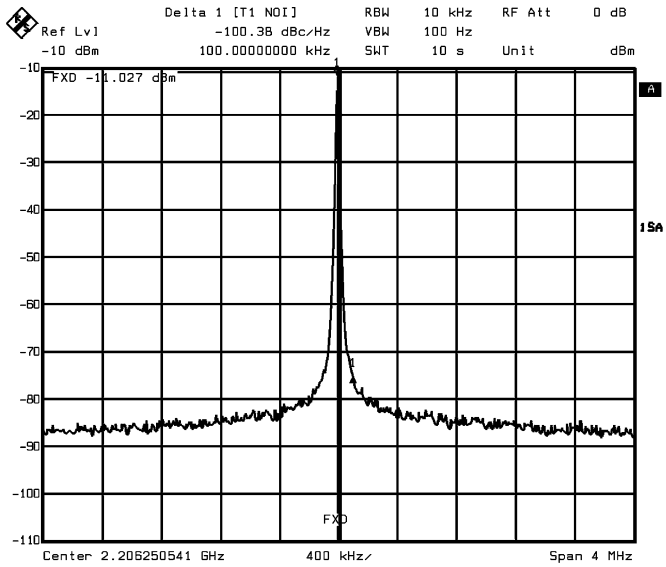

Fig. 15. Output signal spectrum of the LILFD when locked at 17.6 GHz.

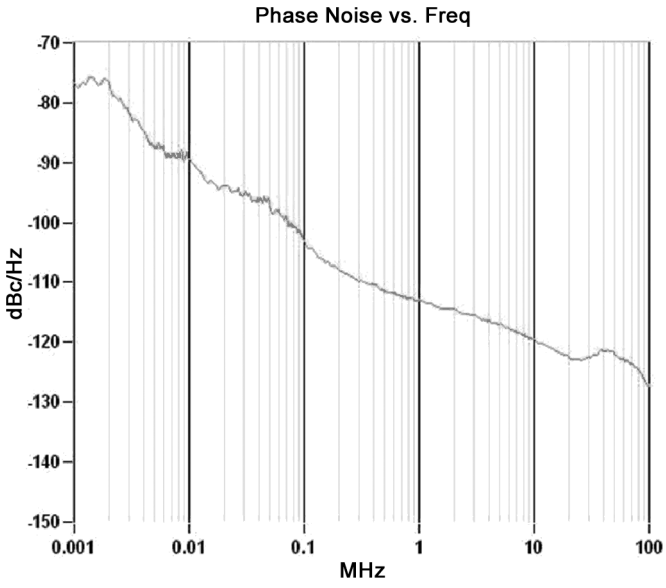

Fig. 16. Measured output phase noise of the LILFD when locked at 17.6 GHz.

input frequency is out of the locking range, the output spectrum looks like the spectrum of a free-running ring oscillator with a wide spread; the center frequency moves back and forth due to the noise and temperature fluctuations.

The locking range of the LILFD was measured under different input power levels with VBP set to 0.3 V. The measured result is shown in Fig. 17. The locking range is proportional to the input amplitude and symmetric around the free-running frequency when the input power is small. However, when the input power gets pretty large, the locking range loses symmetry and the locking range mainly expands on the lower side. That is because single-ended input signal is applied during the measurement. It will not be a problem for the LILFD in practical applications because fully differential signals are readily available from the VCO in most PLLs. The sensitivity of the LILFD was measured over the entire locking range with the same bias voltage on VBP. The measurement result is shown in Fig. 18. Again, due to single-ended input signal injection, the sensitivity is not symmetric around the free-running frequency. The minimum sensitivity of -23 dBm was measured close to the free-running frequency of 11.7 GHz. The measured sensitivity is a bit larger than the simulation results due to the noise and interferences in the testing environment.

The chip consumes 3.6 mW under a supply voltage of 1.8 V excluding the power dissipation of the output buffers. The core of the LILFD circuit occupies an active area of 35 μm $\times$ 35 μm. The microphotograph of the chip is shown in Fig. 19. As a reference, a divide-by-8 CML static frequency divider

TABLE I
PERFORMANCE COMPARISON BETWEEN THE LILFD AND EXISTING SOLUTIONS

	Input	Output	Power (mW)	Supply Voltage (V)	Process (μm)	Division Ratio	Center Freq. (GHz)	LROCF
This work	Fully diff	Fully diff	3.6	1.8	0.18	8	18	4%
							14	13%
							11	30%
							6.5	47%
[1]	Single	Single	0.35	1.5	0.24	8	1	2.5%
[2]	Single	Pseudo-diff.	0.044	0.7	0.2	2	4.3	53%
[3]	Pseudo-diff	Fully diff	3	1.5	0.13	2	50	3%
							40	0.2%
							15	19%
[6]	Pseudo-diff	Fully diff	10.4-12.5	2	0.13	8	20	0.75%
						6	15	5.1%
						4	10	20%
						2	5	40%
[7]	Pseudo-diff	Fully diff	6.8	1.8	0.18	8	14.5	1.4%
						6	10.7	9.3%
						4	6.8	23.5%
						2	3.3	60%
[8]	Fully diff	Fully diff	12	1.8	0.13	2	36	9.5%
CML Static FD (Post-layout simulation)	Fully diff	Fully diff	5.3	1.8	0.18	8	12	N/A

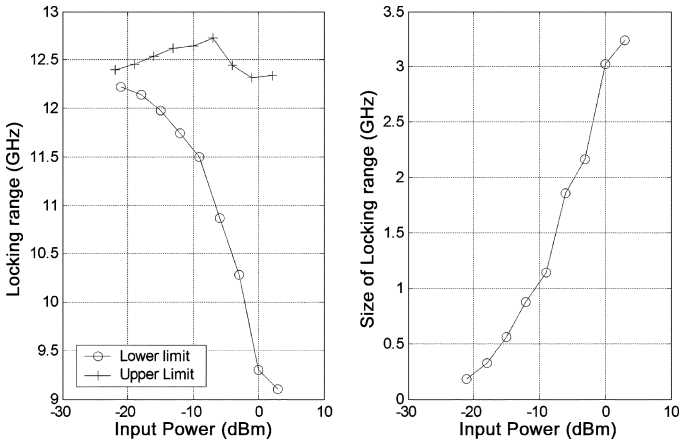

Fig. 17. Measured locking range of the LILFD versus input power when VBP $= 0.3$ V.

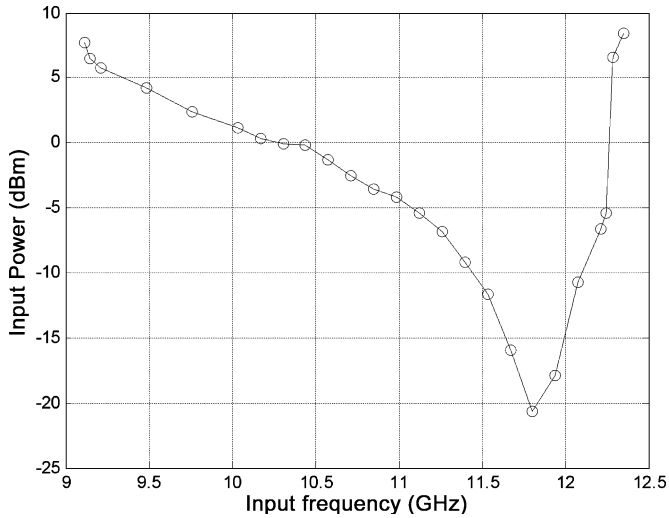

Fig. 18. Measured input sensitivity versus input frequency when VBP $= 0.3$ V.

was also designed and simulated with post-layout parasitics in the same technology. It achieves a maximum input frequency of 12 GHz with a power dissipation of 5.3 mW. Performance comparison between the LILFD and the existing solutions is given in Table I. It shows that the LILFD has significant overall advantage in terms of power dissipation, maximum operating frequency and locking range compared with the existing solutions. Compared with CML static frequency divider, the LILFD has significantly less power dissipation and higher maximum operating frequency. Compared with the topologies reported in [1] and [3], the LILFD has much larger LROCR. The LILFD has significantly larger LROCR and lower power dissipation than the ILFD reported in [6] and [7]. Although the divide-by-2 case of the ILFD reported in [7] has a large LROCR (60%), the operating frequency of 3.3 GHz is very low for the given technology (CMOS 0.18 μm); a simple CMOS frequency divider might as well be used for much lower power dissipation. As a matter of fact, the ILFD reported in [2] has much low power dissipation mainly because it is designed to work at relatively low operating frequencies for the given technology and uses a very low power supply voltage of 0.7 V. However, that topology is quite sensitive to common-mode noise and power supply variation due to the nature of a single-ended design. The LILFD is a design with fully differential input/output and achieves much better rejection to common-mode noise and interferences. The ILFD reported in [8] has fully differential input/output with pretty high operating frequency due to the use of passive inductors. However, it can only divide the input frequency by a fixed ratio of two.

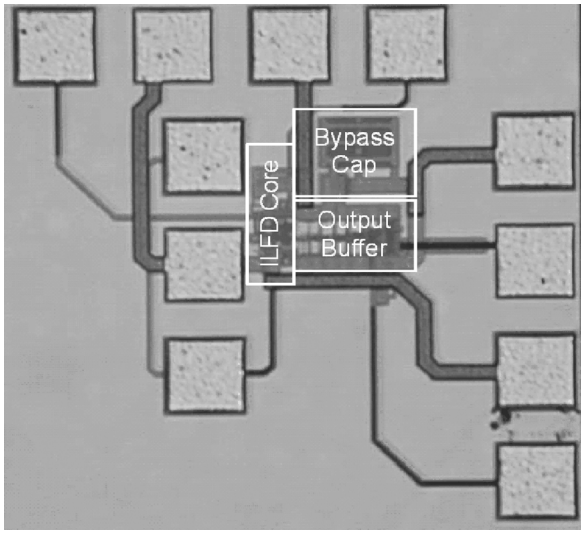

Fig. 19. Die photo of the LILFD prototype chip.

V. Conclusion

A fully differential divide-by-8 ILFD based on latches is described. It operates from 3 GHz to 18 GHz under different biasing conditions. The LROCR of the proposed topology is around 50% when operating at low and moderate frequencies. It has higher operating frequencies and lower power compared with CML static frequency dividers and larger locking range than existing ILFD structures. Its locking range stays symmetric around the free-running frequency under different input power levels, which makes easier to design it to operate in a pre-defined frequency band. The LILFD is the first reported high-division-ratio ILFD with fully differential input and output. The structure can be easily modified to implement other even number division ratios. It can be used as standalone frequency dividers or high-frequency prescalers in PLLs in practical applications.

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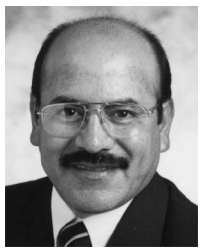

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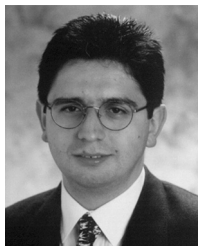

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