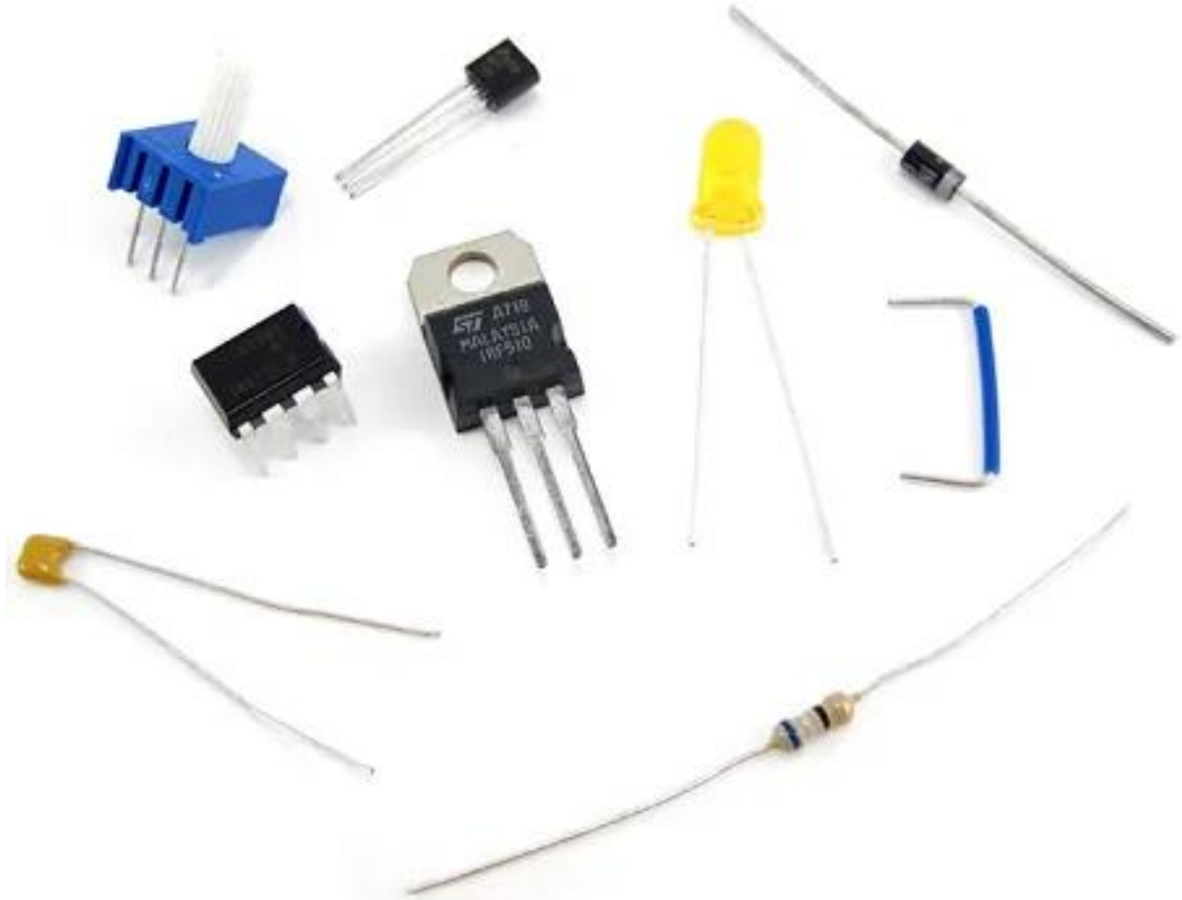
آزمایشگاه مدار منطقی

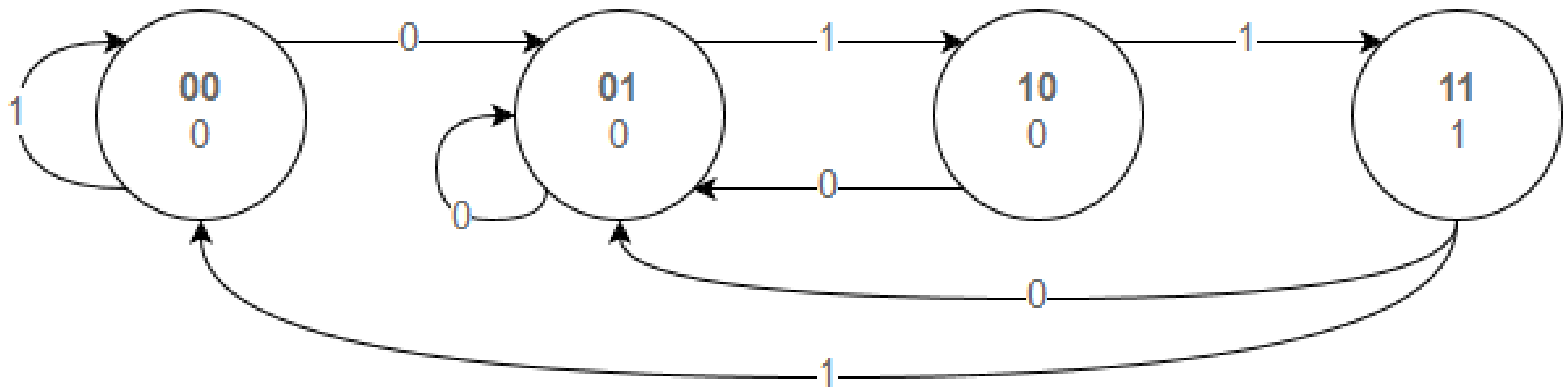
فملا معمارزنجانی



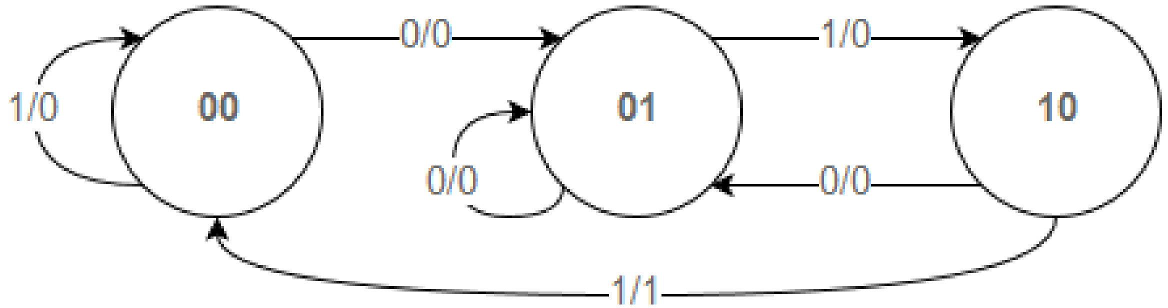
جلسه یازدهم

- طراحی ماشین قهوه ساز
- پروژه پایانی (۵ نمره)
- دیتا شیت آی سی ها

Moore



Mealy



طراحی و پیاده سازی ماشین خودکار تحویل قهوه

دستگاه قهوه ساز مورد آزمایش ما به گونه ای عمل میکند که در صورت گذاشتن ۷۵ سنت در داخل دستگاه، دستگاه یک لیوان قهوه را تحویل مشتری میدهد. دستگاه فقط دارای یک شیار برای گذاشتن سکه است و تنهای سکه های ۲۵ سنتی را نیز می پذیرد. یک سنسور در بالای شیار سکه است که هرگاه سکه ۲۵ سنتی در آنجا قرار گرفت یک سیگنال ۱ برای کنترلر دیجیتال می فرستد. اگر مجموع سکه ها به سه تا سکه یعنی ۷۵ سنت رسید، دستگاه آماده پرداخت لیوان قهوه است. حال با توجه به توصیف مسئله،

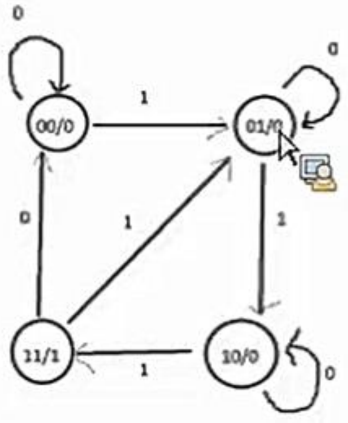
مدل Moore ماشین مذکور را طراحی نمائید

مدل Mealy ماشین مذکور را طراحی نمائید

به کمک فلیپ فلاپهای D و مدل Moore به طراحی شماتیک کنترلر بپردازید

طراحی شماتیک مرحله سوم را با کمک آی سی های TTL بر روی بورد ببندید و آن را تست کنید. برای سنسور می توانید از یک button-push استفاده کنید که هرگاه فشار داده شد به منزله قرار گرفتن یک سکه۲۵ سنتی است

به کمک فلیپ فلاپهای JK و مدل Mealy به طراحی شماتیک کنترلر بپردازید

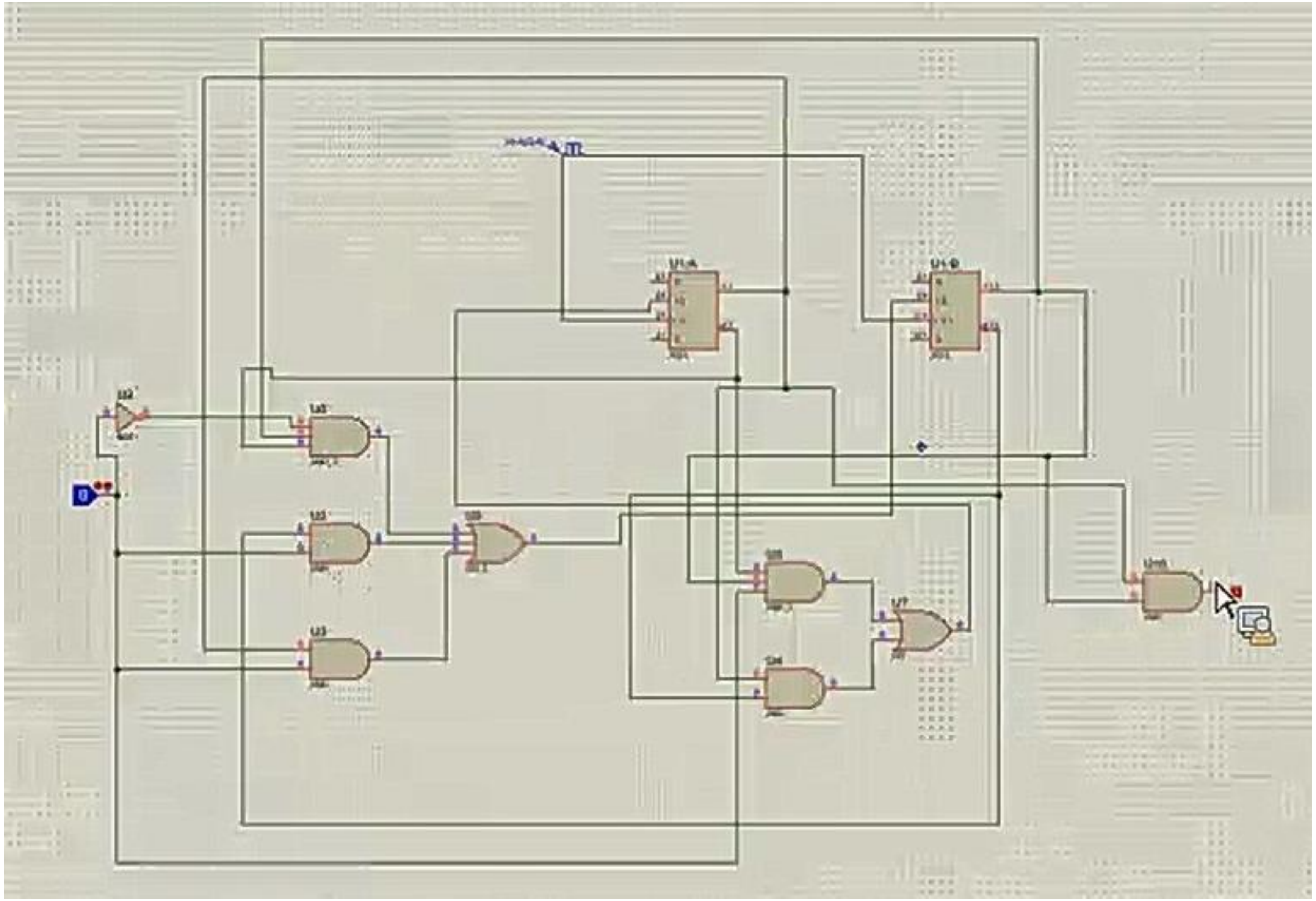


a	b	x	a	b	out
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	0	1	1

Db = ax + a'bx' + b'x

Da = ab' + a'bx

<table>
<tr><td>x \ ab</td><td>00</td><td>01</td><td>11</td><td>10</td></tr>
<tr><td>0</td><td></td><td>|</td><td>|</td><td>|</td></tr>
<tr><td>1</td><td>|</td><td>|</td><td>| |</td><td>| |</td></tr>
</table>



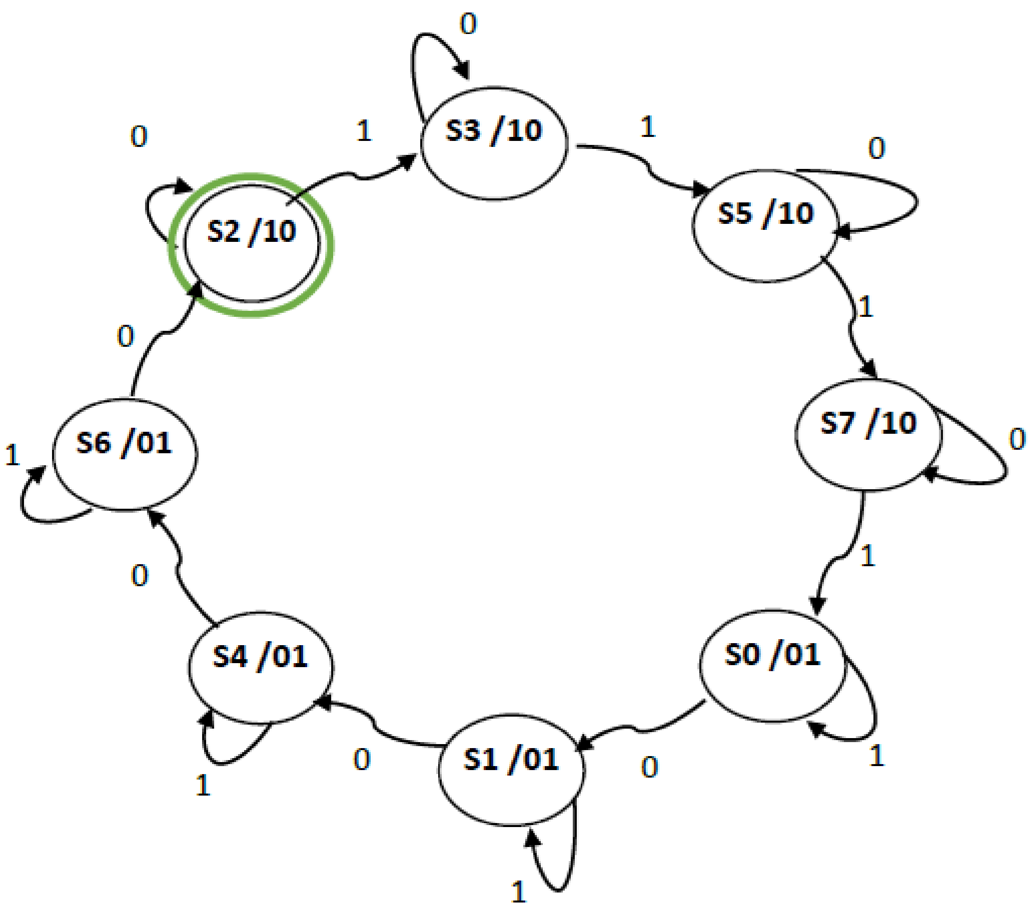
لطفا تمامی مراحل طراحی تا شبیه سازی و اجرای موارد زیر را انجام داده و ارسال کنید.

۱- ماشین موری طراحی کنید که توالی مقابل را شمارش کرده و با فلیپ فلاپهای نوع *jk* پیاده سازی نمایید.

a. توجه : هر وضعیت را معادل عدد باینری معادل خودش قرار دهید. (مثلا *S3* را ۰۱۱ و *s5* را ۱۰۱ در نظر بگیرید.

b. این مدار علاوه بر بیتهای حالت ، یک بیت ورودی و دو بیت خروجی دارد.

c. در مدار نهایی برای نمایش *STATE* ها سون سگمنت و نمایش خروجی ها *LED* قرار دهید.



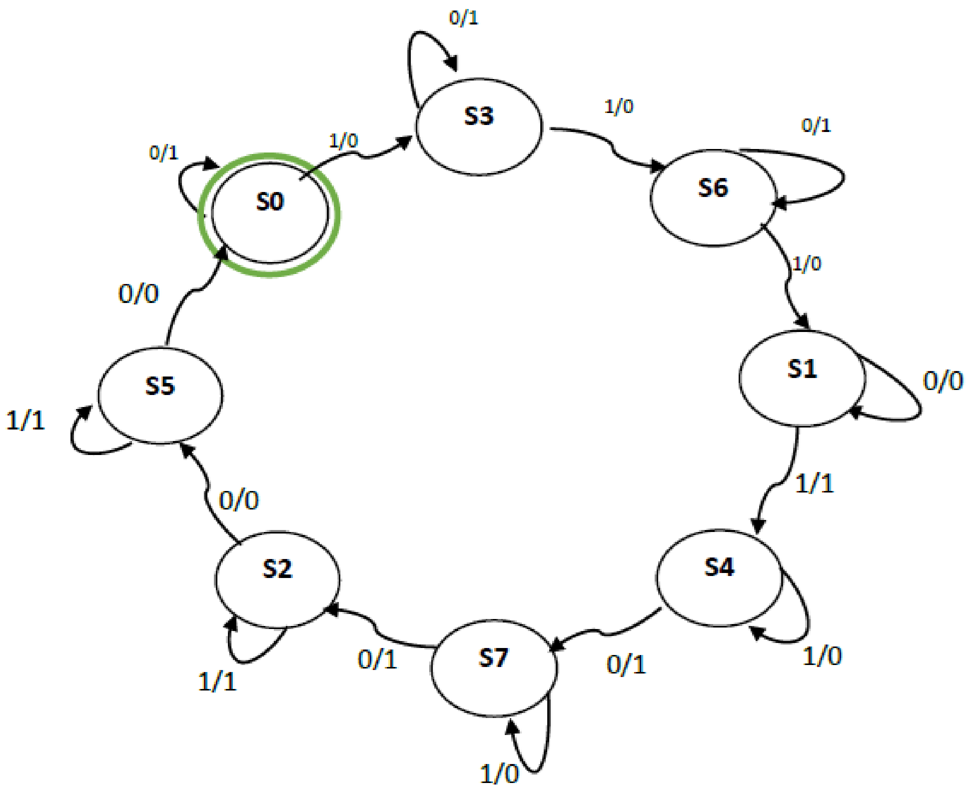
لطفا تمامی مراحل طراحی تا شبیه سازی و اجرای موارد زیر را انجام داده و ارسال کنید.

۲- ماشین میلی طراحی کنید که توالی مقابل را شمارش کرده و با فلیپ فلاپهای نوع *T* پیاده سازی نمایید.

a. توجه : هر وضعیت را معادل عدد باینری معادل خودش قرار دهید. (مثلا *S3* را ۰۱۱ و *s5* را ۱۰۱ در نظر بگیرید.

b. این مدار علاوه بر بیتهای حالت ، یک بیت ورودی و یک بیت خروجی دارد.

c. در مدار نهایی برای نمایش *STATE* ها سون سگمنت و نمایش خروجی ها *LED* قرار دهید.

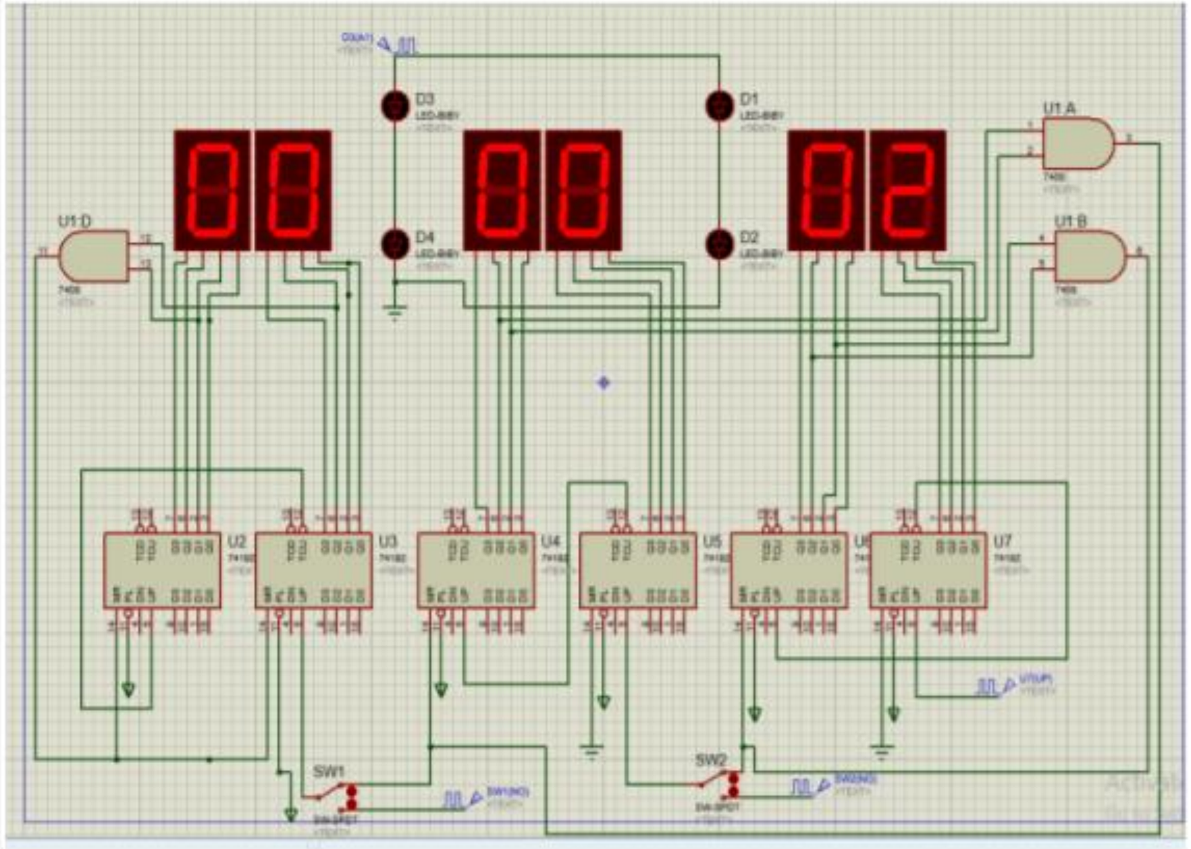


ساعت دیجیتال

در این پروژه می باست با استفاده از شبیه ساز پروتئوس یک ساعت دیجیتال با نمایشگر 7segmnt طراحی نمایید.

- ✓ این ساعت باید قابلیت ست شدن داشته باشد.بدین صورت که آنراوی ساعت مورد نظر تنظیم و با شروع کارمدار از آن ساعت شمارش انجام شود.برای هر کدام از ثانیه دقیقه و ساعت دو 7-seg استفاده کنید.
- ✓ مدار باید قابلیت تبدیل به تایمر داشته باشد.به این معنی که روی عدد مورد نظر ست شده و شمارش به صورت پایین شمار انجام شود.
- ✓ امکان تنظیم هشدار.به این معنی که هشدار برای ساعت مشخص تنظیم شده و با رسیدن به آن ساعت یک LED روشن شود.
- ✓ امکان انتخاب نمایش ساعت به صورت ۲۴ ساعته و ۱۲ ساعته .در حالت ۱۲ ساعته دو LED حالت AM و PM را نمایش دهد.(اضافه کردن این بخش نمره مثبت خواهد داشت)

شکل کلی مدار به صورت زیر میباشد



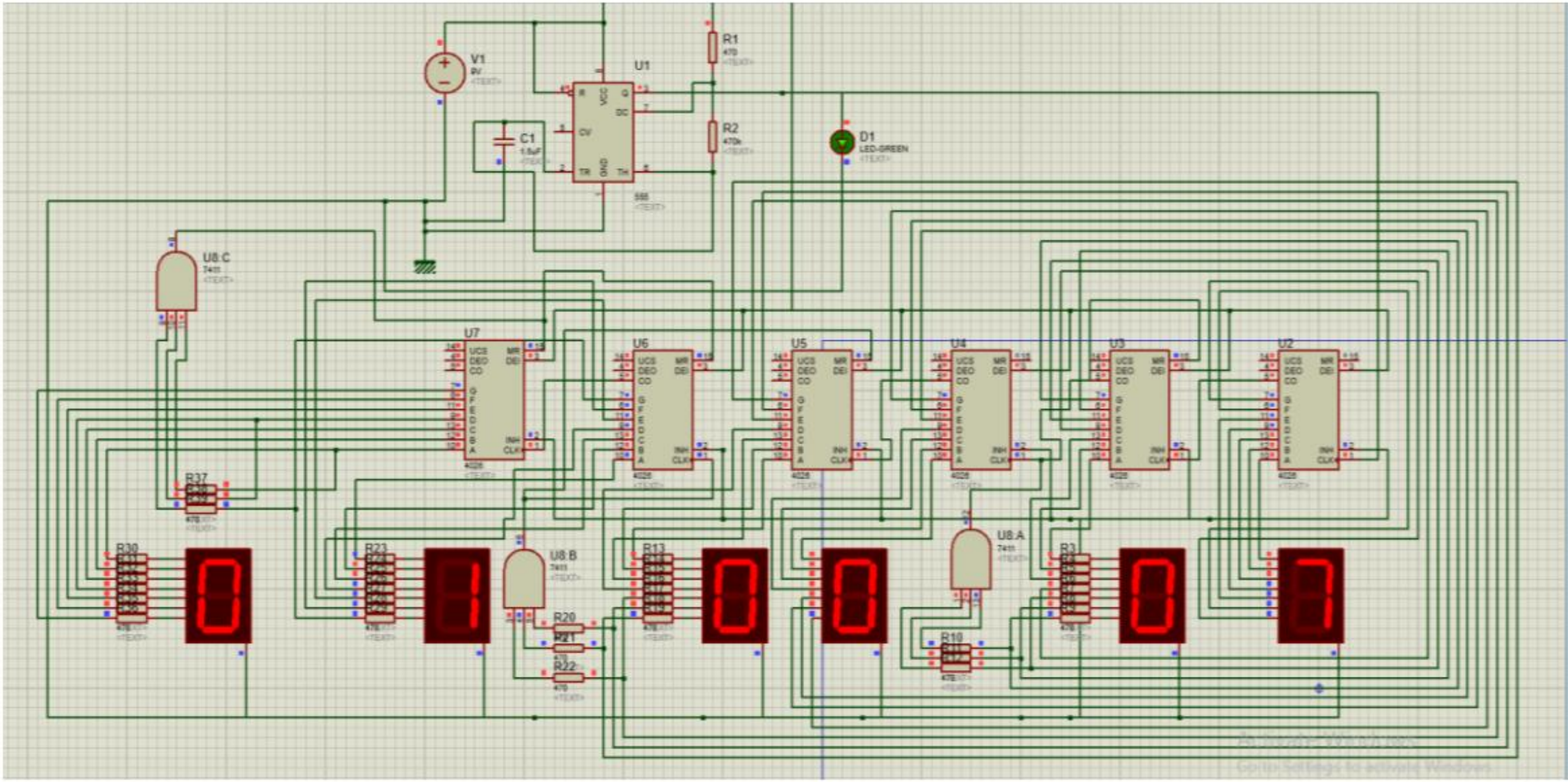
برای پیاده سازی طرح ساعت دیجیتال با استفاده از نرم افزار پروتئوس از اجزا زیر استفاده میکنیم.

1)7SEG-BCD
2)4082 Dual 4-input AND Gate
3)7408 2-input AND Gate
4)74192
5)LED
6)Button
7)Switch

ژراتور DC برای انتخاب صفر و 1 منطقی

کلاک منبع

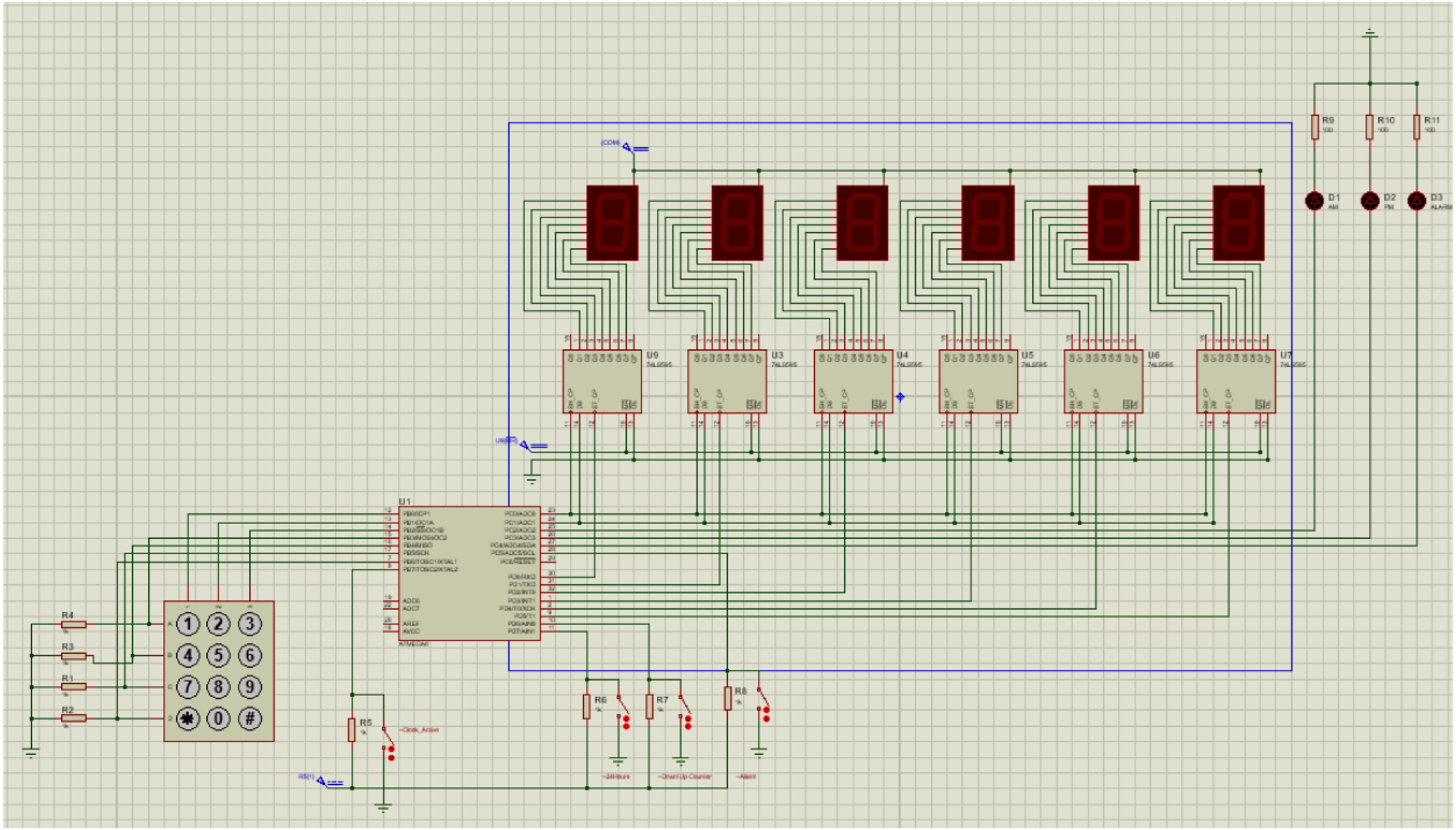
- در نهایت عملکرد مدار به صورت زیر خواهد بود.



شکل۱۲: عملکرد ساعت دیجیتال بعد از تکمیل شدن

قطعات مورد نیاز

- تایمر ۵۵۵
- آی‌سی ۴۰۲۶
- آی‌سی ۷۴۱۱ (گیت AND با سه ورودی)
- نمایشگر سون سگمنت کاتد مشترک
- خازن با مقدار ۱.۵ میکرو فاراد
- مقاومت‌های ۴۷۰ اهمی و ۴۷۰ کیلو اهمی
- منبع ولتاژ (باتری) ۹ ولتی
- ال ای دی سبز رنگ

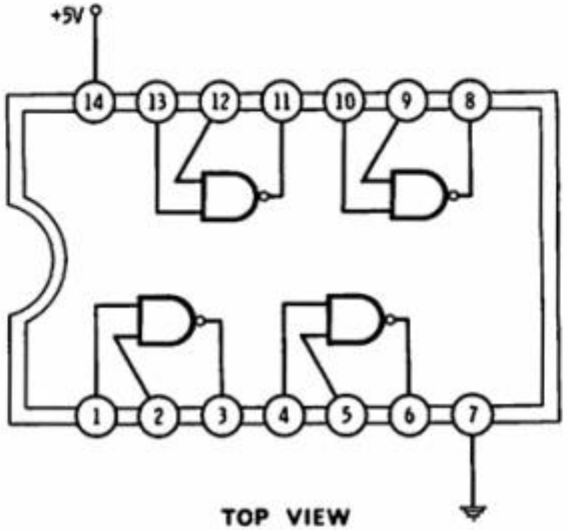


مدار ۵ شمای کلی مدار ساعت دیجیتال

دیتا شیت آی سی ها

7400

QUAD 2-INPUT NAND GATE

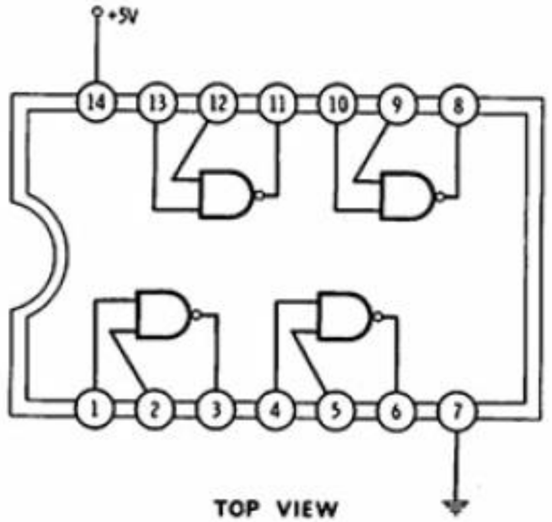


All four positive-logic NAND gates may be used independently. On any one gate, when *either* input is *low* the output is driven *high*. If *both* inputs are *high* the output is *low*.

Propagation delay .... 10 nanoseconds average

Current per package .... 12 milliamperes average

QUAD 2-INPUT NAND GATE
(Open-Collector Output)



TOP VIEW

All four positive-logic NAND gates may be used independently. On any one gate, with *either* input *low*, the output is driven to an *open circuit*. When both inputs are high, the output is *low*. An output-high state can be obtained only by adding an external resistor, usually 2.2K, from output to +5 volts.

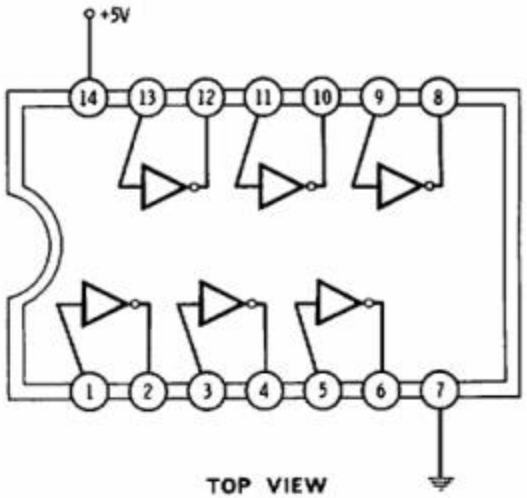
The pinouts on the 7403 are identical to the logically similar 7400. The circuitry is identical to the 7401. Note that this is a NAND gate, not a NOR gate.

Propagation delay .... 8 nanoseconds to output low,
35 nanoseconds to open circuit

Current per package .... 8 milliamperes average

7404

HEX INVERTER



TOP VIEW

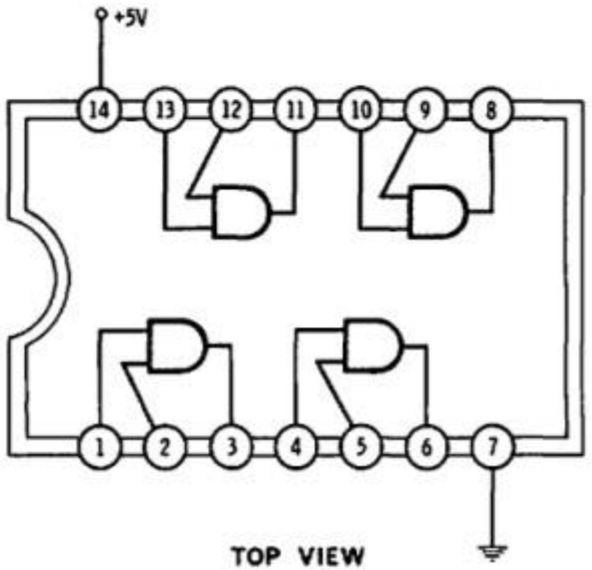
All six inverters may be used independently. On any one inverter, the *low*-input condition drives the output *high*. The *high*-input condition drives the output *low*.

Propagation delay .... 10 nanoseconds average

Current per package .... 12 milliamperes average

7408

QUAD 2-INPUT AND GATE



TOP VIEW

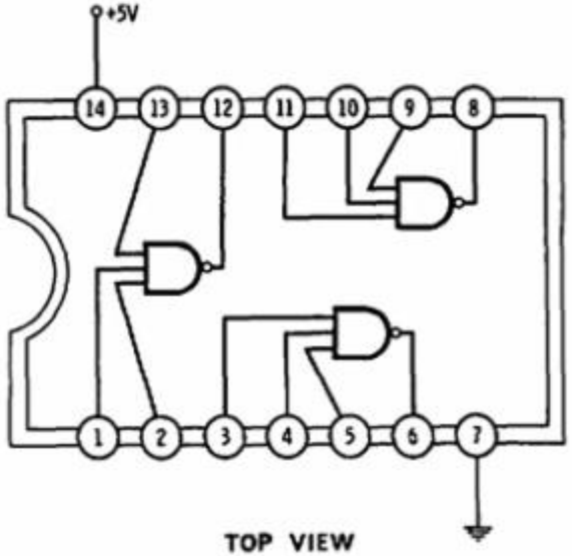
All four positive-logic AND gates may be used independently. On any one gate, when *either* input is *low*, the output is *low*. When both inputs are *high* the output is *high*.

Propagation delay .... 15 nanoseconds average

Current per package .... 16 milliamperes average

7410

TRIPLE 3-INPUT NAND GATE

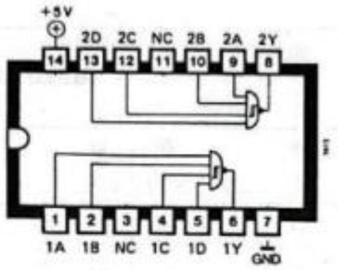


TOP VIEW

All three positive-logic NAND gates may be used independently. On any one gate, when *any* input is *low*, the output is driven to a *high* state. When *all* three inputs are *high*, the output is driven to a *low* state.

Propagation delay .... 9 nanoseconds average

Current per package .... 6 milliamperes average



Description:
This package contains two 4-input NAND Schmitt-triggers.

Mode of operation:
Each of the NAND gates can be used independently.
For each gate, the output is high, if one or more inputs are low. If all four inputs are high, the output will be low.
This device, because of the internal hysteresis of 0.8 V, is ideal for input signals that are subject to noise or have slow rise and fall times. In addition, it may be used in astable or monostable applications.
If the input voltage is rising in a positive direction, the output will change at 1.7 V. If the input voltage is moving in the negative direction, the change takes place at 0.9 V. For this reason, the hysteresis, or the "dead band" is 0.8 V. This is temperature compensated internally.

Inputs				Output
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

Application:
Level detection and pulse shaping, use in systems with noisy signals, monostable and astable multivibrators, implementation of NAND, AND and inverter functions

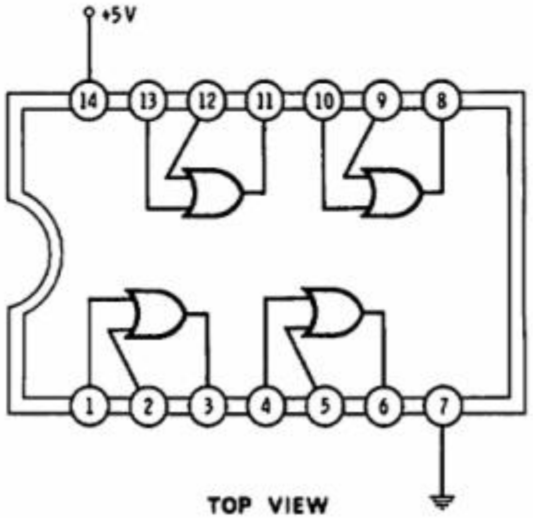
Data:		Std	ALS	AS	F	H	L	LS	S
Propagation delay	ns	16	10		7.8			16.5	
Hysteresis	V	0.8	0.8		0.8			0.8	
Supply current	mA	17	4		5.5			3.5	
Families:		●	●		●			●	

Dual 4-INPUT SCHMITT-TRIGGER NAND GATE

7413

7432

QUAD 2-INPUT OR GATE



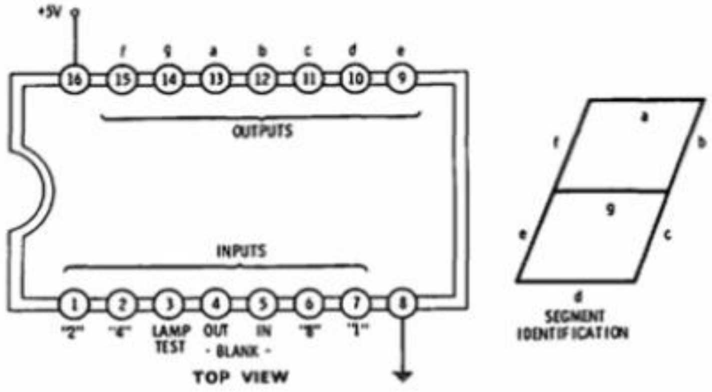
TOP VIEW

All four positive-logic OR gates may be used independently. On any one gate, when *either* input is *high,* the output is driven *high*. When *both* inputs are *low* the output is *low.*

Propagation delay .... 12 nanoseconds average

Current per package .... 19 milliamperes

BCD TO 7-SEGMENT DECODER-DRIVER
(Low=on, 40-mA, 30-Volt Outputs)



This package accepts a 1-2-4-8 positive-logic Binary Coded Decimal input and converts it to the proper pattern to light a 7-segment display. A *low* output is intended to light the segment.

The outputs can sink 40 milliamperes in the low state and can withstand 30 volts in the high state. Note that the *supply* must remain at +5 volts. An output-high state can be obtained only if a display device or resistor pulls the output to some positive voltage less than 30 volts.

Current-limiting resistors, typically 330 ohms, must be used when drving a light emitting diode display with this package. Incandescent or fluorescent readouts can be directly driven.

The Lamp Test input should remain high. Bringing the Lamp Test to ground simultaneously brings all the outputs to ground.

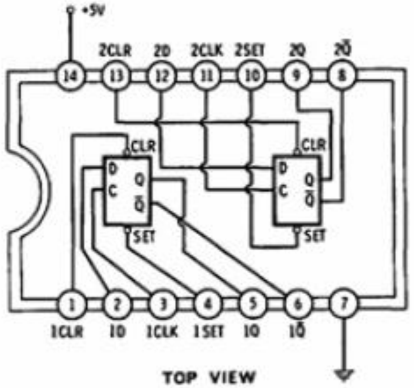
A low on the Blanking *input* will extinguish only character "0." A low on the Blanking output is provided to extinguish the character "0" of the next stage if leading-edge blanking is desired.

A low on the Blanking *output* will extinguish the display. It is permissible to short this output to ground.

Propagation delay .... 45 nanoseconds

Current per package .... 43 milliamperes

DUAL D EDGE-TRIGGERED FLIP-FLOP
(With Preset and Preclear)



TOP VIEW

Contains two independent positive-edge-clocked D flip-flops. This is a clocked logic block and is covered in detail in Chapter 5. There are two outputs: Q, and its complement $\overline{Q}$.

The information presented to the D input goes on to the Q output whenever the clock input changes from a low to a high level. The *only* time the output can change is when the clock goes positive; changes on the D input are not passed on if the circuit is not clocked.

If D is high, on clocking, Q goes high and $\overline{Q}$ goes low. If D is low, on clocking, Q goes low and $\overline{Q}$ goes high.

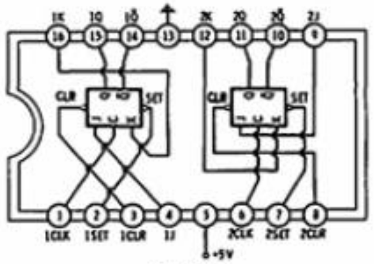
Information on the D input can be changed at any time. It is only its value at the instant of the positive clock edge that matters; this is what is entered into the flip-flop.

The Clear and Set inputs should be left or tied positive for normal operation. If the Clear input is grounded, the flip-flop *immediately* goes into the state with Q low and $\overline{Q}$ high. If the Set input is grounded, the flip-flop *immediately* goes into the state with Q high and $\overline{Q}$ low. Set and Clear should *never* be simultaneously grounded or a disallowed state will result.

Maximum toggle frequency .... 25 megahertz

Current per package .... 17 milliamperes

DUAL JK LEVEL-TRIGGERED FLIP-FLOP (With Preset and Preclear)



TOP VIEW

Contains two independent level-clocked JK flip-flops. Note the unusual supply connections.

This is a clocked logic block and is covered in detail in Chapter 5. There are two outputs: Q, and its complement $\overline{Q}$.

Under certain input conditions, Q and $\overline{Q}$ can change whenever the Clock input goes to a low level. The Q and $\overline{Q}$ outputs do not change for a change in the J and K inputs; the only time they can change is as the input clock goes to a low level.

If J and K are grounded, the clock does *nothing*. If J and K are made positive, the clock changes the output states on Q and $\overline{Q}$, or *binarily divides*. If J is high and K is low, clocking makes Q high and $\overline{Q}$ low. If J is low and K is high, clocking makes Q low and $\overline{Q}$ high.

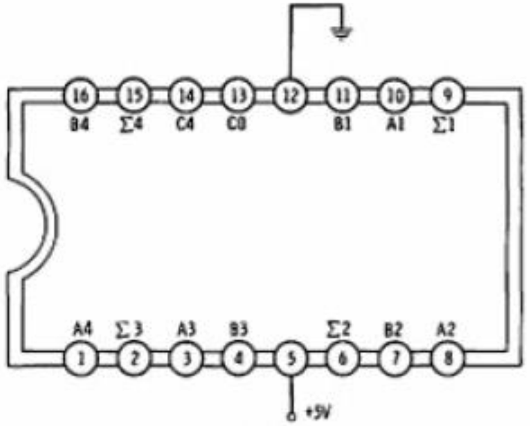
Information on the J and K inputs can be changed only once immediately after clocking. Further changes can bring about invalid operation (see Chapter 5). The clock must be conditioned to drop very rapidly per desired operation.

The Clear and Set inputs should be left, or tied positive for normal operation. If the Clear input is grounded, the flip-flop *immediately* goes into the state with Q low and $\overline{Q}$ high. If the Set input is grounded, the flip-flop *immediately* goes into the state with Q high and $\overline{Q}$ low. Set and Clear should *never* be simultaneously grounded, or a disallowed state will result.

Maximum toggle frequency .... 20 megahertz

Current per package .... 20 milliamperes

4-BIT FULL ADDER



TOP VIEW

This is an arithmetic unit that provides the sum of two 4-bit binary numbers. Note the unusual supply connections.

The *A* number is weighted A1 = 1, A2 = 2, A3 = 4, A4 = 8 and is used as one input.

The *B* number is weighted B1 = 1, B2 = 2, B3 = 4, B4 = 8 and is used as a second input.

The sum of these two numbers, A and B, appears as $\Sigma1 = 1$, $\Sigma2 = 2$, $\Sigma3 = 4$, and $\Sigma4 = 8$.

If the answer exceeds decimal 15 (binary 1111), a 1 also appears on the C4 line as a Carry Output.

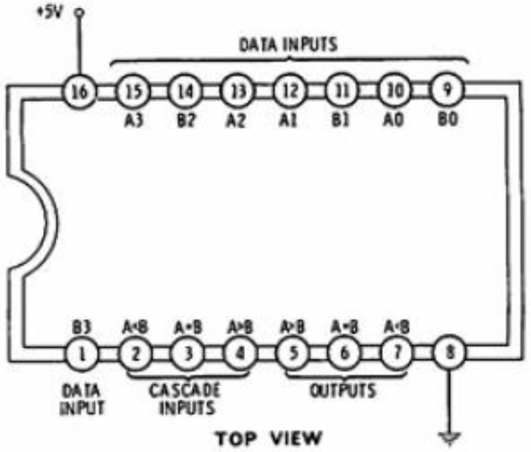
When used only with 4-bit numbers, the C0 input should be grounded. When used as the upper 4 bits on an 8-bit number, the C0 input is connected to the C4 output of the previous (less significant) four stages.

Positive logic with 1 being at high level is used.

Propagation delay .... 16 nanoseconds typical per package

Current per package .... 60 milliamperes average

4-BIT MAGNITUDE COMPARATOR



This package compares two 4-bit words and provides an output indicating whether they are equal or which is larger.

Usually the input data words to be compared are weighted A1 = 1, A2 = 2, A3 = 4, and A4 = 8, while the second word is weighted B1 = 1, B2 = 2, B3 = 4, and B4 = 8.

If only 4-bit words are being compared, the A = B Cascade input should be wired *high*. The A > B and A < B Cascade inputs should be *grounded*.

If the two words are equal, the A = B goes high. If A > B, the A > B output goes high. If A < B, the A < B output goes high. Thus, a high state appears at the proper output; the other two remain low.

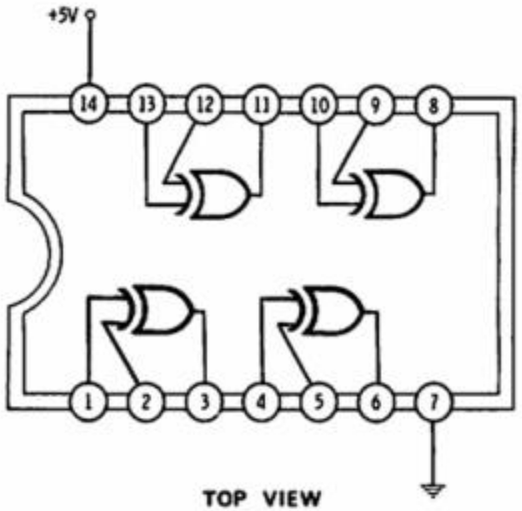
To work with 8-bit words, the outputs of the first 4-bit comparison (least significant bits) are connected to the Cascade Inputs of the second stage. The final answer appears as the outputs of the most significant 4-bit comparator, with the proper output going high.

Propagation delay .... 23 nanoseconds

Current per package .... 55 milliamperes

7486

QUAD EXCLUSIVE-OR GATE



TOP VIEW

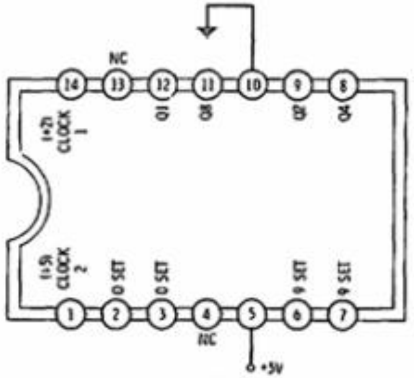
The package contains four independent EXCLUSIVE-OR gates. They may be used separately.

On any one gate, when one, *but not both, inputs are high,* the output is *high.* When *both inputs are high* or *both inputs are low,* the output is *low.*

Propagation time .... 18 nanoseconds

Current per package .... 30 milliamperes

DECADE COUNTER (÷10) (Ripple, not Presettable, not Unit-Cascadable)



TOP VIEW

This is a divide-by-2 and a divide-by-5 counter in a single package. They may be used together as a divide-by-10 or separately. It ripple-counts in the BCD-up direction. Note the unusual supply pinouts.

For a BCD counter, weighted 1-2-4-8, enter via Clock 1, and jumper Q1 to Clock 2. Both 9-Set and both 0-Set inputs must be *grounded* for normal counting.

The counter advances on the negative-going clock edge. The clock must be properly conditioned and made bounceless and noise free. If a conventional decade counter is needed, *all set terminals must be held at ground.*

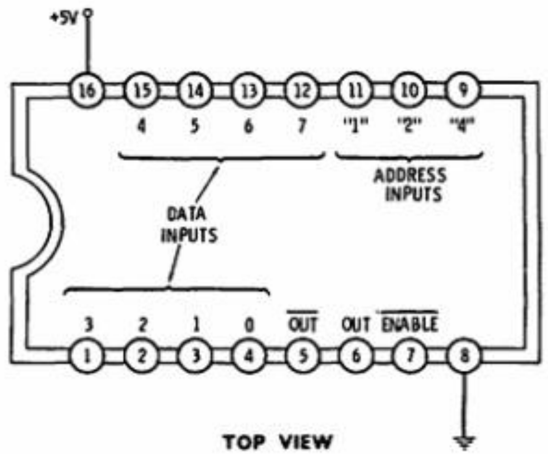
The counter may be reset to zero by bringing either or both 0-Set inputs positive. The counter may be preset to 9 by bringing either or both 9-Set inputs positive.

An external jumper must be provided between counter halves. If entry is via Clock 2, and Q8 is jumpered to Clock 1, a counter weighted 1-2-4-5 results, with Q1 as the most significant output and a symmetrical square wave at the output. More details on this device appear in Chapter 6. The circuit is not unit-cascadable.

Typical maximum toggle frequency .... 18 megahertz

Current per package .... 32 milliamperes

1-OF-8 DATA SELECTOR



TOP VIEW

This package selects one of eight inputs and provides the data on the selected input or its complement as an output. It will also generate *any* logic function of four or less input variables. (See Chapter 3.)

Inputs are selected by applying a code from 000 through 111 on the 1, 2, and 4 Address inputs. The data on the selected input appear at pin 6; the complement of the selected data appears at pin 5. Pin 5 is faster in responding, as pin 6 is an inverter/follower.

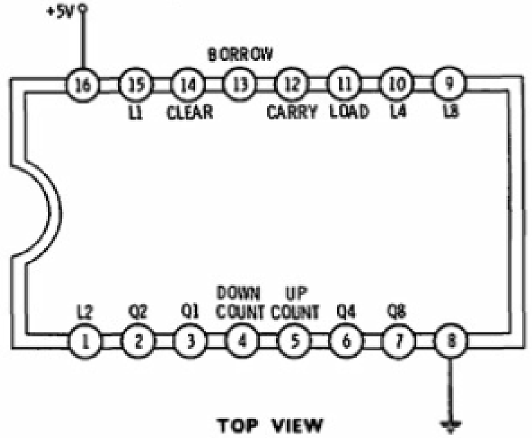
The Enable input (sometimes called a Strobe) must be *low* for normal operation. Driving it high drives the pin-6 output *low* and the pin-5 output *high,* independently of the condition of the selected input.

For logic function generation, three of the variables are applied to the Address inputs. The selected Data inputs are connected low, high, to the fourth variable or to the complement of the fourth variable per the desired truth table. See Chapter 3 for more details.

Select time .... 19 nanoseconds

Current per package .... 29 milliamperes

DECADE (÷10) UP/DOWN COUNTER (Carry, Borrow, Presettable, Synchronous)



TOP VIEW

This is a synchronous decade (base-10) counter that counts in either direction. Two input clocks are used, and stages are Carry/Borrow cascaded.

For a normal up-counting sequence, Load should be high, and Clear should be low.

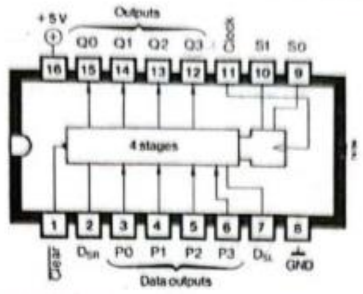
The counter advances one count on each ground-to-positive transition of the Up-Count input clock. It backs up one count on each ground-to-positive transition of the Down Count input clock. When up-counting, hold the Down-Count input high. When down-counting, hold the Up-Count input high.

To load, the desired word is placed on Load inputs L1, L2, L4, and L8. The Load input is then briefly brought low. To clear the counter, the Clear input is briefly made *positive*. Note that the Clear must be low for normal counting.

Stages are cascaded by connecting Carry to Up Count and Borrow to Down Count. See Chapter 6. For more details, consult data sheet.

Maximum operating frequency .... 32 megahertz

Current per package .... 65 milliamperes



Description:
This package contains a bidirectional 4-bit shift register for parallel and serial input or output, with a clear input.

Mode of operation:
When the $\overline{\text{Clear}}$ input is taken low, all outputs (Q0 - Q3) are set low, regardless of the state of the other inputs.
When the $\overline{\text{Clear}}$ input is high, the operating mode is determined by the two mode control inputs (S0, S1). S0 low and S1 high selects a left shift. The serial data is applied to the D_{SL} input. With S0 high and S1 low, a right shift is selected and the serial data is applied to D_{SR}.
If both S0 and S1 are high, parallel loading of the data at P0 - P3 is selected. The input of serial data is inhibited during parallel loading.
Serial and parallel data is entered in to the shift register synchronously on the low-to-high transition (positive edge) of the clock pulse on pin 11. The data must be present at the data inputs before the positive edge of the clock pulse.
If both S0 and S1 are low, the clock is inhibited. These two inputs should only be changed when the clock input is high.

Clock	Mode Select S0	Mode Select S1	$\overline{\text{Clear}}$	Function
X	L	L	H	no change
↑	H	L	H	Right shift (Q0 -> Q3)
↑	L	H	H	Left shift (Q3 -> Q0)
↑	H	H	H	Parallel load
X	X	X	L	Reset (clear)

Application:
Shift registers, data storage, serial-parallel and parallel-serial converters.

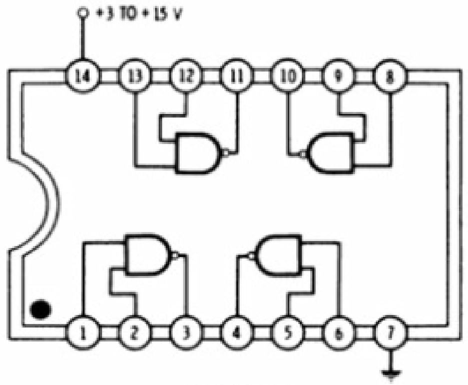
Data:		Std	ALS	AS	F	H	L	LS	S
Max. clock frequency	MHz	25	110		150			25	75
Supply current	mA	39	35		33			15	85
Families:		●		●	●			●	●

4-bit bidirectional SHIFT REGISTER (parallel/serial-in, parallel/serial-out) with clear

74194

4011

QUAD 2-INPUT NAND GATE



TOP VIEW

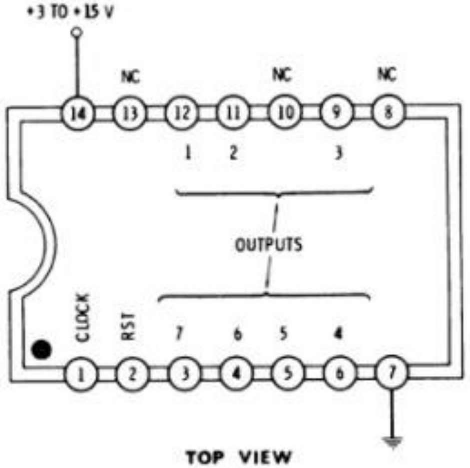
All four positive-logic NAND gates may be used independently.

On any one gate, with *either* or both inputs *low*, the output will be *high;* with both inputs *high*, the output will be *low*.

Propagation delay is 25 nanoseconds at 10 volts and 60 nanoseconds at 5 volts. Total package current at 1 megahertz is 0.4 milliampere at 5 volts and 0.8 milliampere at 10 volts.

Device is functionally equivalent to 7400 (TTL) and 74C00 (CMOS).

7-STAGE (÷128) BINARY RIPPLE COUNTER



TOP VIEW

This is a binary ripple counter that counts in the up direction using positive logic.

The reset input is normally held at ground. Every time the clock changes from positive to ground, the counter advances one count. The 1 output divides the input clock by $2^1 = 2$. The 2 output divides the input clock by $2^2 = 4$, up to the 7 output which divides by $2^7 = 128$. Making the reset input positive forces all outputs to ground and holds them there until the reset returns to ground.

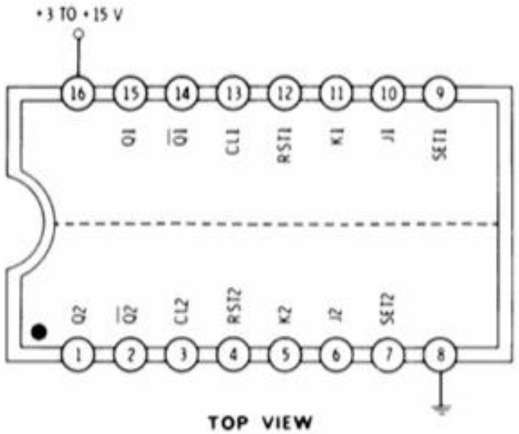
The clock input must be conditioned to be noiseless and fall only once per desired count. Clock rise and fall times should be faster than 5 microseconds.

Since this is a ripple counter, the outputs change in sequential order. Incorrect counts will briefly result during the settling time. Device is functionally and pin-for-pin equivalent to the 74HC4024 for LS TTL levels.

Maximum input freqency is 7 megahertz at 10 volts and 2.5 megahertz at 5 volts. Total package current is 0.2 milliampere at 5 volts and 0.4 milliampere at 10 volts for a 1-megahertz clocking rate. Consult the specific manufacturer's data sheet for propagation delay times.

Note: Device should not be confused with the MC4024 (74424) MTTL dual voltage-controlled astable IC.

DUAL JK FLIP-FLOP



TOP VIEW

Each flip-flop may be used independently. There are two modes, *clocked* and *direct*.

In the *clocked* mode, the direct set and clear inputs must remain at ground. Inputs to the J and K lines decide what the flip-flop is going to do. The actual operation doesn't happen until the positive edge (ground-to-positive transition) of the clock.

If J and K remain grounded, clocking does nothing.
If J is positive and K grounded, clocking forces Q positive and $\overline{Q}$ to ground.
If J is grounded and K positive, clocking forces Q to ground and $\overline{Q}$ positive.
If both J and K are positive, clocking alternates the Q and $\overline{Q}$ states.

In the *direct* mode, a positive set input forces Q positive and $\overline{Q}$ to ground. A positive reset input forces Q to ground and $\overline{Q}$ positive. Should both set and reset simultaneously go positive, both Q and $\overline{Q}$ will also go positive. This is usually a disallowed state. The last direct input to go to ground will determine the final state of the Q and $\overline{Q}$ outputs. The direct inputs override the clocked inputs.

The clock input must be noiseless and have only a single ground-to-positive edge transition per desired clocking. Clock rise and fall times should be 5 microseconds or faster.

Maximum clock frequency is 8 megahertz at 10 volts and 3 megahertz at 5 volts. Total package current is 0.4 milliampere at 5 volts and 0.8 milliampere at 10 volts for a 1-megahertz clock frequency.

Device is functionally equivalent to the 7473, 7476, 74107, 74111, and 74167 (all TTL), and the 74C73, 74C76, and 74C107 (all CMOS).