Based on the information provided in the two articles, I have designed a 2x2 memory bank with control signals and transposable ability. I have used the transposable addressing scheme described in the design.

SRAM (0,0)	SRAM (0,1)
SRAM (1,0)	SRAM (1,1)

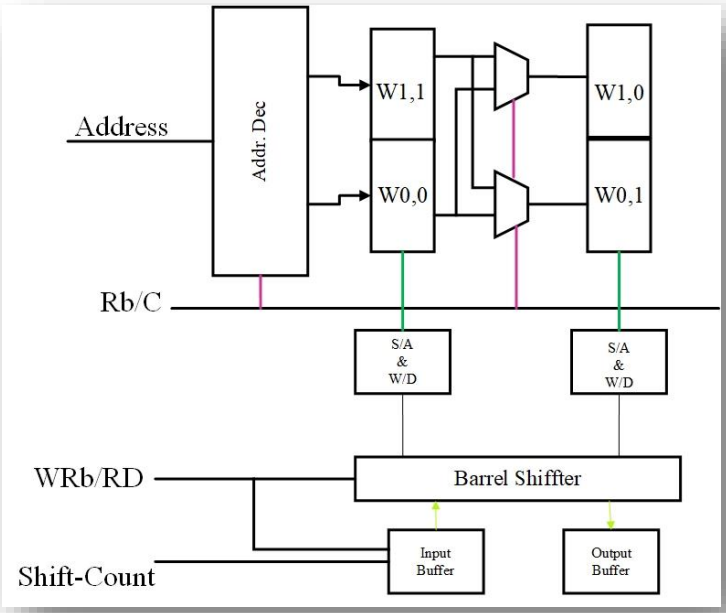

Fig 1: The 2x2 memory bank with control signals and transposable ability scheme

The memory bank's SRAM cells are each identified as SRAM (row, column). Two columns (0 and 1) and two rows (0 and 1) make up the memory bank.

SRAM Cell (0,0): 0

SRAM Cell (0,1): 1

SRAM Cell (1,0): 0

SRAM Cell (1,1): 1

Control Signals:

- Write Enable (WE): This is an active-high signal used to enable write operations. When WE are high, data can be written into the memory cells.
- Read Enable (RE): This is an active-high signal used to enable read operations. When RE is high, data can be read from the memory cells.
- Row Bit/Column Bit (Rb/C): This control signal determines the access mode: 0 for row-wise access and 1 for column-wise access. It selects whether to read or write data in a regular or transposed manner.
- Write Data (WD): This signal carries the data to be written into the memory cells during a write operation.
- Read Data (RD): This signal carries the data read from the memory cells during a read operation.

Write some values (1 or 0) into the SRAM cells and read them both regular and transposed to assess the design.

1. **Read**
   According fig.1:

   - **Regular Read Operation:**
     - ✓ Set RE = 1 to enable the read operation.
     - ✓ Set the row address = 1.
     - ✓ The data from SRAM cells in row 1 will appear at the output (RD).

   - **Transposed Read Operation:**

- ✓ Set Rb/C to 0 to **select row-wise access**.
- ✓ Set RE to 1 to enable the read operation.
- ✓ Provide the row address to select the desired row (0 or 1).
- ✓ The data from the selected row will appear at the output (RD).

Example: To read from row 1 in a regular way:

- Set Rb/C = 0 (row-wise access).
- Set RE = 1 (enable read operation).
- Provide row address = 1.
- The data from SRAM cells (1,0) and (1,1) will appear at the output (RD).

- ✓ Set Rb/C to 1 to **select column-wise access**.
- ✓ Set RE to 1 to enable the read operation.
- ✓ Provide the column address to select the desired column (0 or 1).
- ✓ The data from the selected column will appear at the output (RD).

Example: To read from column 0 in a transposed way:

- Set Rb/C = 1 (column-wise access).
- Set RE = 1 (enable read operation).
- Provide column address = 0.
- The data from SRAM cells (1,1) and (0,1) will appear at the output (RD).

2. WRITE

- **Regular Write Operation:**

  To write data into the memory bank in a regular (row-wise) manner:

  - ✓ Set WE = 1 to enable the write operation.
  - ✓ Set the row address to select the desired row.
  - ✓ Provide the data to be written (Write_Data).

For example, to write data '1' into row 0 using the regular write operation:

- ✓ Set WE = 1 to enable the write operation.
- ✓ Set the row address = 0.

- ✓ Provide the data to be written (Write_Data = "01").
- ✓ The data '01' will be written into the SRAM cells in row 0.

- **Transposed Write Operation:**

  - ✓ Set Rb/C = 1 to select column-wise access.
  - ✓ Set WE = 1 to enable the write operation.
  - ✓ Provide the column address to select the desired column.
  - ✓ Provide the data to be written (Write_Data).

Example, the transposed write operation by writing data '0' into column 1:

- ✓ Set Rb/C = 1 (column-wise access).
- ✓ Set WE = 1 (enable write operation).
- ✓ Provide the column address = 1.
- ✓ Provide the data to be written (Write_Data = "00").
- ✓ The data '00' will be written into the SRAM cells in column 1.