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Controlling the Drain Side Tunneling Width to Reduce Ambipolar Current in Tunnel FETs Using Heterodielectric BOX

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***Abstract*— In this brief, we demonstrate using 2-D simulations that the use of a heterodielectric BOX (HDB) above a highly doped ground plane can control the tunneling width at the channel–drain interface and lead to a significant reduction in the ambipolar current in tunnel FETs (TFETs). The HDB consists of SiO_2 under the source and the channel regions, and HfO_2 under the drain region. When the thickness of the HDB is 25 nm and the ground plane is heavily doped, we show that the drain region at the channel–drain interface is effectively depleted. As a result, the tunneling width at the channel–drain interface increases leading to a complete suppression of ambipolar conduction in a TFET even when the gate voltage $V_{GS} = -0.8$ V.**

***Index Terms*— Ambipolarity, ON-state current, source-pocket (p-n-p-n) tunneling FET (TFET).**

I. Introduction

THE tunnel FET (TFET) has been proposed as a replacement of the standard CMOS for low-power applications [1]–[4]. The TFETs are characterized by low leakage currents, steep subthreshold swing, better immunity to short channel effects, and compatibility with the conventional CMOS process [1]–[9]. However, their application is limited due to the two fundamental problems: 1) a low ON-state current and 2) an ambipolar conduction. The limitation of low ON-state current in silicon TFETs can be solved using a p-n-p-n TFET with a source pocket instead of the conventional p-i-n structure. The p-n-p-n TFETs have been reported to have a steeper subthreshold slope, a reduced operating voltage, and an improved reliability compared with the p-i-n TFETs in addition to the increased ON-state current [10]–[12]. But the unique property of ambipolar conduction in TFETs limits their utility for digital circuit applications [13], [14]. To alleviate the ambipolar behavior, several device architectures, including gate–drain underlap, low drain doping, lateral heterostructure with high bandgap material at drain side, and the low-*k* spacers have been proposed [13]–[17]. Although these methods reduce ambipolar current, they can only be realized at the cost of increased fabrication complexity and reduced ON-state current due to increased drain series resistance. Recently, a novel gate-on-drain overlap method was proposed to control the ambipolar characteristics of the TFETs [18]. However, this approach does not provide scaling flexibility as it requires a gate-on-drain overlap length of 30 nm to suppress the ambipolar currents up to a gate voltage (V_{GS}) of −0.5 V.

In this brief, we demonstrate an approach to completely eliminate the ambipolar conduction in TFETs using a heterodielectric BOX (HDB) above a heavily doped (p^+) ground plane of an n-channel p-n-p-n TFET. The proposed device architecture facilitates the depletion of the drain region at the channel–drain interface increasing the tunneling barrier width on the drain side resulting in the suppression of the ambipolar conduction. Using calibrated 2-D simulations, we demonstrate that the ambipolar conduction is completely eliminated in the proposed HDB p-n-p-n TFET, even for a gate voltage $V_{GS} = -0.8$ V, when the BOX thickness is 25 nm and the ground plane is heavily doped.

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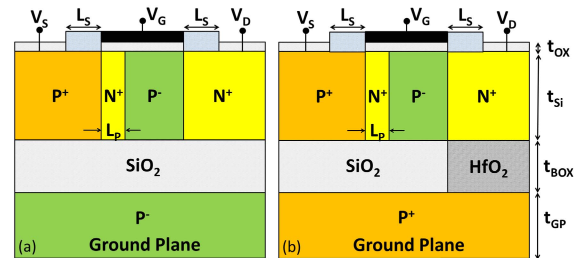

Fig. 1. Schematic of (a) conventional p-n-p-n TFET and (b) HDB p-n-p-n TFET.

II. Device Structure and Simulation Parameters

Fig. 1 shows the schematic of the conventional source-pocket p-n-p-n TFET and the proposed HDB p-n-p-n TFET. The only difference between these two structures is that the latter has an HDB in which the high-*k* dielectric is placed just below the drain and a heavily p^+ doped ground plane is used instead of a lightly doped ground plane. The parameters used for the two devices in our simulations are listed in Table I.

III. Simulation Results and Discussion

All the simulations were carried out using Silvaco Atlas, version 5.19.20.R [21]. Nonlocal band-to-band tunneling model was used to account for the tunneling in the lateral direction due to its better accuracy. To account for high field mobility effects, Lombardi mobility model was included.

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TABLE I
PARAMETERS USED FOR THE DEVICE SIMULATION

Parameter	PNPN TFET	HDB PNPN TFET
BOX thickness (t_{BOX})	25 nm	25 nm – 40 nm
Ground plane doping (N_A)	1 x 10^{17} cm^{-3}	1 x 10^{20} cm^{-3}
SOI film thickness (t_{Si})	10 nm	10 nm
Gate oxide (SiO_2) thickness (t_{OX})	1 nm	1 nm
Gate work function	4.33 eV	4.33 eV
Gate length	50 nm	50 nm
Source doping (N_A)	1 x 10^{20} cm^{-3}	1 x 10^{20} cm^{-3}
Drain doping (N_D)	5 x 10^{18} cm^{-3}	5 x 10^{18} cm^{-3}
Channel doping (N_A)	1 x 10^{17} cm^{-3}	1 x 10^{17} cm^{-3}
Source-pocket length (L_P)	4 nm	4 nm
Source-pocket doping (N_D)	1 x 10^{19} cm^{-3}	1 x 10^{19} cm^{-3}
Spacer between Gate and Source/Drain contacts [19] (L_S)	30 nm	30 nm

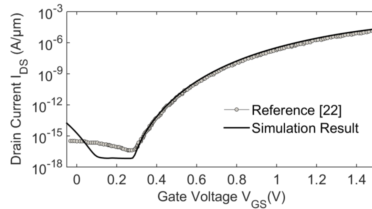

Fig. 2. Simulation models calibrated by reproducing the results of [22].

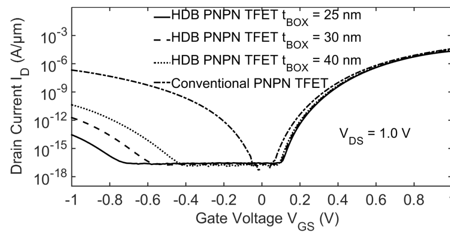

Fig. 3. Transfer characteristics of the conventional p-n-p-n TFET and the HDB p-n-p-n TFET for different BOX thicknesses at $V_{DS} = 1$ V.

Fermi–Dirac statistics and the Shockley–Read–Hall recombination model were also used. Bandgap narrowing model was enabled to consider the highly doped regions of the device. Although the defects and the trap-centers could be present at the Si–HfO_2 interface, we have considered a defect-free interface in our simulations. The ground plane is at the same potential with respect to the source which is grounded. As shown in Fig. 2, the simulation models were calibrated by reproducing the results reported in [22] since the simulation conditions are well explained in [22]. It may be pointed out that the main objective of this brief is to demonstrate the relative effect of the HDB above a highly doped ground plane on the device electrical characteristics and not to show the exact values of the currents.

Fig. 3 compares the transfer characteristics of the conventional p-n-p-n TFET and the proposed HDB p-n-p-n TFET for different BOX thicknesses (t_{BOX}). We observed that the ambipolar current is eliminated up to $V_{GS} = -0.5$ V when a BOX thickness of 40 nm is used. No ambipolar current is observed for a BOX thickness of 25 nm even for $V_{GS} = -0.8$ V. The drain region gets further depleted when a thinner BOX is used increasing the tunneling width on the drain side and hence significantly reducing the

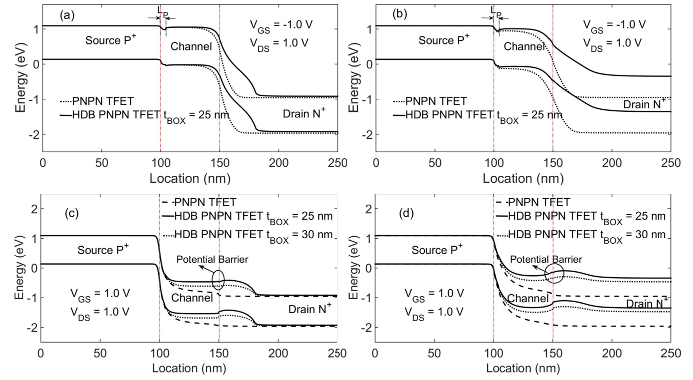

Fig. 4. Energy-band profiles of the conventional p-n-p-n TFET and the HDB p-n-p-n TFET at (a) 1 nm below Si–SiO_2 interface at the top and (b) 1 nm above the Si-BOX interface in the ambipolar-state and (c) 1 nm below Si–SiO_2 interface at the top and (d) 1 nm above Si–BOX interface in the ON-state.

ambipolar current. The suppression of ambipolar current observed in Fig. 3 is due to the depletion of the drain region at the channel–drain interface by the use of an HDB over a heavily doped ground plane. This can be understood from the band diagrams of the p-n-p-n TFET and the HDB p-n-p-n TFET at $V_{GS} = -1$ V and $V_{DS} = 1$ V, as shown in Fig. 4. Comparing Fig. 4(a) with Fig. 4(b), we observe that the HDB facilitates the depletion of the drain region at the channel–drain interface more at the bottom of the silicon film than at the top. This depletion of the channel-drain interface leads to an increase in the tunneling width resulting in a reduction of the ambipolar conduction.

It may be noted that the ON-state current of the proposed HDB p-n-p-n TFET decreases ($\sim$1.8 times) when the BOX thickness is reduced to 25 nm, as shown in Fig. 3. This slight reduction in the ON-state current can be understood from Fig. 4(c) and (d). With a reduction in the BOX thickness, the drain region depletion increases at the channel–drain interface resulting in a potential barrier for electrons at the channel–drain interface, which leads to a reduced ON-state current. The potential barrier height is more at the bottom of the silicon film than at the top due to which the electrons flow near the top surface. But for BOX thicknesses above 30 nm, this decrease in the ON-state current is negligible because the potential barrier becomes insignificant as the conduction band becomes nearly flat at the channel–drain interface. Therefore, we observe that to control ambipolar current without affecting the ON-state current, the HDB thickness should be above 30 nm when the drain doping (N_D) is 5×10^{18} cm^{-3}.

Fig. 5 shows the electron concentration contour plot of the conventional p-n-p-n TFET and the proposed HDB p-n-p-n TFET for $V_{GS} = -1$ V and $V_{DS} = 1$ V. The presence of high-k dielectric BOX under the drain facilitates the depletion of the drain region at the channel–drain interface as the effective oxide thickness is much smaller below the drain. However, the thickness of SiO_2 below the channel region is large enough to prevent depletion of the lightly doped channel region and, therefore, does not affect the ON-state current.

A higher ground plane doping or a thinner HDB is required to deplete the drain region effectively if a higher drain

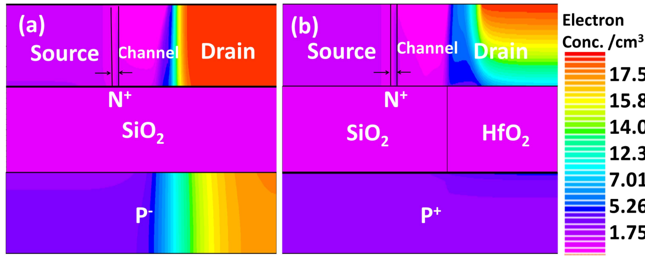

Fig. 5. Electron concentration contour plot of (a) conventional p-n-p-n TFET and (b) HDB p-n-p-n TFET for $V_{GS} = -1$ V and $V_{DS} = 1$ V.

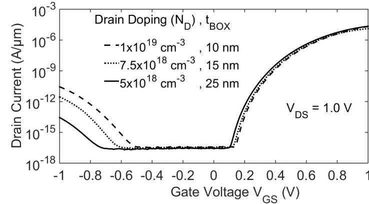

Fig. 6. Transfer characteristics of the HDB p-n-p-n TFET for different drain dopings and appropriate BOX thickness at $V_{DS} = 1$ V.

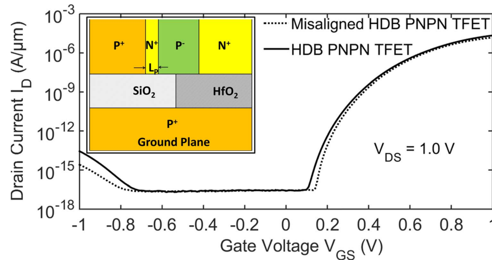

Fig. 7. Impact of HDB misalignment on the transfer characteristics of HDB p-n-p-n TFET with $t_{BOX} = 25$ nm. Inset: misaligned high-k dielectric BOX (halfway under the channel) in the HDB p-n-p-n TFET.

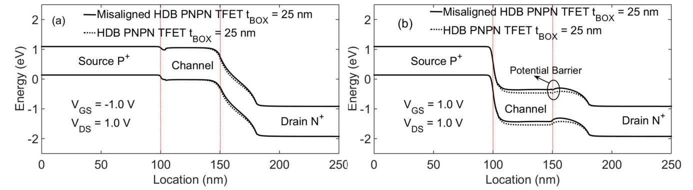

Fig. 8. Energy-band profiles of the HDB p-n-p-n TFET at 1 nm below Si–SiO_2 interface showing the effect of high-k dielectric BOX misalignment in (a) the ambipolar-state and (b) the ON-state.

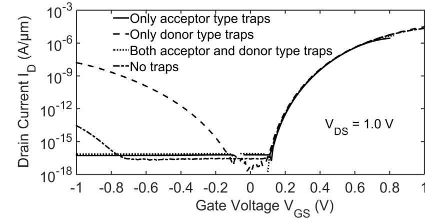

Fig. 9. Impact of traps at the Si/HfO_2 interface on the transfer characteristics of the HDB p-n-p-n TFET with $t_{BOX} = 25$ nm.

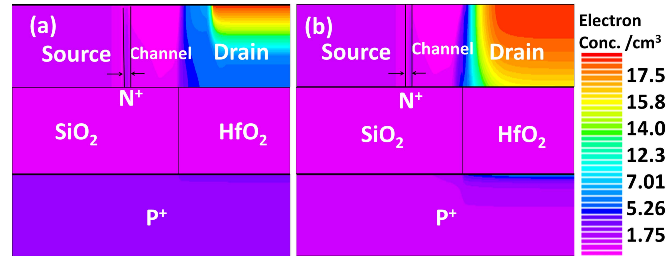

Fig. 10. Electron concentration contour plot showing the effect of (a) acceptor traps and (b) donor traps at the Si/HfO_2 interface for $V_{GS} = -1$ V and $V_{DS} = 1$ V.

doping is used. Fig. 6 shows the transfer characteristics of the proposed device for different drain dopings and the HDB thickness used to control the ambipolar conduction. We observe that a thinner BOX is effective in controlling the ambipolar current for a higher drain doping. The proposed method is able to suppress the ambipolar currents up to $V_{GS} = -0.5$ V even for a drain doping of 1×10^{19} cm^{-3} by using an HDB thickness of 10 nm. However, as the drain doping is increased beyond 1×10^{19} cm^{-3}, it becomes difficult to deplete the drain region at the channel–drain interface using the proposed method and as such it is not useful to suppress the ambipolar conduction for drain dopings greater than 1×10^{19} cm^{-3}.

To investigate the impact of process variations in the placement of high-k oxide, we simulated the device for misalignments in the position of the high-k oxide. The transfer characteristics of the HDB p-n-p-n TFET change only slightly when the high-k BOX is placed halfway under the channel, as shown in Fig. 7. The ON-state current reduces slightly (~1.4 times) and the ambipolar current also reduces slightly. This can be understood from the band diagram of the misaligned HDB p-n-p-n TFET [Fig. 7 (inset)] and the HDB p-n-p-n TFET (Fig. 8). The slight reduction in the ON-state current is attributed to the increase in the potential barrier due to the further depletion of the channel region at the drain side. The decrease in the ambipolar current is also due to the enhanced depletion of the channel region, which widens the tunneling width on the drain side. Thus, the suggested approach is immune to misalignments even when the high-k BOX is halfway under the channel.

We analyzed the HDB p-n-p-n TFET in the presence of only acceptor traps, only donor traps, and both the acceptor and donor traps at the Si/HfO_2 interface. The density and the position of the traps in the bandgap, which results in the lowest ON-state current and the highest OFF-state current in TFETs [23] were chosen to consider the worst case scenario. For the acceptor traps, a trap density of 5×10^{13} cm^{-2} located 0.6 eV below the conduction band and for the donor traps, a trap density of 5×10^{12} cm^{-2} located 0.2 eV above the valence band were used [23]. The capture cross section for the traps was obtained from [24]. Fig. 9 compares the transfer characteristics of the HDB p-n-p-n TFET with different types of traps. It was observed that the acceptor traps further reduce the ambipolar conduction while the donor traps enhance the ambipolar conduction.

The electron concentration contour plot in the presence of both types of traps is shown in Fig. 10. The ionized acceptor traps are negatively charged, and therefore, help in deplet-

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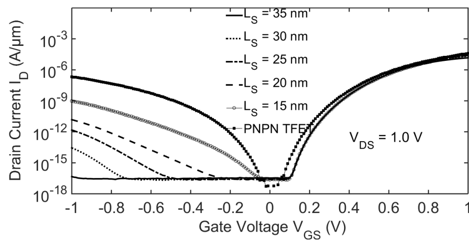

Fig. 11. Effect of spacer length (L_S) on the transfer characteristics of the HDB p-n-p-n TFET with $t_{\mathrm{BOX}} = 25$ nm.

ing the drain region further at the channel–drain interface, reducing the ambipolar conduction. However, the ionized donor traps are positively charged, therefore, lead to accumulation of electrons at the bottom of the drain and screen the depletion of the drain region at the channel–drain interface by the high-k BOX as can be observed from Fig. 10. However, when both the types of traps are used, the acceptor type traps dominate due to their high density and the transfer characteristics are similar to those with only acceptor traps present.

We investigated the effect of spacer length (L_S) on the transfer characteristics of the HDB p-n-p-n TFET, as shown in Fig. 11. The voltage range for which the ambipolar current is suppressed increases with an increase in the spacer length (L_S). This is because the drain region is effectively depleted at the channel–drain interface as the drain contact is further separated from the interface. For a spacer length of 35 nm and above, the ambipolar current is completely eliminated even up to a $V_{\mathrm{GS}} = -1$ V. Even for a spacer length of 15 nm, the ambipolar current is not completely suppressed in HDB p-n-p-n TFET but the magnitude of ambipolar current at $V_{\mathrm{GS}} = -1$ V is three orders of magnitude less than the ambipolar current of the conventional p-n-p-n TFET.

IV. Conclusion

In this brief, we have proposed a p-n-p-n TFET with reduced ambipolar current using an HDB along with a heavily doped (p^+) ground plane substrate. We have demonstrated using 2-D simulations that the presence of the HDB above the heavily doped ground plane effectively depletes the drain region at the channel–drain interface resulting in insufficient band bending for tunneling to occur even for a large negative gate bias. The suggested device architecture can suppress the ambipolar conduction up to a gate voltage of -0.8 V when the HDB thickness is 25 nm and the spacer length is 30 nm. We analyzed the effect of interface traps on the performance of the HDB p-n-p-n TFET. The proposed HDB p-n-p-n TFET could be an attractive alternative to the conventional p-n-p-n TFETs even for the digital circuit applications.

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